SGS-THOMSON MICROELECTRONICS

AN556
APPLICATION NOTE

THE L6353: A SMART GATE DRIVER

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The superior performance of voltage controlled switch makes this device the preferred one in modern power electronics applications.

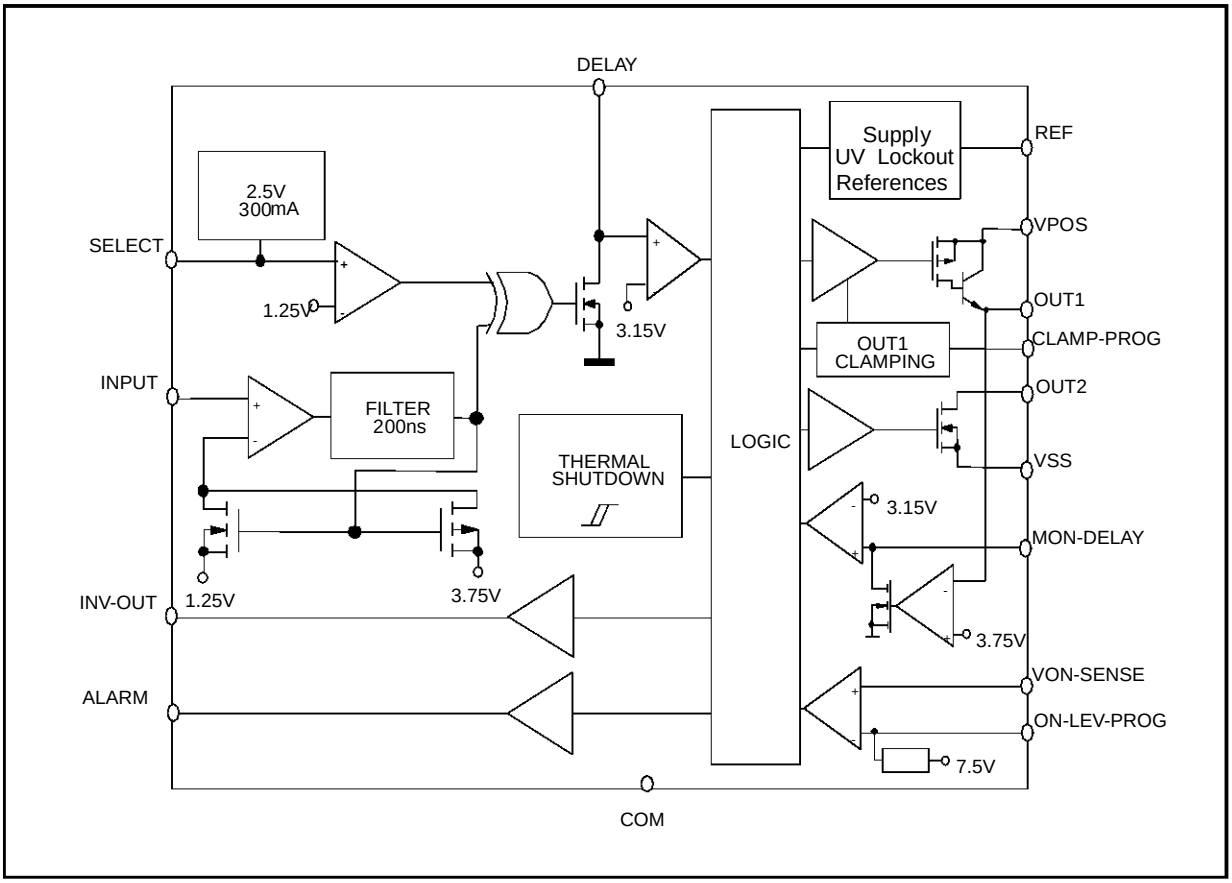
The L6353 is a new monolithic integrated circuit designed to realise a versatile and smart interface between the signal circuitry and every kind of voltage controlled power switch, with a minimal design time and a reduction of parts count.

Device Description

The L6353 is a smart silicon device which integrates all the circuitry for a versatile and rugged gate driver. The chip implements several features such as: an easy-to-link signal source by means of either an optocoupler or pulse transformer, a two-step turn-on procedure of the external power switch (dedicated to IGBT driving), a switch dropout voltage monitoring, the possibility to give a negative bias to the gate, the external programmability of safety thresholds and delays, the syncronisation and edge aligning and a powerful buffer of ±8A with split output.

To introduce the device see fig.1 which shows the functional diagram:

Figure 1. L6353 - Functional diagram



FUNCTIONAL DESCRIPTION

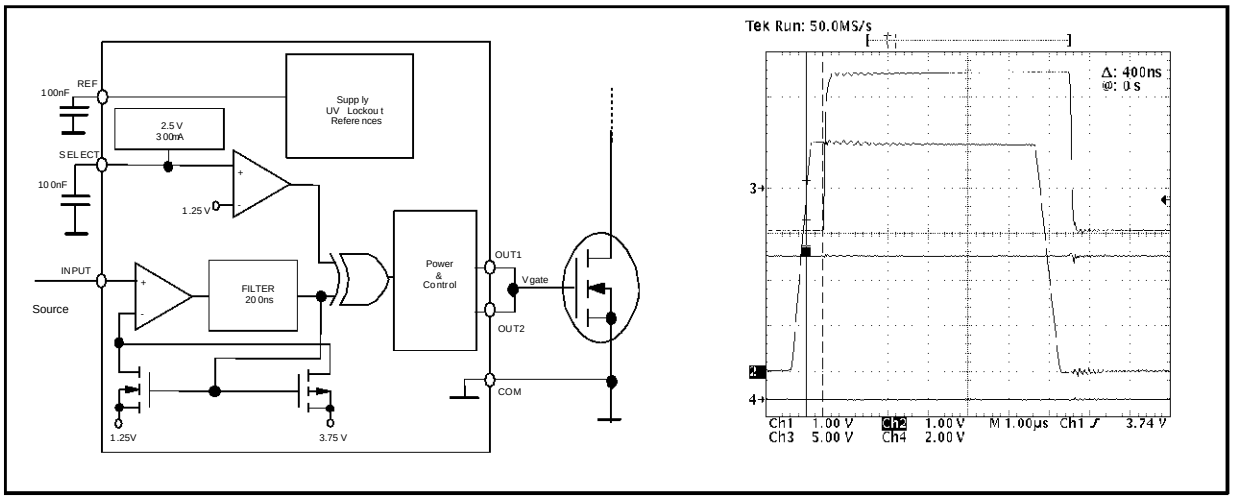
Interfacing L6353 to the signal source

A typical switching application requires a good noise immunity on the incoming signal to avoid the switch false triggering (turn-on/turn-off). Besides, electrical isolation and level shifting between the power and the signal parts can be needed. The L6353 is designed with the reference thresholds of control signal at 3.75V on rising edge and 1.25V on falling-edge (compatible with the CMOS output-levels), a fixed 200ns analog filter to eliminate glitches and some tricks to ease linking to the signal source.

Figures 2, 3 and 4 sketch some practicable circuits and show the main signals.

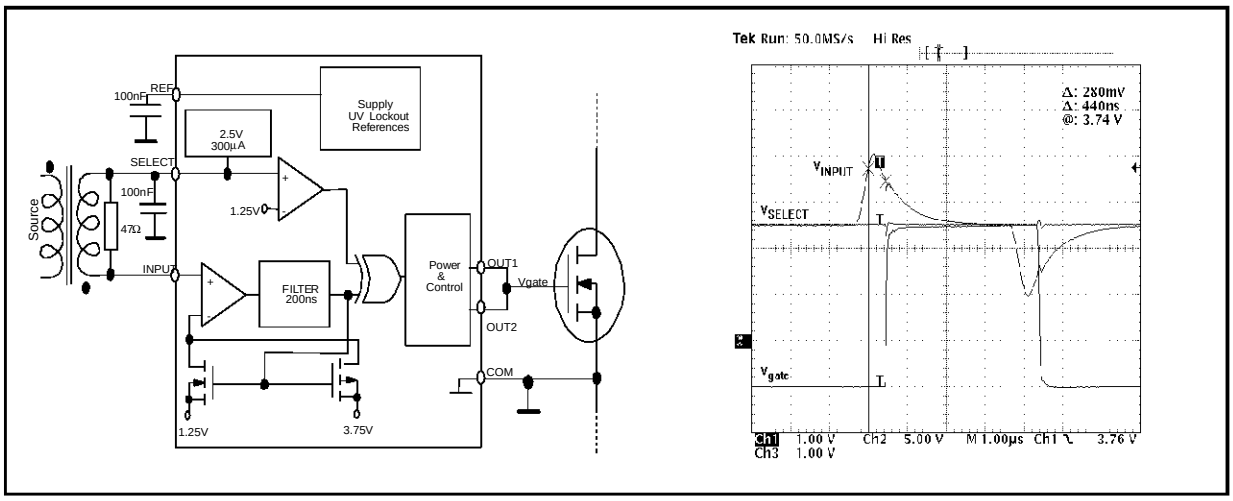
Fig.2 shows the direct feeding of control signal to the INPUT pin. The gate is driven in-phase by leaving the SELECT pin ats 2.5V (the phase is reversed if the pin is grounded).

Figure 2. Direct interfacing and main waveforms.



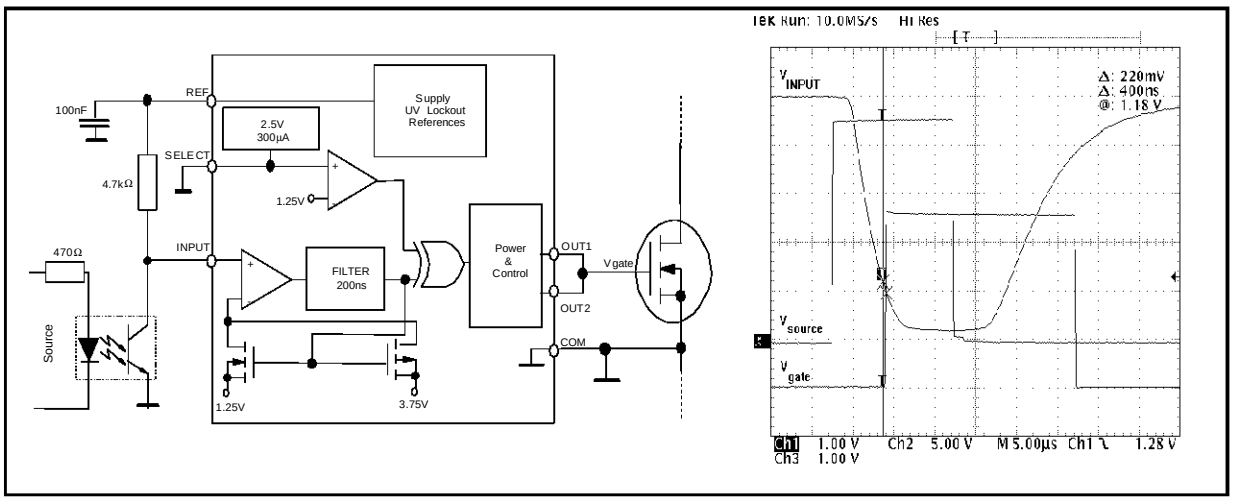
In applications requiring electrical isolation, the SELECT pin is designed especially for biasing a pulse transformer. Then, the quiescent level at INPUT pin is shifted to 2.5V and there is a differential threshold of +1.25V at switch-on and -1.25V at switch off.

Figure 3. Pulse-transformer interfacing and main waveforms.



A cheap way to get the electrical isolation resorts to an optocoupler. In this case, the built-in 5V at VREF pin can be used to bias the optocoupler and, of course, the SELECT pin allows to manage the phase.

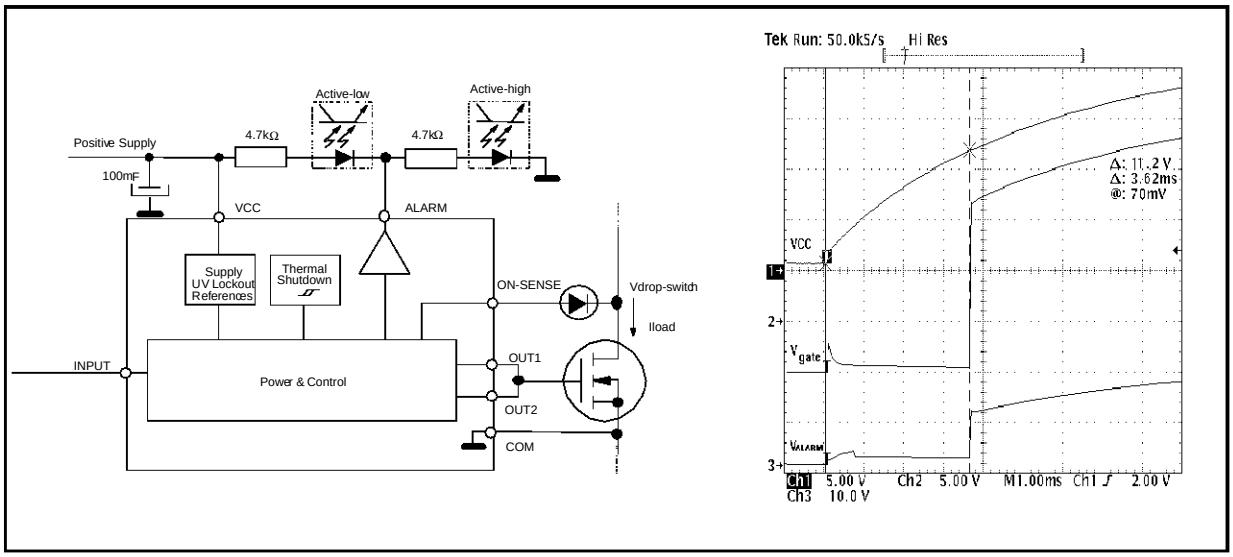
Figure 4. Optocoupler interfacing and main waveforms.



Failure warning at the alarm output

The L6353 sends an alarm signal in case of fault detection either in the chip or in the driven switch. The system monitors chip temperature, chip supply voltage and the switch voltage drop in on state. The fault signal, available at ALARM pin, is active low. The totem-pole output, with ±20mA current capability, is also useful (see fig.5) to get a signal either high or low on fault.

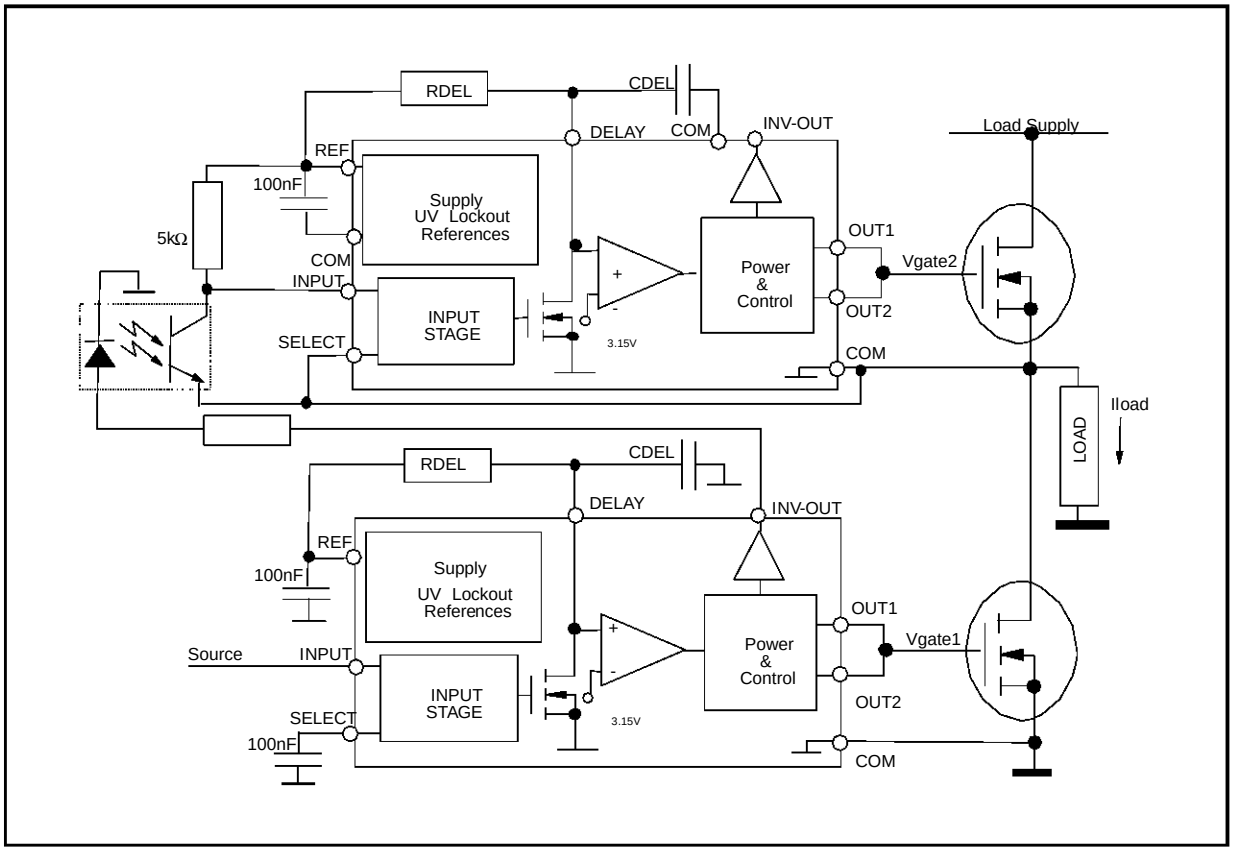
Figure 5. ALARM circuitry and waveforms on power-on.



Synchronising more switches

Often, more switches must work synchronously. The synchronisation is always guaranteed by using the signal at OUTPUT instead of the one at INPUT, because of the L6353 safe processing. The INV-OUT pin is suitable for this function (see fig.6) because it sends a signal out of phase with the output, with ±20mA of current capability.

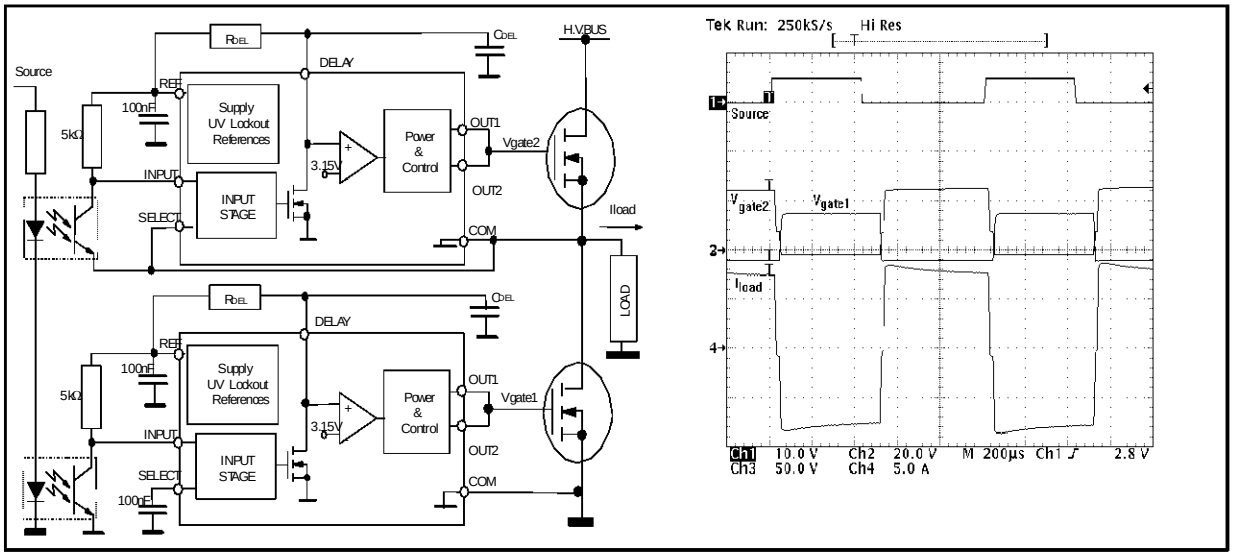
Figure 6. Master/Slave synchronisation.



Aligning the switching edges

In inverter leg applications the difference in response time of each switch can lead to simultaneous conduction. An easy way to align the switch edges is to place an adequate delay in the signal path of each driver. The L6353 is provided with the DELAY pin to adjust the INPUT-to-OUT1 lag at turn-on by means of an RC cell connected to the REF pin (see fig.7).

Figure 7. Input to output delay circuitry.



The relationship between the RC parts value and the internal timing circuitry is:

$$t_{DELAY} = R_{DEL}\, C_{DEL} \quad [1]$$

where:

R_{DEL} is the timing resistance [kΩ]

C_{DEL} is the timing capacitance [µF]

t_{DELAY} is the input to output delay time [µs]

t_{DELAY} should be calibration on the difference in response time of the external parts (e.g. optocoupler, switch).

The DELAY pin always needs a pull-up resistor.

Protection against failure

To avoid system damage, it is mandatory not to exceed the SOA of the selected switch. To better understand how to respect these limits, the relationships describing the operating conditions of a voltage controlled switch are here reminded:

$Is \approx 0$ $Vg < Vth$ (off mode) [2a]

$Is \propto Vd$ $Vd < Vg-Vth$ (on mode) [2b]

$Is \propto (Vg-Vth)^2$ $Vd > Vg-Vth$ (linear mode) [2c]

where :

Is is the current through the switch

Vd is the switch drop voltage

Vth is the activation threshold voltage

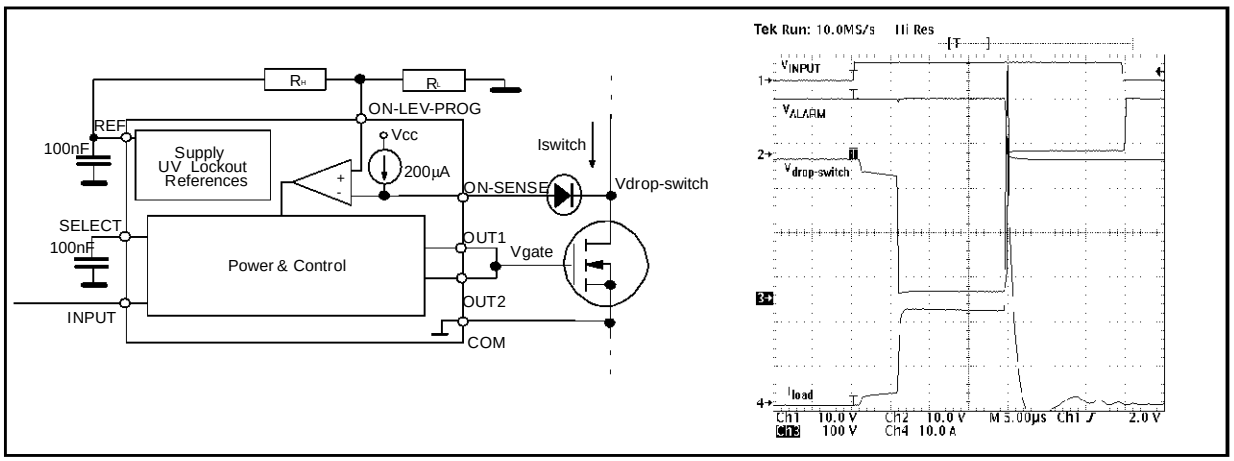
Vg is the driving gate voltage

The [2a] states that the switch current is negligible as long as the gate voltage is under the activation threshold; the [2b] states that the on state voltage drop across a well driven switch is usually very low; the [2c] states that the voltage drop across a bad-working switch, is always higher.

Protection against steady-state switch overload

The equations [2b] and [2c] suggest an easy way for a load failure detection by monitoring the switch voltage drop. The L6353 performs this function connecting the ON-SENSE pin as shown fig.8. The function is turned off by shorting this pin to COM. The diode must be ultra-fast and have the same voltage rating as the external switch. A load failure is detected by comparing the sense voltage to a reference level. On failure detection, the L6353 turns off immediately (<400ns) the switch and sets the ALARM low. The INPUT falling edge resets the driver. For an improved versatility, the ON-LEV-PROG pin allows to

Figure 8. Load failure protection



change (by means of a resistive divider) the reference level from the default 7.5V, in the range 5V - 15V. The relationship between the reference level and the resistive divider (from REF pin) is:

$$V_{ON\text{-}LEV\text{-}PROG} = 0.17\ V_{ON\text{-}SENSE} \quad [3a]$$

$$V_{ON\text{-}LEV\text{-}PROG} = \frac{V_{ref}\ R_L}{R_H + R_L} \quad [3b]$$

Of course, $V_{ON\text{-}SENSE}$ is the switch voltage drop (when it is carrying the overload current) plus a diode forward drop. The graph of fig. 9 helps design: you draw a line crossing the VL-P axis at $V_{ON\text{-}SENSE}$ and read the resistor value on the other two axes. The divider is tuned by solving equations [3a] and [3b]. The example shows how to set the maximum drop voltage to 7V (+0.7V) using two resistors of 22k and 6.8k.

Safe turn-on of power switch on a low-impedance load

If you turn on a switch connected to a low-impedance load (for example: a short circuit) by feeding the gate a full voltage then high switch currents will occur (see [2c]). In IGBT's, such a current can be so high to fire the parasitic SCR, which destroys the switch (LATCH-UP). The L6353 avoids this risk with a safe turn-on procedure in two steps (see fig.10): on the first step it does not monitor the switch voltage drop but limits the switch current by clamping the gate voltage; on the second step it applies the full voltage at switch gate while the voltage drop is monitored.

Figure 9. LEVEL-PROG graph

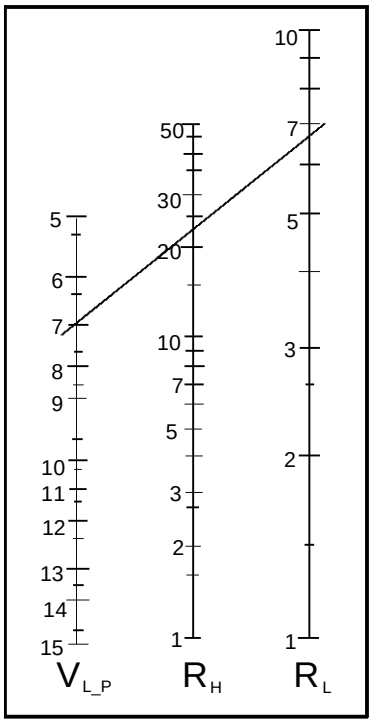
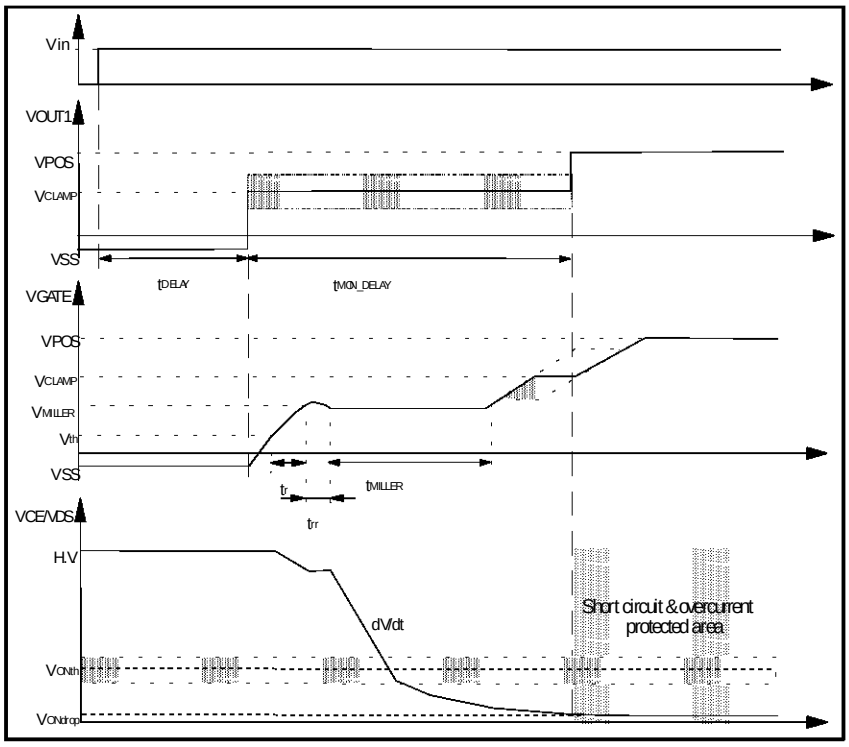


Figure 10. Power switch protection method



The relationships between the gate clamped voltage and a resistive divider (from REF pin) is:

$$V_{CLAMP\text{-}PROG} = 0.17\ V_{CLAMP} \quad [4a]$$

$$V_{CLAMP\text{-}PROG} = \frac{V_{ref}\ R_L}{R_H + R_L} \quad [4b]$$

where:

$V_{CLAMP\text{-}PROG}$ is the CLAMP-PROG pin voltage
V_{CLAMP} is the first step gate voltage

The following relationships provide the way to relate V_{CLAMP} to the switch characteristics:

$$V_{CLAMP} = V_{MILLER} + V_{OVR} \quad [4c]$$

$$V_{MILLER} = V_{th} + \frac{I_{S0}}{g_{fm}} \quad [4d]$$

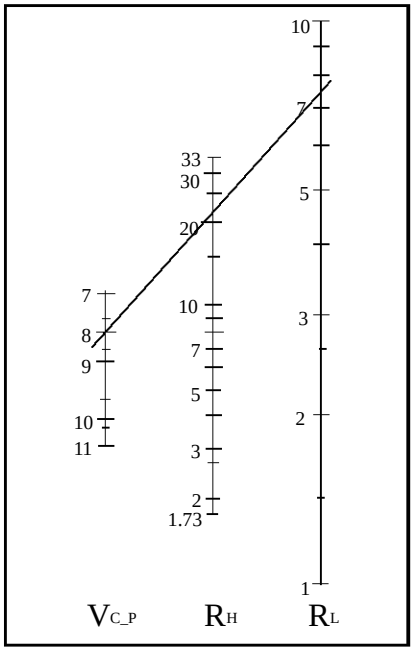
where:

V_{MILLER} is the gate voltage during Miller's modulation of gate capacitance.
V_{OVR} is the Miller's excess voltage for a fast turn-on
g_{fm} is the power switch transconductance
I_{S0} is the nominal load current

The graph of fig.11 helps find the resistors values: you draw a line crossing the VC-P axis at V_{CLAMP} and read the resistors value on the other two axes. The divider is tuned by solving the equation [4a] and [4b]. The example shows how to set the gate-clamped voltage to 8V using resistors of 22k and 7.5k.

In case the switch is a MOS, which does not suffer from latch-up, then the function can be excluded by shorting the CLAMP-PROG pin to COM.

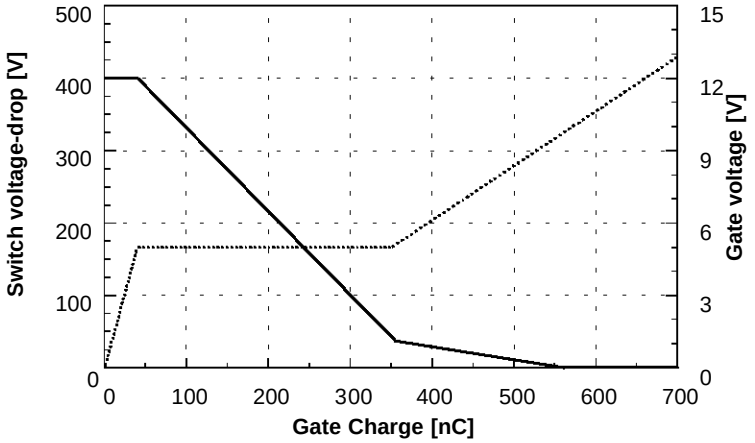
Figure 11. CLAMP-PROG graph



Delaying the monitor function

Fig.12 shows the characteristics of a typical voltage controlled switch.

Figure 12. Typical voltage controlled switch characteristics



To reach the gate voltage needed for a full conduction of the switch, a certain amount of charge (depending both on the switch and the application) must be stored into the gate capacitance. Since this is charged with a limited current source, the switch turn-on transition needs some time. This means that until transition is completed, the monitoring of the switch voltage drop must be blanked. The relationships between the blanking time and the RC cell (from REF pin) is:

$$t_{MON\text{-}DELAY} = R_{EXT}\, C_{EXT} \quad [5a]$$

where:

$t_{MON\text{-}DELAY}$ is the monitoring signal blanking time [µs]
R_{EXT} is the timing resistance [kΩ]
C_{EXT} is the timing capacitance [µF]

On the other hand, the time to reach the true low voltage drop is the sum of the turn-on time, the transition time of the switch at loading conditions and a margin time for the spread (limited only by the switch thermal performance), so:

$$t_{MON\text{-}DELAY} = t_{on} + t_{MILLER} + t_{MRG} \quad [5b]$$

$$t_{on} = R_{Gon}\, C_i \ln\left(\frac{V_{CLAMP} - V_{SS}}{V_{CLAMP} - V_{MILLER}}\right) \quad [5c]$$

$$t_{MILLER} = \frac{Q_{MILLER} - C_i\, V_{MILLER}}{V_{CLAMP} - V_{MILLER}} R_{Gon} \quad [5d]$$

where:

t_{on} is the time to reach the gate voltage threshold

t_{MILLER} is the transition duration of switch voltage

t_{MRG} is a designer time margin

Q_{MILLER} is the charge amount to go beyond the gate voltage plateau

C_i is the input gate capacitance

R_{Gon} is the charging resistance

R_{Goff} is the discharging resistance

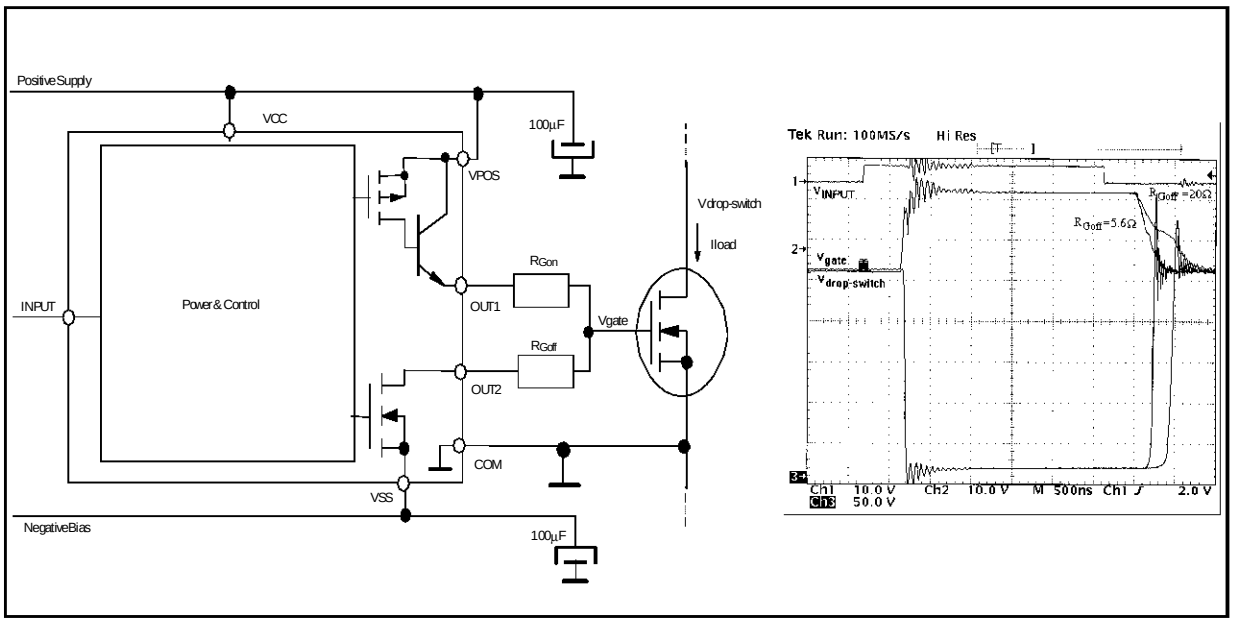
The MON-DELAY pin always needs a pull-up resistor.

Controlling the dI/dt and the static dV/dt of external power

A lot of problems in switching systems (EMI, power switch latch-up, optocoupler short-circuit, etc.) are caused by high dV/dt and dI/dt. It is easy to avoid these problems with the L6353 because the output buffer is split in high-side and low-side. In this way, only one pair of resistors is needed to shape both dV/dt at turn-off and dI/dt at turn-on. Fig.13 shows the connection of the output pins and the switch gate.

During the switch transition most of the charge flowing into the gate pin is used to balance the discharge of the Reverse Transfer Capacitance. Then, the gate voltage stops at a level which depends on load current and switch, while the gate driver is like a current source. It follows that transient duration can be approximated to charge and discharge time of this capacitance and the resistors in series to the gate

Figure 13. Typical connection between IC and the switch gate



can be designed with the relationships:

$$\left.\frac{dV}{dt}\right|_{turn-on} \cong \frac{V_{OUT1} - V_{MILLER}}{R_{Gon}\, C_r} \qquad [6a]$$

$$\left.\frac{dI}{dt}\right|_{turn-off} \cong g_{fm}\frac{V_{SS} - V_{th} - \frac{I}{2_{g_{fm}}}}{R_{Goff}\, C_i} \qquad [6b]$$

where:

t_{on}	is the duration of turn-on switch transition
C_i	is the Input Capacitance
C_r	is the Reverse Transfer Capacitance
R_{Gon}	is the charging resistance
R_{Goff}	is the discharging resistance
g_{fm}	is the transconductance of the external power

Driver supply

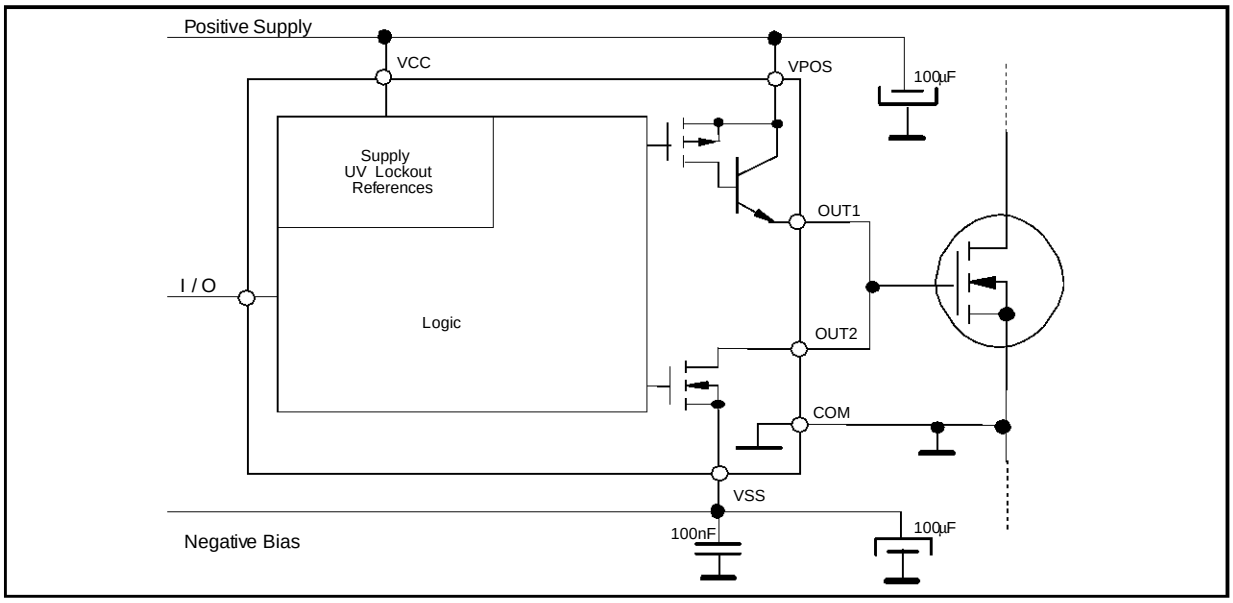
The L6353 is provided with separated pins for its supply: one for control circuits (VCC) and two for the power circuits (V_{POS}, VSS). An undervoltage circuitry monitors the control circuits supply and ties OUT2 to VSS as long as VCC voltage is under 11.5V, while the ALARM is low. The power circuits positive pole (V_{POS}) can be connected to VCC. The negative pole (VSS) is useful to increase the dV/dt latch-up immunity of the switch by feeding a negative bias to its gate (up to -7V). If the negative bias is not required, VSS can be connected to COM.
To supply the device it must be considered that a buffer capacitor is needed to sustain the current pulses absorbed by V_{POS} at switch turn-on. The buffer capacitor must be designed considering the rms values of this pulsed current:

$$I_{Grms} \geq \sqrt{\frac{V_{POS} \cdot Q_{GATE} \cdot f_{sw}}{3R_{Gon}}}$$

Using the same considerations, the buffer capacitor on VSS (if used) withstands the rms current that is:

$$I_{Grms} \geq \sqrt{\frac{VSS \cdot Q_{GATE} \cdot f_{sw}}{3R_{Goff}}}$$

Figure 14. Optimal supply



where:

I_{rms}	is the capacitors rms current
Q_{GATE}	is the total amount of gate charge
V_{POS}	is the steady-state gate voltage
VSS	is the negative supply voltage
$R_{Gon/off}$	are the gate resistance at turn-on and at turn-off
f_{sw}	is the operating frequency

Thermal balance and Frequency limitation

The L6353 improves the system reliability integrating a circuit which monitors the chip temperature. There are a temperature sensor and a comparator stage with two very precise thresholds: at 130°C the chip sends the alarm signal but keeps on working and at 160°C shutdowns the output stage. It follows that a design with L6353 is easy because just few data allow to estimate the chip temperature: operating conditions, power dissipated and package thermal characteristic.

$$T_j = R_{th} P_D + T_a \qquad [8a]$$

$$P_D = P_Q + P_{AL} + P_{INV} + P_{SW} \qquad [8b]$$

$$P_Q = I_Q V_{CC} + I_{REF} (V_{CC} - V_{REF})$$

$$P_{AL} = I_{AL} V_{DROP} D$$

$$P_{INV} = I_{INV} V_{DROP} D$$

$$PSW = \{[(VP_{OS}-V_{CLAMP}) (Q_{MILLER}-V_{SS} C_i)+2(V_{POS}-V_{OUT1}) (V_{POS}-V_{OUT1} -V_{MILLER})C_i+ (V_{OUT2}-V_{SS}) [V_{POS} C_i + Q_{MILLER}-V_{SS} C_i]\}f \qquad [8c]$$

where:

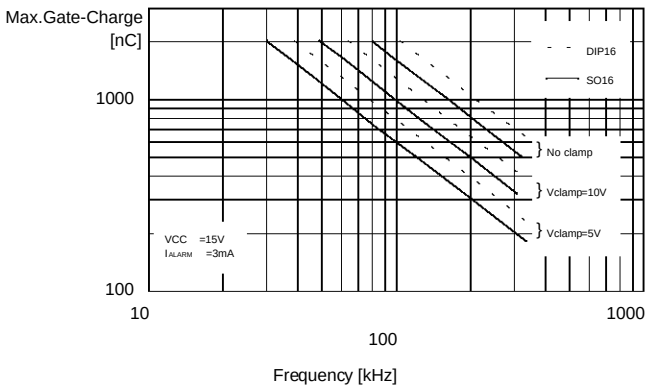
P_D	is the total power dissipated
P_Q	is the quiescent power dissipated in the chip
P_{INV}	is the power dissipated using the INV-OUT function
P_{AL}	is the power dissipated using the ALARM function
P_{SW}	is the operative power dissipated during transition
D	is the switch duty-cycle
R_{th}	is the package thermal resistance

Substituting into [7a] and rewriting:

$$P_{SW} \leq \frac{T_j - T_a}{R_{th}} - P_Q \qquad [8d]$$

For the total gate charge of the switch, considering the over heating alarm threshold and the available packages, the relationship [8d] states a limit of operating frequency (see fig.15).

Figure 15. Maximum Gate-Charge vs Operative



Promotional tool for L6353

Fig.16 shows a printed circuit board where it is possible to assembly one of the following circuits with possibility to try different set-ups: (optocoupler either open-collector with a pull-up resistor or totem-pole output needing 5V supply; a switch which can be either MOSFET or IGBT with a free-wheeling diode mounted on a heat-sink).For more complex configurations like inverter legs, bridge etc. two or more of them can be connected together.

The PCB has also the aim to introduce a few layout rules to avoid interference and parasitic effects which arise switching high current. Firstly, on single-supply driving, a minimal track length between VSS and COM pins is mandatory. On the supply tracks, the capacitor location is very close to the IC pins. The pin COM must be connected near the supply capacitor. It is necessary to take special care of the switch pin used for both power and control, which is connected to the supply capacitor by a separated, wide and short track. Finally, a ground track must be put under each optocoupler to improve its dV/dt immunity.

Figure 16. Printed Circuit Board (scale 1:1)

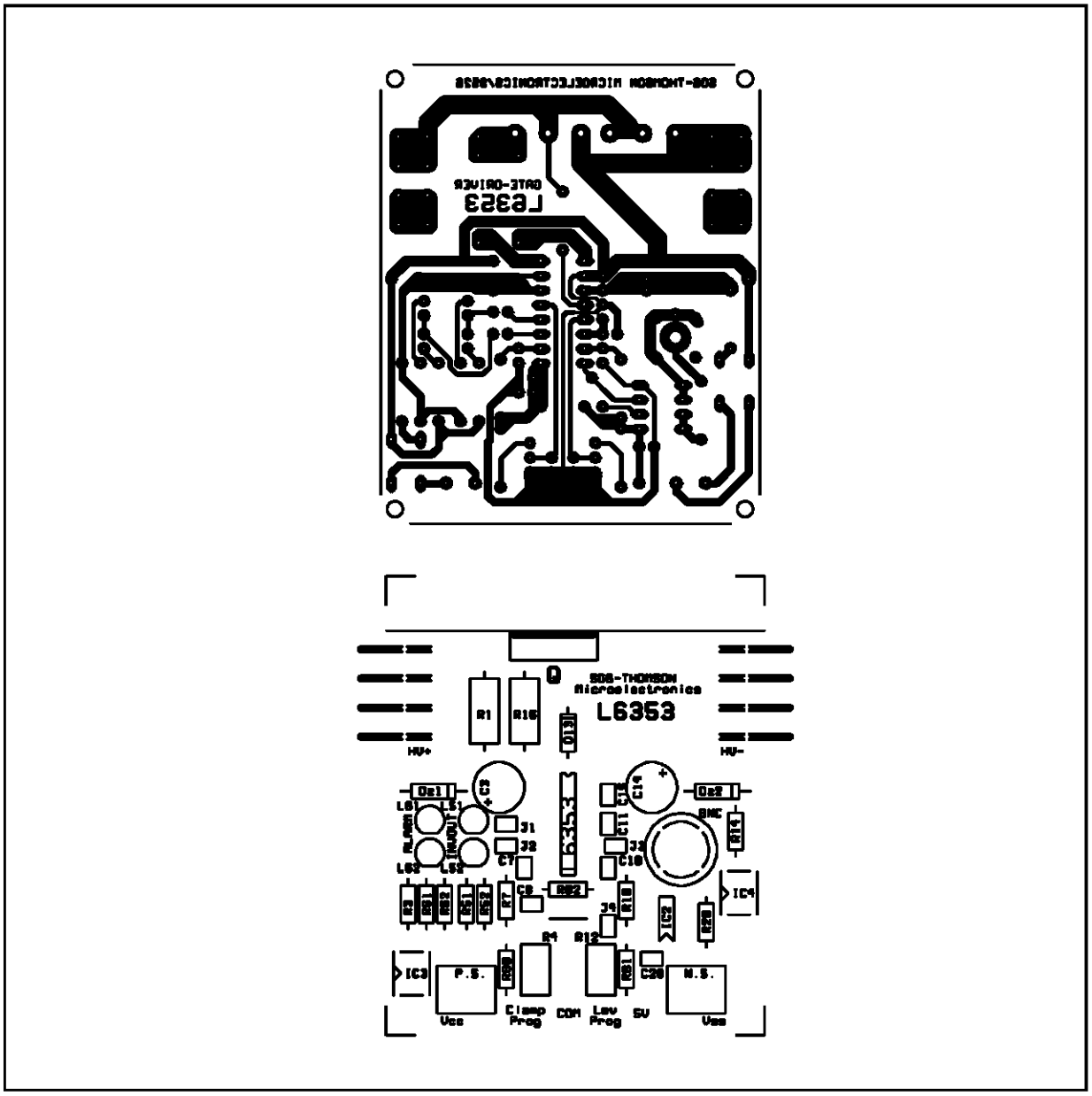
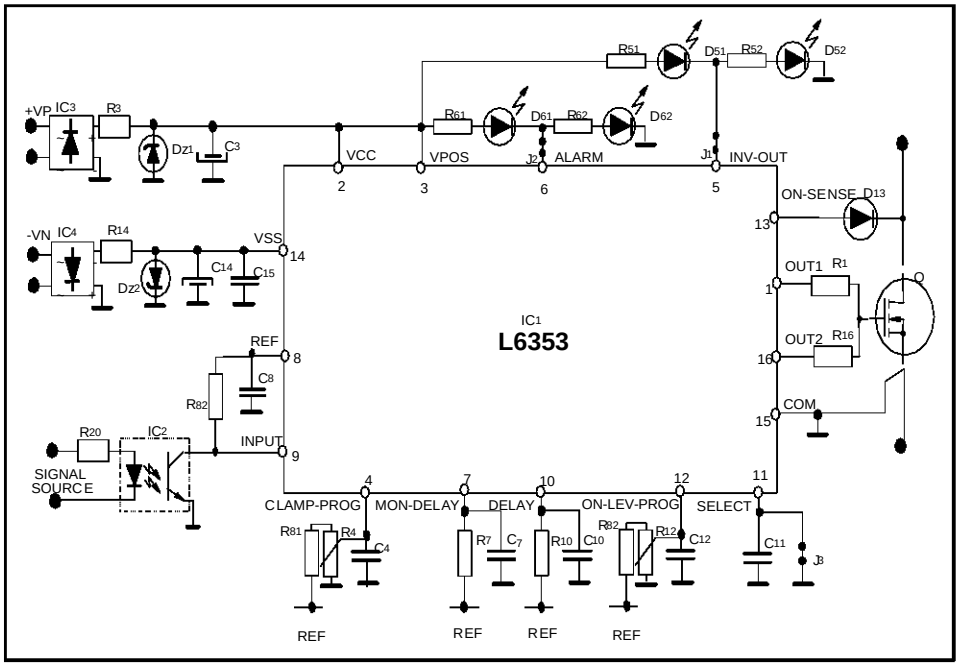


Figure 17. TEST-circuit schematic.

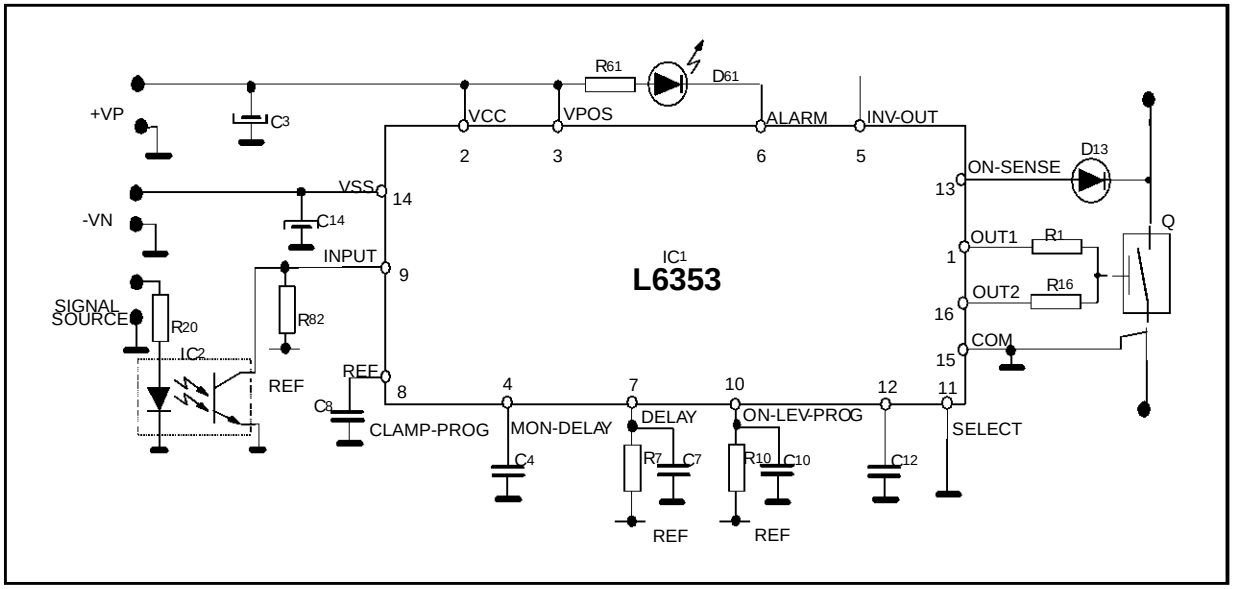


Parts List

IC1 = L6353
IC2 = 4N25
IC3 = Bridge Rectifier
IC4 = Bridge Rectifier
D1 = BYT11-1000
D51 = YELLOW LED
D52 = YELLOW LED
D61 = RED LED
D62 = GREEN LED
Dz1 = BZX85C6v8
Dz2 = BZX85C20
R1 = 1.2Ω - 1W (metal)
R3 = 10Ω-0.5W (metal)
R61 = 10kΩ -.25W
R7 = 4.7kΩ-.25W -1%
R10 =4.7kΩ-.25W - 1%
R14 = 100Ω-0.5W (metal
R16 = 5.6Ω - 1W (metal)
R20 = 470Ω -.25W
R80 =4.7kΩ-.25W
R81 = 4.7kΩ-.25W
R82 = 4.7kΩ-.25W
C3 = 100µF-25V (low ESR)
C4 =100nF (multi)
C7 = 1nF (multi)
C8 = 4.7nF (multi)
C10 = 1nF (multi)
C12 =100nF (multi)
C14 =100µF- 25V(low ESR)
Q = STW20NA50 *

Since it can be used stand-alone, there is an excess of parts: the supply circuitry (the rectifier bridges, zeners and limiting resistors) is designed to feed a floating double polarity connecting only a transformer; the control source is coupled with an optocoupler; the clamped gate-voltage and the maximum voltage drop allowed across the switch can be trimmed at values that are best matching the switch characteristic (either default or otherwise); two LED connected to the ALARM that are exclusively brightening to indicate the board status: either normal or fault; two LED connected to the INV-OUT (just to show the signal). In fig. 18, a typical application circuit, pruned of the parts in excess, is shown.

Figure 18. Typical application schematic.

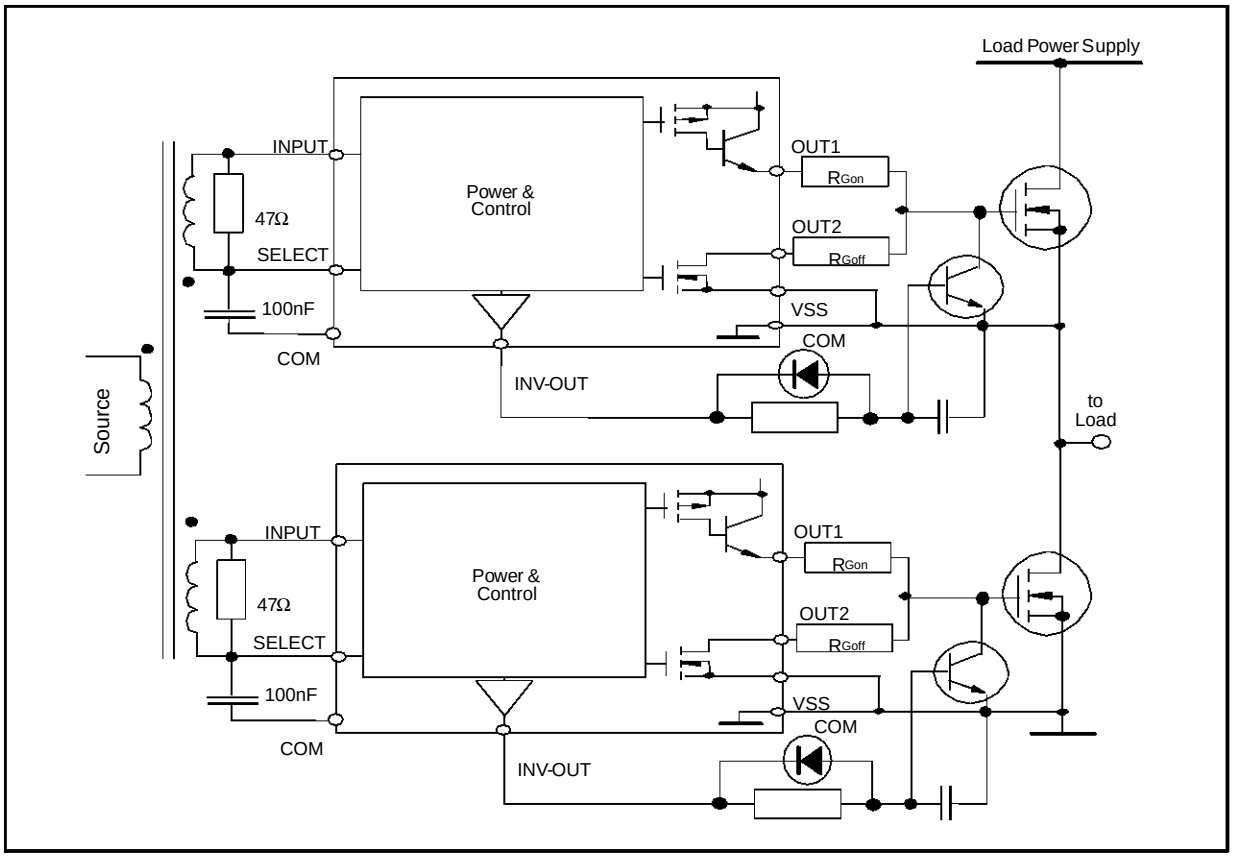


APPLICATION SUGGESTIONS

- extension of INV-OUT

The switch immunity against static dV/dt is weakened by requirements of single supply or slow turn-off. An improvement is made by tieing, at turn-off, the gate to the common pin of theswitch. This is easily implemented by the INV-OUT pin with a cheap additional circuit: a small BJT, a capacitor and a resistor with a diode in parallel to speed-up the BJT turn-off. The BJT does not have to carry the gate discharge current, so it can be of a small size. Fig.19 shows a practical example of its usage:

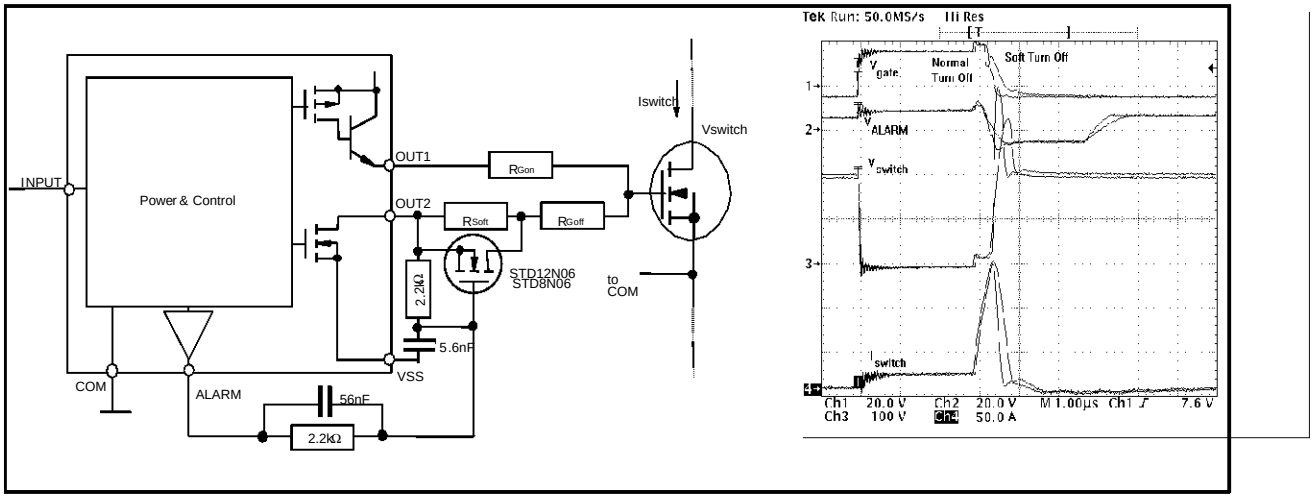
Figure 19. Improved dV/dt immunity on single supply



- Soft Turn-Off in any switch overload conditions

Fig.20 shows a simple circuit which implements this function; the waveforms show both the high voltage overshoot if you use the normal switch-off speed on load short-circuit and the short voltage overshoot if you use the soft turn-off. The typical off resistor values are in the range of the same hundreds Ohm in ”soft turn-off” and up to some tens Ohm in normal switch-off.

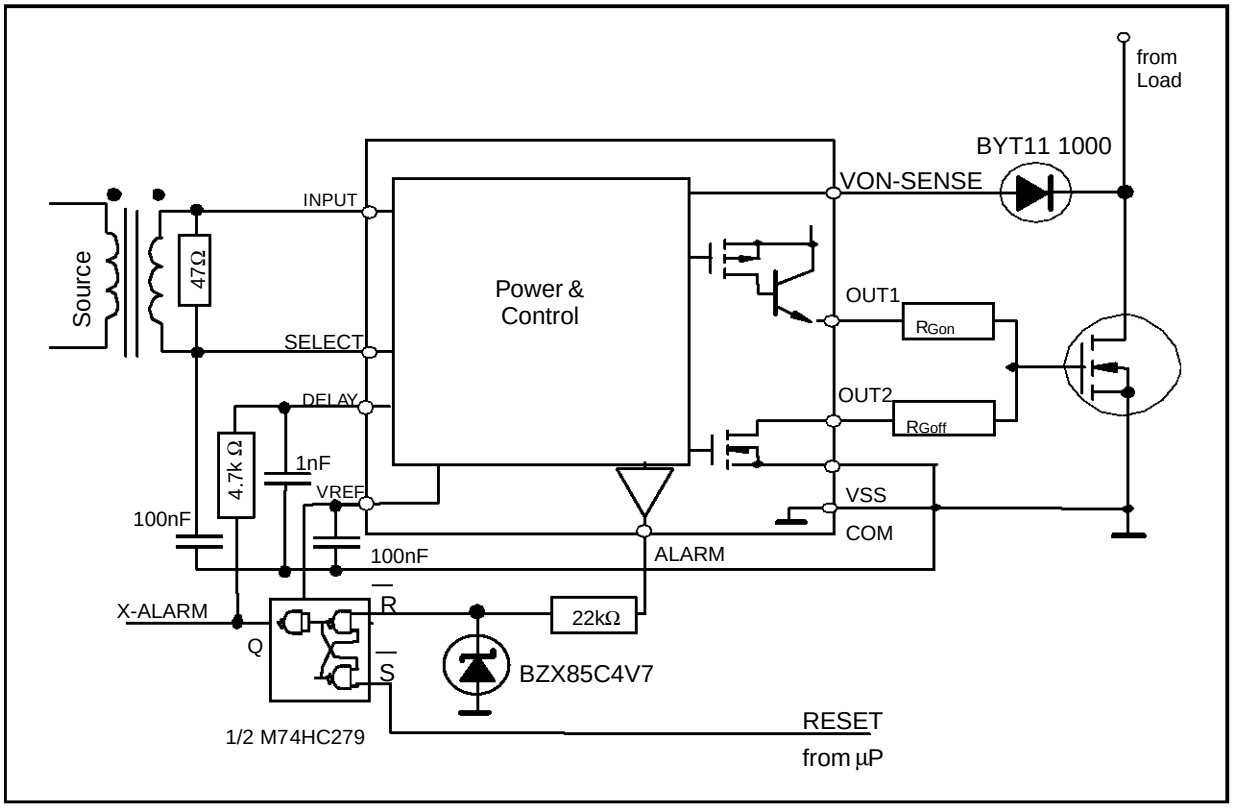
Figure 20. Soft Turn Off circuit and waveforms



- First failure hold-off with external reset

Fig.21 shows a simple circuit which holds in off state the switch after the first failure ALARM. On switch failure (eg. an overload), the ALARM disables the INPUT control signal and the driver normal operation is resumed by a low level pulse on Reset.

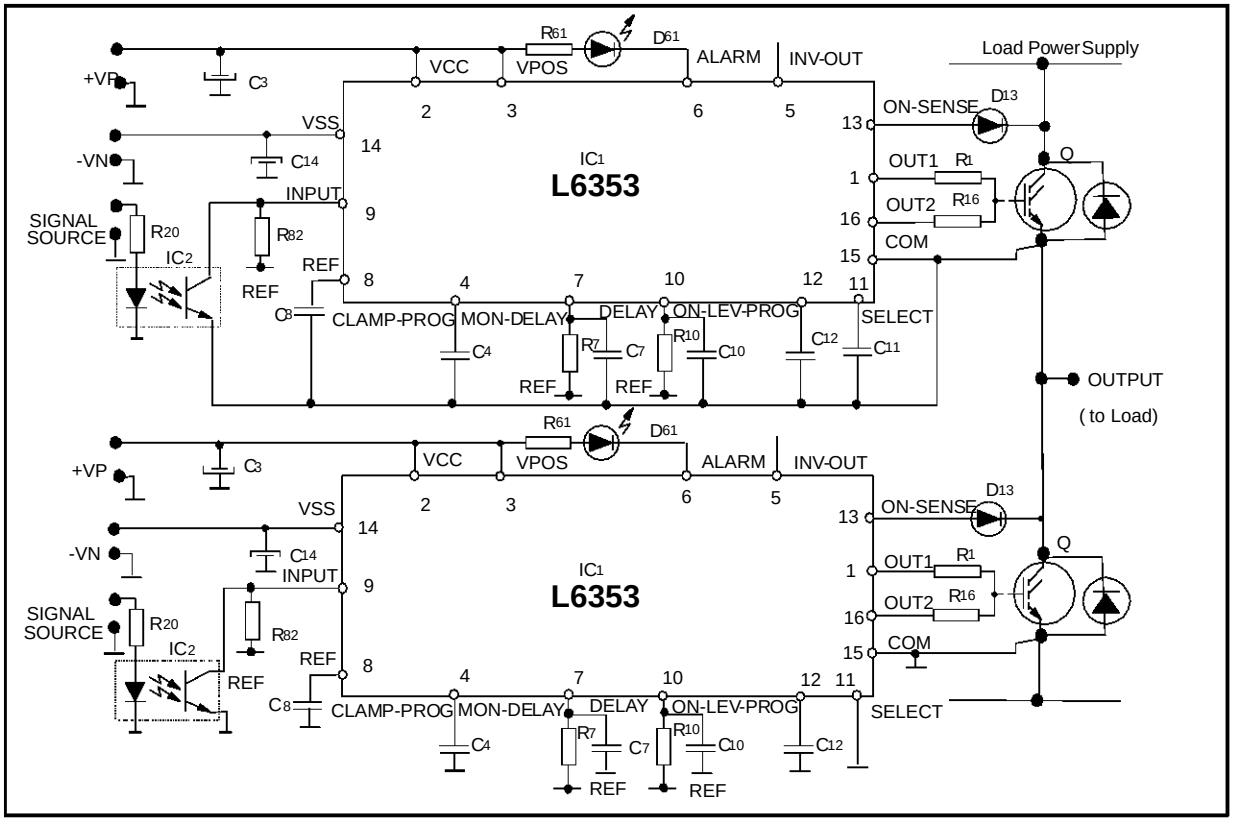
Figure 21. First failure hold-off with external reset circuit



- an Inverter leg

Fig.22 shows a leg of an Inverter and also highlights how you need few parts for its construction. Of course, to test this circuit two Demo-PCB, linked side-by-side, can be used. The two boards joining point is the middle of the leg, which is connected to the load, and the remaining two are connected to the load power supply.

Figure 22. Inverter-leg.



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