

TDA9102C SELECTION vs HORIZONTAL DUTY CYCLE

By Michel GUILLIEN

CONTENTS	Page
I. INTRODUCTION	1
II. DUTY CYCLE CALCULATION	2
II.1. DUTY MIN.	2
II.2. DUTY MAX.	3
II.3. TYPICAL LIMITS.	4
III. APPLICATION FOR INCREASING THE DUTY CYCLE OF A TDA9102C	5
III.1. STANDARD APPLICATION	5
III.1.1. Modified Application	5
III.1.2. Components Calculation in Modified Application	6
III.1.3. Summing	6
IV. APPLICATION FOR DECREASING THE DUTY CYCLE OF A TDA9102C	6
IV.1. STANDARD APPLICATION	6
IV.1.1. Modified Application	7
IV.1.2. Components Calculation in Modified Application	7
V. CONCLUSION	8

I. INTRODUCTION

The TDA9102C is a horizontal and vertical deflection processor particularly well suited for high end monitors.

One of the key parameters is the very low jitter of the horizontal deflection processor.

The horizontal duty cycle is the ratio between the time during which the line switching transistor receives an off command and the line period.

As the monitors are using more and more various and higher line frequencies, this duty cycle must be well adapted to the actual application.

The following pages show how to calculate the min and max duty cycle for which typical application can

work.

For the rare cases where the TDA9102C do not fit to the used diagram, a simple application is given, both to increase or to decrease the device duty cycle. It is anyway important to note that the experience shown that in most of the case, when the TDA9102C does not fit the application, it is because of too low value. Consequently, mainly the application to increase the duty cycle will be used.

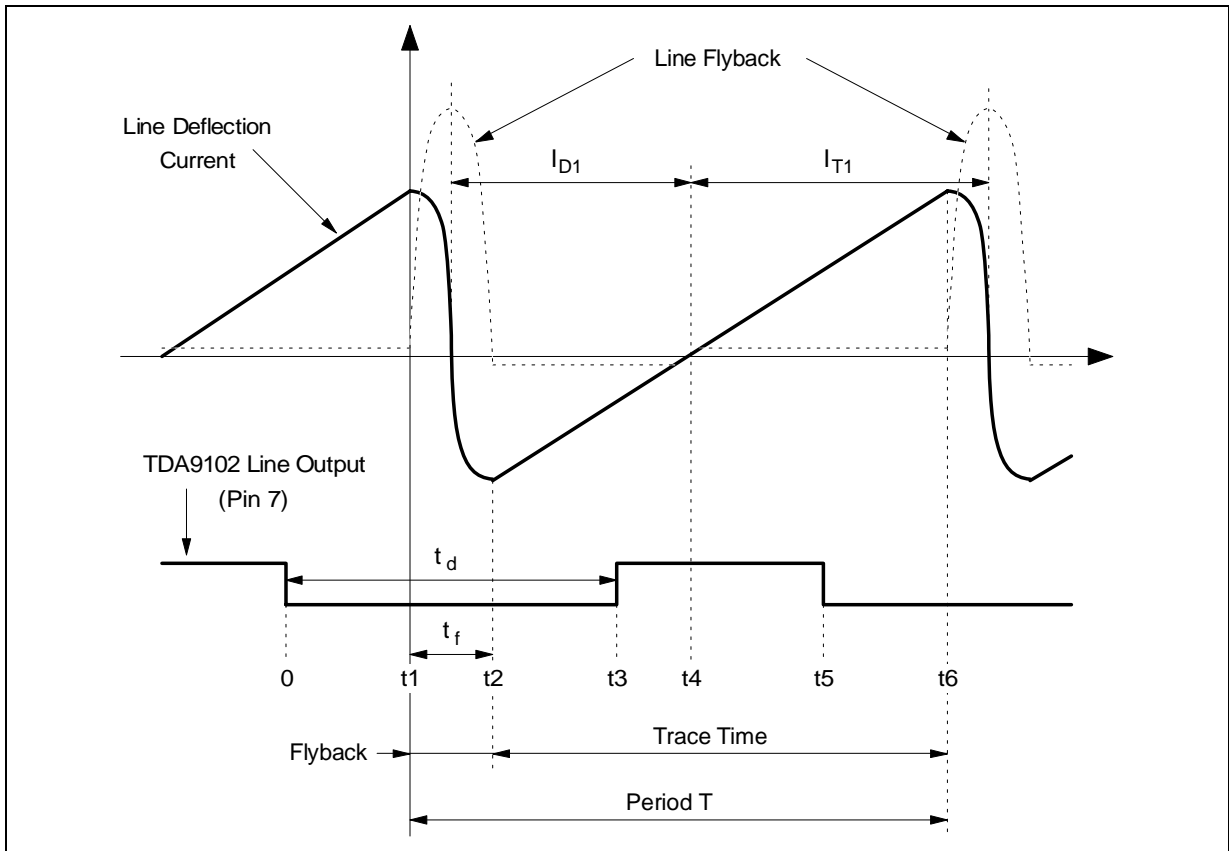
Nota Bene :

For a quick over view a floppy disk is available using the formulas given here-after and allowing to find at once the right application.

For starting the program, just type "9102"

II. DUTY CYCLE CALCULATION

Figure 1



II.1. Duty Min.

- When the output of the line processor turns low, it takes a time t_1 , before the line switching transistor actually turns off.
- Then it takes a time $t_f = t_2 - t_1$ for the current in line yoke to invert (fly back time)
- As soon as the flyback is finished, the line transistor may be turned on again, although it will actually conduct only when the line current becomes positive (at t_4).

Thus the minimum off time t_d is :

$$t_{d \min} = t_{1 \max} + t_{f \max}$$

Since the duty cycle is defined as $\frac{t_d}{T}$ where T is the

line period : $d_{\min} = (t_{1 \max} + t_{f \max}) f$ where $f = \frac{1}{T}$

So the worst case for d_{\min} is at the highest fre-

quency used in the monitor :

$$d_{\min} = f_{\max} (t_{1 \max} + t_{f \max}) \quad (1)$$

t_f is usually well know by the designer ; shortening t_f is limited by the switching transistor T_1 breakdown voltage.

t_1 is the delay between the command for switching off the line transistor T_1 and its actual switching.

In diagram 1 and 2, t_1 is the recovery time t_{r1} of T_1 In diagram 3, t_1 is the recovery time t_{r1} of T_1 added to the turn on time t_{o2} of transistor T_2 .

So :

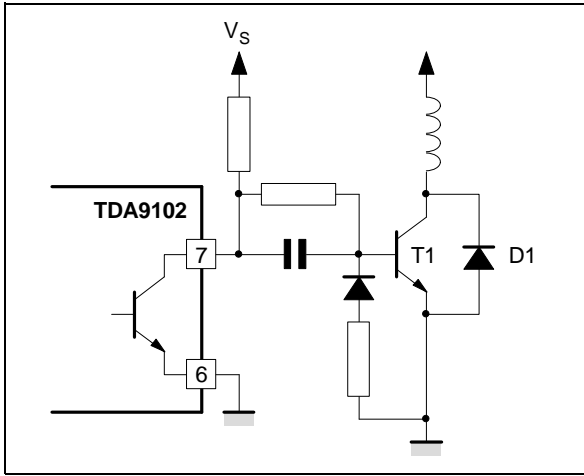
$$d_{\min} = f_{\max} (t_{r1 \max} + t_{f \max}) \quad (2)$$

for diagram 1 and 2

$$d_{\min} = f_{\max} (t_{r1 \max} + t_{o2 \max} + t_{f \max}) \quad (3)$$

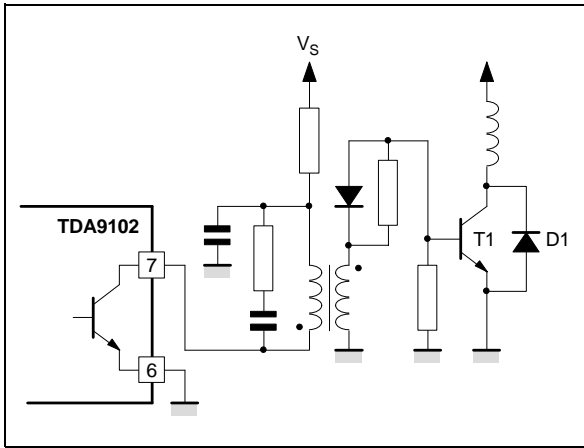
for diagram 3

Diagram 1 : Direct Drive



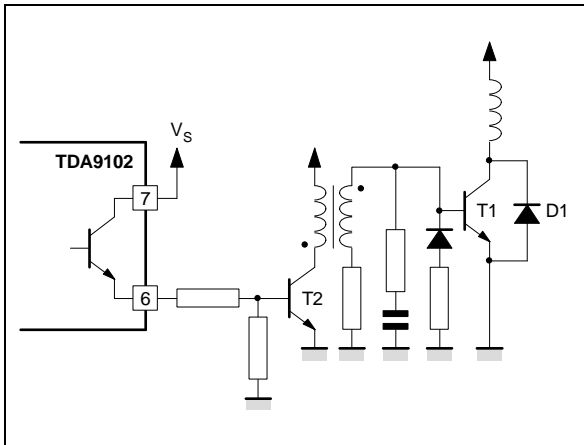
9102007.EPS

Diagram 2 : Transformer Drive



9102008.EPS

Diagram 3 : Indirect Drive



9102009.EPS

II.2. Duty Max.

Referring to Fig 1, the line switching transistor T₁ must be turned on before t₄, that is to say before the current becomes positive.

Since it takes a time t₀ for T₁ to turn on, the command, that is to say the positive going edge of Pin 7 must arrive at a time t₃ < t₄ - t₀.

t₄ would be in the middle of the trace time, at $\frac{t_2 + t_6}{2}$, if no energy was lost.

Since the negative part of the current (from t₂ to $\frac{t_2 + t_6}{2}$) is giving energy back to the power supply

while the positive part is drawing energy from it, the latter must be greater. The consequence is that t₄ arrives before the first half of the trace time, say at

$$t_4 = t_2 + \frac{k}{2} (t_6 - t_2)$$

$$t_4 = t_2 + \frac{k}{2} (T - t_f)$$

k < 1 is an inefficiency factor.

This sets the maximum allowable off time t₃ to :

$$t_{d \max} = t_{3 \max} = \left(t_1 + t_f + \frac{k}{2} + (T - t_f) - t_{0 \min} \right)_{\min}$$

Since the duty cycle is $d = \frac{t_d}{T} = f t_d$

$$d_{\max} = \frac{k}{2} + \left(f \left[t_1 + t_f \left(1 - \frac{k}{2} \right) - t_{0 \min} \right] \right)_{\min} \quad (4)$$

For applications 1 and 2, t₁ = t_r (T₁ turn-off time), t₀ = t₀₁ (T₁ turn-on time)

Since for any transistor t_r > t₀ and since k ≤ 1, the coefficient of f is always positive.

Therefore, the worst cas is :

$$d_{\max} = \frac{k}{2} + f_{\min} \left[t_{r1 \min} + t_{f \min} \left(1 - \frac{k}{2} \right) - t_{01 \max} \right] \quad (5)$$

for applications 1 and 2

For application 3, t_r = t_{r1} + t₀₂ (T₁ turn-off time + T₂ turn-on time) and t₀ = t₀₁ + t_{r2} (T₁ turn-on time + T₂ turn-off time)

Normally T₁ is a larger transistor working at a higher current than T₂ so that t_{r1} + t₀₂ > t₀₁ + t_{r2} and the coefficient of f in (4) is positive.

TDA9102C SELECTION vs HORIZONTAL DUTY CYCLE

In this case :

$$d_{\max} = \frac{k}{2} + f_{\min} \left[t_{r1 \min} + t_{o2 \min} + t_f \min \left(1 - \frac{k}{2} \right) - t_{o1 \max} - t_{r2 \max} \right]_{\min} \quad (6)$$

for application 3

However is T_2 is a very cheap transistor versus T_1 , the said coefficient may be negative ; in this case :

$$d_{\max} = \frac{k}{2} - f_{\max} \left[t_{o1 \max} + t_{r2 \max} - t_f \min \left(1 - \frac{k}{2} \right) - t_{r1 \min} - t_{o2 \min} \right]_{\min} \quad (7)$$

for application 3 with $t_{r1} + t_{o2} + t_f \left(1 - \frac{k}{2} \right) - t_{o1} - t_{r2} < 0$

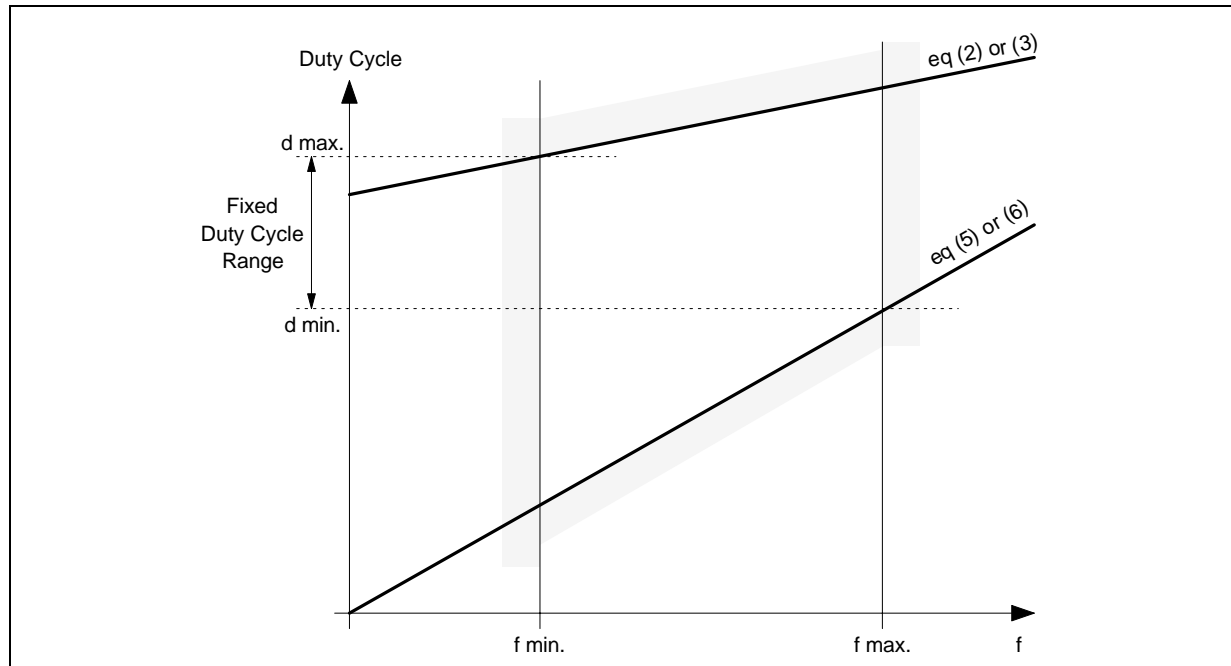
Note that in the general case d_{\max} worst case is $\frac{k}{2}$.

This shows that for high frequency application, where equations (2) and (3) show that the duty cycle can not be too small, k needs to be as high as possible. This is why it can be interesting to derive the EHT power from a system independant from the deflection one, even for a single frequency terminal.

II.3. Typical Limits

Using (2) or (3) and (5) or (6), the allowable limits can be drawn as in Fig 2 :

Figure 2



Example :

using diagram 1, with

$t_{r1} = 2\mu s \pm 0.5\mu s$, $t_{o1} = 0.5\mu s$, $f_{\min} = 31.5\text{kHz}$, $f_{\max} = 56\text{kHz}$, $k = 0.95$, $t_f = 2\mu s \pm 0.2\mu s$

yields to :

$$(2) : d_{\min} = 56 \times 10^3 \times (2.5 + 2.2) \times 10^{-6} = 0.26 \text{ (26 \%)}$$

$$(5) : d_{\max} = \frac{0.95}{2} + 31.5 \times 10^3 \left[2 + 1.8 \times \left(1 - \frac{0.95}{2} \right) - 0.5 \right] \times 10^{-6} = 0.53 \text{ (53 \%)}$$

In this case, TDA9102C (35 to 44 %) can be used. At 78kHz dmin would be 36.2 %. Thus TDA9102C would still fit the application.

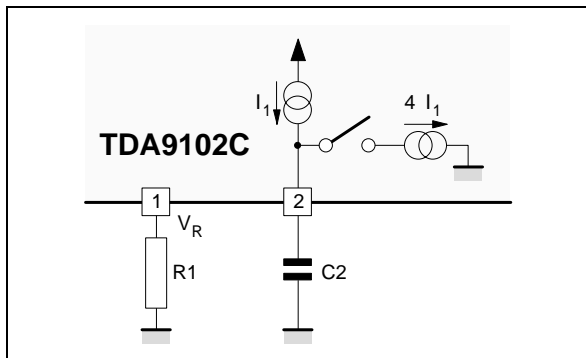
In such applications where it looks safer to center the selected device duty cycle in the allowable duty cycle range, paragraphs III and IV show a way to increase (resp. decrease) the duty cycle of a TDA9102C.

III. APPLICATION DIAGRAM FOR INCREASING THE DUTY CYCLE OF A TDA9102C

This application is needed when the minimum duty cycle of the selected TDA 9102C can be lower than the minimum allowable duty cycle of the application. The latter being proportionnal to f max, the calculations must be done at this max frequency.

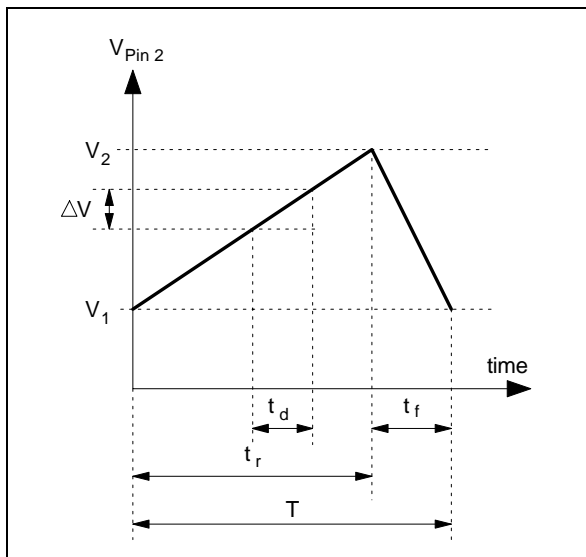
III.1. Standard application

Figure 3



9102011.EPS

Figure 4



9102012.EPS

During rise time tr, a current I1, is charging C2. This current is the image of the current driven from Pin 1 by R1 :

$$I_1 = \frac{V_R}{2R_1}$$

When the voltage on pin 2 reaches a threshold V2, a switch is activated so that the capacitor C2 is discharged by a current 4I1 - I1 = 3I1. The fall time tf ends when the threshold value V1 is reached.

Thus :

$$T_r = 2 \frac{V_2 - V_1}{V_R} R_1 C_2$$

$$T_f = 2 \frac{V_2 - V_1}{V_R} \frac{R_1 C_2}{3}$$

$$T = \frac{8}{3} \frac{V_2 - V_1}{V_R} R_1 C_2 \quad (8)$$

The off time td is used to define the duty cycle as :

$$\text{duty cycle} = \frac{t_d}{T}$$

The off time is the time during which Pin 7 is low. ΔV is a fixed voltage difference which determines td.

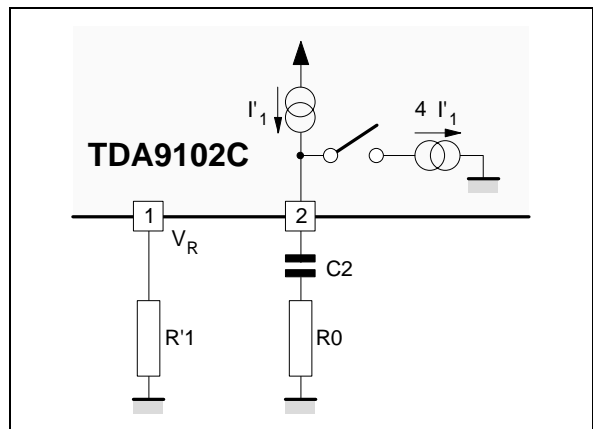
$$t_d = \frac{2\Delta V}{V_R} R_1 C_2 \quad (9)$$

Mixing (8) and (9) yields to :

$$\Delta V = \frac{t_d}{T} \frac{4}{3} (V_2 - V_1) \quad (9')$$

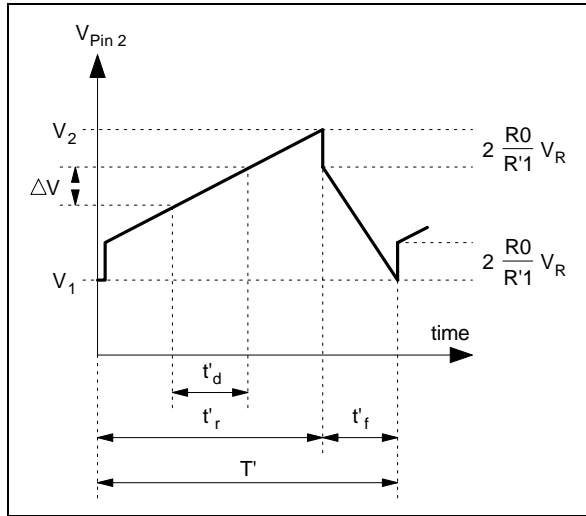
III.1.1. Modified Application

Figure 5



9102013.EPS

Figure 6



During rise time, a constant voltage drop $I_1 R_0$ is added to the voltage across C_2 . During fall time, $-3I_1 R_0$ is added.

Thus the voltage step is $4I_1 R_0 = 2 R_0 \frac{V_R}{R_1}$

The new period can be derived from formula (8), provided the voltage threshold difference $V_2 - V_1$ is decreased by $2 R_0 \frac{V_R}{R_1}$

Hence :

$$T' = \frac{8}{3} \frac{V_2 - V_1 - 2 \frac{R_0}{R_1} V_R}{V_R} R_1 C_2 \quad (10)$$

The off time t_d is straight forward :

$$t_d = \frac{2\Delta V}{V_R} R_1 C_2 \quad (11)$$

III.1.2. Components Calculation in Modified Application

III.1.2.1. R_1 CALCULATION

C_2 is assumed to be constant.

Equation (II) shows that fixing a duty cycle, or an off time t_d yields to a mandatory R_1 . Then equation (10) gives the adequate R_0 value for the given frequency. However the datasheet does not provide ΔV value, but provides $\frac{t_d}{T}$ in standard application (see formula (9)).

Introducing these known parameters in equation (II) yields to :

$$t_d = \frac{8}{3} \frac{(V_2 - V_1)}{V_R} \frac{t_d}{T} R_1 C_2 \quad (12)$$

$$R_1 = \frac{3}{8} \frac{t_d}{C_2} \frac{V_R}{(V_2 - V_1)} \frac{T}{t_d} \quad (13)$$

$\frac{t_d}{T}$: device duty cycle, t_d : needed off time

III.1.2.2. R_0 CALCULATION

Using (10) :

$$\frac{3}{8} T' \frac{V_R}{R_1 C_2} = V_2 - V_1 - 2 \frac{R_0}{R_1} V_R$$

$$2 \frac{R_0}{R_1} V_R = V_2 - V_1 - \frac{3T'}{8} \frac{V_R}{R_1 C_2}$$

$$R_0 = \frac{V_2 - V_1}{V_R} \frac{R_1}{2} - \frac{3T'}{16C_2}$$

(Replacing R_1 by (13))

$$R_0 = \frac{3T'}{16C_2} \left(\frac{d'}{d} - 1 \right) \quad (14)$$

III.1.3. Summary

When the minimum duty cycle $\frac{t_d}{T}$ of your application is higher than the minimum duty cycle $\frac{t_d}{T}$ of the chosen device, use the modified application of Fig.5, calculating R_1 from (13) and R_0 from (14). Chose the actual values for R_0 and R_1 , so that a safety margin is allowed for component tolerances.

IV. APPLICATION DIAGRAM FOR DECREASING THE DUTY CYCLE

This application is used when the max duty cycle of TDA9102C can be higher than the max allowable duty cycle of the application. The latter being proportional to f_{max} , the calculation is to be made at f_{min} .

IV.1. Standard Application : please refer to § III

$$T = \frac{8}{3} \frac{V_2 - V_1}{V_R} R_1 C_2 \quad (8)$$

$$t_d = \frac{2\Delta V}{V_R} R_1 C_2 \quad (9)$$

$$\Delta V = \frac{t_d}{T} \frac{4}{3} (V_2 - V_1) \quad (9')$$

IV.1.1. Modified Application

Figure 7

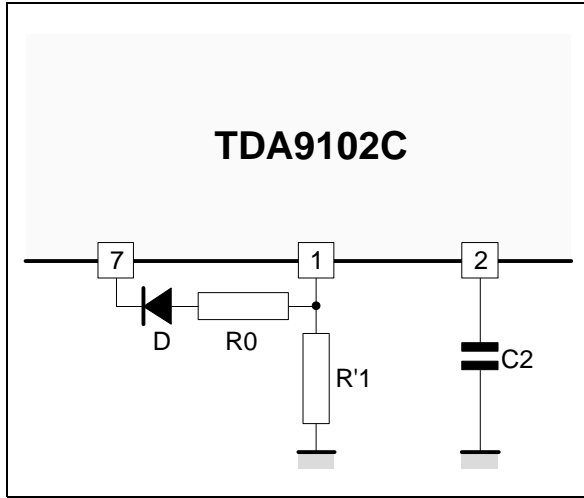
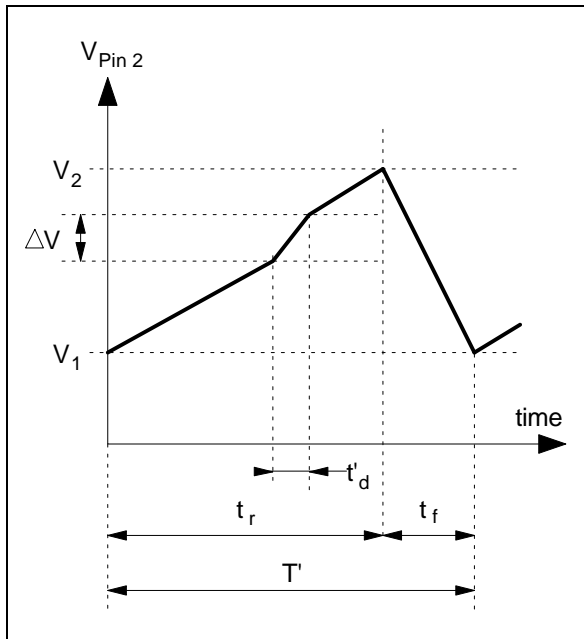


Figure 8



When the off time t'd starts, pin 7 is low so that R0 drives an additional current from pin 1, thus increasing the slope on C2.

If VD is the sum of the saturation voltage on pin 7 and the voltage drop across the diode D, the additional current is : $I_0 = \frac{V_R - V_D}{R_0}$

Since the current charging C2 is half the current driven from pin 1, the off time is :

$$t_d = \frac{2\Delta V C_2}{\frac{V_R}{R_1} + \frac{V_R - V_D}{R_0}} \quad (15)$$

using (9') :

$$t_d = \frac{8}{3} \frac{t_d}{T} \frac{(V_2 - V_1) C_2}{\frac{V_R}{R_1} + \frac{V_R - V_D}{R_0}} \quad (16)$$

IV.1.2 Component Calculation of the Modified Application (Fig.5)

definitions :

- td : device off time (normal application)
- $d = \frac{t_d}{T}$: device duty cycle
- t'd : needed off time (modified application)
- T' : line period (modified application)
- $d' = \frac{t'_d}{T'}$: needed duty cycle
- $V_S = V_2 - V_1$: voltage swing at pin 2 (4V)
- VR : voltage at pin 1 (3.5V)
- $V'_R = V_R - V_D$: voltage across R0 during off time (≈ 2.5V)

(16) can be rewritten as :

$$t_d = \frac{8}{3} \frac{d V_S C_2}{\frac{V_R}{R_1} + \frac{V'_R}{R_0}} \quad (17)$$

and (9') as (9'') $\Delta V = \frac{4}{3} d V_S$

a second equation is necessary to derive both R'1 and R0.

It is given by calculating the line period T' :

Referring to Fig.6 :

$$T' = (t_r - t'_d) + t'_d + t_f = \frac{V_S - \Delta V}{\frac{V_R}{2R_1}} C_2 + \frac{8}{3} \frac{d V_S C_2}{\frac{V_R}{R_1} + \frac{V'_R}{R_0}} + \frac{V_S C_2}{\frac{3}{2} \frac{V_R}{R_1}}$$

TDA9102C SELECTION vs HORIZONTAL DUTY CYCLE

$$\begin{aligned}
 (9') \Rightarrow T' &= \frac{2 R'_1}{V_R} \left(C_2 V_S - \frac{4}{3} d V_S C_2 + \frac{4}{3} \frac{d V_S C_2}{1 + \frac{V'_R R'_1}{V_R R_0}} + \frac{C_2 V_S}{3} \right) \\
 &= \frac{8}{3} \frac{V_S}{V_R} R'_1 C_2 \left(1 - d + \frac{d}{1 + \frac{V'_R R'_1}{V_R R_0}} \right) \\
 &= \frac{8}{3} \frac{V_S C_2}{\frac{V_R}{R'_1} + \frac{V'_R}{R_0}} \left(1 - d + (1 - d) \frac{V'_R R'_1}{V_R R_0} + d \right)
 \end{aligned}$$

$$(17) \Rightarrow T' = \frac{t'_d}{d} \left(1 + (1 - d) \frac{V'_R R'_1}{V_R R_0} \right)$$

$$\frac{T' d}{t'_d} = 1 + (1 - d) \frac{V'_R R'_1}{V_R R_0}$$

$$\frac{d}{d'} - 1 = (1 - d) \frac{V'_R R'_1}{V_R R_0}$$

$$\frac{V'_R}{R_0} = \frac{V_R}{R'_1} \frac{d - d'}{d' (1 - d)} \quad (18)$$

replacing in (17) :

$$\begin{aligned}
 t'_d &= \frac{8}{3} \frac{d V_S C_2}{\frac{V_R}{R'_1} \left(1 + \frac{d - d'}{d' (1 - d)} \right)} \\
 &= \frac{8}{3} \frac{V_S C_2 R'_1 d' (1 - d)}{V_R (1 - d')}
 \end{aligned}$$

$$R'_1 = \frac{3}{8} \frac{t'_d (1 - d') V_R}{C_2 d' (1 - d) V_S} \quad (19)$$

$$\text{as } d' = \frac{t'_d}{T'}$$

$$R'_1 = \frac{3}{8} \frac{T' (1 - d') V_R}{C_2 (1 - d) V_S} \quad (20)$$

using (18) :

$$R_0 = R'_1 \frac{d' (1 - d) V'_R}{(d - d') V_R}$$

$$R_0 = \frac{3}{8} \frac{T' (1 - d') d' V'_R}{C_2 (d - d') V_S} \quad (21)$$

V. CONCLUSION

If your maximum allowable duty cycle d' is lower than the max duty cycle d of the TDA9102C use application of Fig.5, calculating R'_1 and R_0 from (20) and (21).

The TDA9102C can be used in virtually all monitor application even though the horizontal duty cycle is basically fixed.

This together with the very good jitter figure and all DC control explains the great success of this device.

Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No licence is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

Purchase of I²C Components of SGS-THOMSON Microelectronics, conveys a license under the Philips I²C Patent. Rights to use these components in a I²C system, is granted provided that the system conforms to the I²C Standard Specifications as defined by Philips.

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - China - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco
The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.