

AN5306NFBS

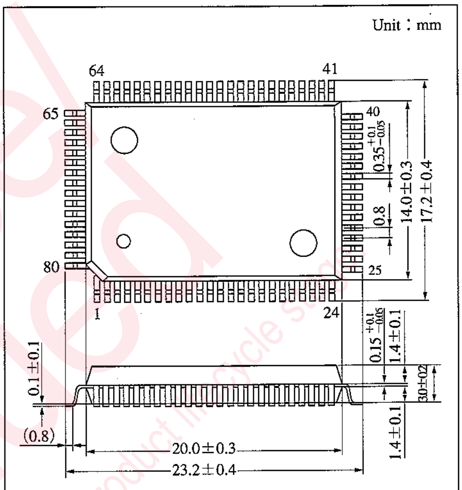
NTSC Video Signal Processor IC

■ Overview

The AN5306NFBS is used to process video, chroma, RGB, synchronization, and deflection signals. It incorporates an IIC bus controller.

■ Features

- Video : Wide bandwidth filter, adjustable preshoot and overshoot for contour enhancement, ABL input
- Chroma : ACC filter, color difference signal output
- RGB : Color difference signal input, RGB signal output
- Synchronization : Synchronous BLK input/output, adjustable AFC1 time-constant, adjustable horizontal position
- Deflection : Generation of parabola waves and saw-tooth waves, distortion correction



80-Pin QFH Package (QFH080-P-1420)

■ Absolute Maximum Ratings

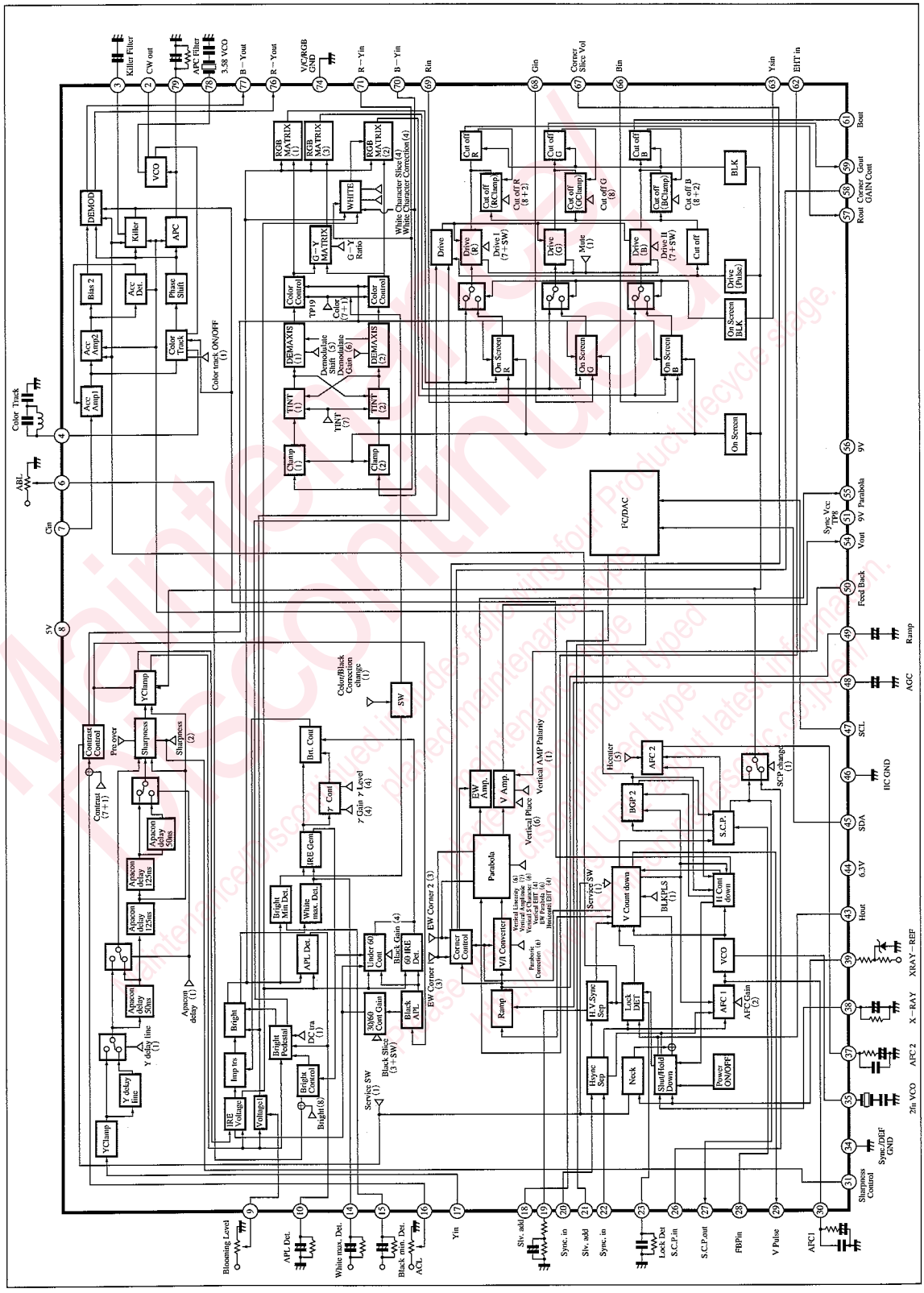
Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	V_{CC1}=9.6	V
		V_{CC2}=5.6	
Supply current	I_{CC}	$I_{CC1(+I51)}$=113	mA
		$I_{CC2(18)}$=89	
		I_{44}=26	
Power dissipation Note 2)	P_D	947	mW
Operating ambient temperature Note 1)	T_{opr}	−20 to +70	℃
Storage temperature Note 1)	T_{stg}	−55 to +150	℃

Note 1) Ta=25℃ except operating ambient temperature and storage temperature.
Note 2) Allowable power dissipation of the package at Ta=70℃.

■ Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Range
Operating supply voltage range	V_{CC1} $V_{56-34, 46, 74}$	8.5V to 9.0V to 9.5V
	V_{CC2} $V_{8-34, 46, 74}$	4.5V to 5.0V to 5.5V
Operating supply current range	I_{44}	15mA to 20mA to 25mA

■ Block Diagram



■ Electrical Characteristics (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
DC Characteristics						
Circuit current	I_{56+51}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	74	90	106	mA
Circuit current	I_8	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	59	71	83	mA
Synchronous input pin voltage	V_{20-34}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	0.8	1.3	1.8	V
Synchronous input pin voltage	V_{22-34}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	0.8	1.3	1.8	V
Video input pin voltage	V_{43-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.7	3.2	3.7	V
ABL input pin voltage	V_{6-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.5	3.0	3.5	V
ACL input pin voltage	V_{16-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.5	3.0	3.5	V
Blooming level pin voltage	V_{9-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.2	2.7	3.2	V
Chroma input pin voltage	V_{7-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	1.5	2.0	2.5	V
B−Y output pin voltage	V_{77-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.3	2.8	3.3	V
R−Y output pin voltage	V_{76-74}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	2.3	2.8	3.3	V
Horizontal Signal Processing						
Horizontal stabilized supply voltage	HV_{CC}	Pin㊹ is connected to 12V via 380Ω. V_{CC1} : 9V, V_{CC2} : 5V	5.9	6.3	6.7	V
Constant current source operation resistance	RHV_{CC}	I_{44} · 15 to 25mA	—	—	30	Ω
Horizontal free-run frequency (1)	f_{HO-1}		15.45	15.75	16.05	kHz
Horizontal free-run frequency (2)	f_{HO-2}	At Hold Down	16.3	16.4	16.8	kHz
f_{HO} supply rising drift	Δf_{HO} V_{CC3}	f_{HO} frequency difference when other supply OFF→ON	0	100	200	Hz
Horizontal output pulse duty	τ_{HO}	Hold down off	34.4	37.5	40.6	%
Horizontal output starting voltage	$V_{fH(S)}$	When f=10k to 20kHz and horizontal oscillation output is more than $1V_{P-P}$	—	—	5.2	V
Horizontal output level	V_{fH}		2.4	2.9	3.4	V
Horizontal pull-in range	f_{PH}	f_{HO}=15.75kHz	±400	—	—	Hz
H center variable range (1)	T_{DH}	Phase lead of 1A[10]→[00]*	1.8	2.5	3.2	μs
H center variable range (2)	T_{DH}	Phase lead of 1A[10]→[1F]*	−3.0	−2.3	−1.6	μs
Lock detector output voltage (1)	V_{23-M}	Synchronous	5.1	5.8	6.5	V
Lock detector output voltage (2)	V_{23-L}	Asynchronous	−0.1	0	0.5	V
Lock detector output voltage (3)	V_{23-T}	Hold-down	7.6	8.3	9.0	V
Hold-down operation voltage	V_{Hth}		2.5	2.8	3.1	V
Burst gate pulse width	T_{BGP}	Sandcastle output	1.8	2.5	3.2	μs
Sandcastle pulse output level (BGP)	V_{BGP}	V_{CC} : typ.	4.0	4.3	4.6	V
Sandcastle pulse output level (HBLK)	V_{HBLK}	V_{CC} : typ.	2.7	3	3.3	V
Sandcastle pulse output level (VBLK)	V_{VBLK}	V_{CC} : typ.	1.2	1.5	1.8	V
Vertical Signal Processing						
Vertical output pulse width	τ_{VO}		360	380	400	μs

* Refer to table 1

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Vertical output level	V_{29}		1.3	1.8	2.3	V
Vertical output free-run frequency	f_{VO}		58.8	60	61.2	Hz
Vertical blanking pulse width	τ_{VBLK}		1.37	1.4	1.43	ms
Y Signal Processing						
Video voltage gain	AY_G	Cont : max. Sharp : min.	17	20	23	dB
Video voltage gain relative ratio	AY	Ratio between RGB channels drive ; typ.	−2.5	0	2.5	dB
Video voltage gain relative ratio DL	AY_{Gd1}	Y delay line ON/OFF	−1.5	0	1.5	dB
Sharpness 1	$AG_{(SH)2}$	f=4MHz sharpness : φφ→7F aper.−con. SW : 250n	11.5	14.5	17.5	dB
Sharpness 2	$AG_{(SH)2}$	f=3MHz sharp : φφ→7F aper.−con. SW : 300n	11.5	14.5	17.5	dB
Contrast control range max.	$AG_{(CON)}$	Sharp : min. Cont : typ.	3.5	6	8.5	dB
Contrast control min. value	$yG_{(CON)}$ min.	Contrast : min.	—	30	200	mV
Brightness variable quantity	V_{BR}	No input Bright : min.→max.	3.0	3.7	4.4	V
DC regeneration rate 1	TDC1	APL10→90% DC transmission quantity change-over : −direction	90	96	102	%
DC regeneration rate 2	TDC2	APL10→90% DC transmission quantity change-over : +direction	96	103	110	%
Y signal delay time 1	t_{DL1}	Y delay line : ON	260	325	390	ns
Y signal delay time 2	t_{DL2}	Y delay line : OFF	160	205	250	ns
Y frequency characteristics 1	Δy_1 (Y)	10MHz attenuation quantity DL for f=3MHz : ON	−6	−3	+1	dB
Y frequency characteristics 2	Δy_2 (Y)	10MHz attenuation quantity DL for f=3MHz : OFF	−5	−2	+2	dB
ACL characteristics	ΔyACL	Pin⑯ 3V→3.5V	8	11	14	dB/V
ABL characteristics	ΔY_{ABL}	Pin⑥ 2.7→3.5V	2.7	3.4	4.1	V/V
Black extension quantity	ΔYBL1	Input : full black Pin⑮ : 3V CR filter	−0.1	0	0.1	V
Black extension gain	ΔYBL2	Input : full black Pin⑮ : 3V Black gain : min.→max.	1.6	1.95	2.3	V
Black extension start point 1	ΔYBL3	Pin⑮ : 5V after 2.4V_{P-P} by contrast Pin⑮ CR filter	−0.12	0	0.12	V
Black extension start point 2	ΔYBL4	Black level : min. after 1.7V_{P-P} by drive Black level : max.	−0.1	0.35	0.8	V
γ correction quantity min. to max.	Y_γ	White γ gain : max. White γ level : min. to max.	0.5	0.85	1.2	V
Blooming level drift quantity	ΔYBLM	Blooming DC Pin⑨ : 0.5V→4.5V	3.2	3.9	4.6	V
Pedestal level (standard)	Y_G	Cut−off : 80	2.0	2.4	2.8	V
Chroma Signal Processing						
ACC characteristics 1	ACC1	Color bar signal (burst 300mV_{P-P})	−1	0	+1	dB
ACC characteristics 2	ACC2	Color bar signal (burst 15mV_{P-P})	−4	−1.5	+1	dB
Killer tolerance on	e_k	Color bar burst 0dB=150mV_{P-P}	−48	−43	−38	dB

ICs for TV

■ Electrical Characteristics (cont.) (Ta=25±2℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Killer tolerance off	e_k	Color bar signal. (Burst 0dB=150mV_{P-P})	−44	—	—	dB
Demodulation output amplitude B−Y	e_{OB}	Color bar signal. (Burst 150mV_{P-P})	0.85	1.25	1.64	V_{P-P}
Demodulation output amplitude R−Y	e_{OR}	Color bar signal. (Burst 150mV_{P-P})	0.67	1.0	1.32	V_{P-P}
Demodulation output ratio	R/B	Rainbow signal R−Y/B−Y output ratio	0.48	0.56	0.64	times
Demodulation angle B−Y	∠B		−8	−2.5	3	deg.
Demodulation angle R−Y	∠R		83	88	93	deg.
Color residue	e_{killer}	Killer filter terminal grounded by 20kΩ	—	—	50	mV_{P-P}
Demodulation output residual carrier	e_{car}	No signal input	—	—	50	mV_{P-P}
APC pull-in range Low	f_{pull}	Burst frequency change	500	600	—	Hz
APC pull-in range High	f_{pull}	Burst frequency change	−500	−600	—	Hz
CW output amplitude	e_{cw}		600	800	1100	mV_{P-P}
Free-run frequency	f_{co}	Deviation from 3.579545MHz	−200	0	200	Hz
RGB Signal Processing						
Tint center *	θ_t	Pin⑦1 356mV_{P-P} Pin⑦0 200mV_{P-P}, DAC value where R.B output coincident	[3F]**	[4C]**	[5C]**	—
Tint variable range max. *	$\Delta\theta_1$	Tint : typ.→max.	25	35	—	deg.
Tint variable range min. *	$\Delta\theta_2$	Tint : typ.→min.	−32	−42	—	deg.
R−Y demodulation axis variable range *	$\Delta\theta_{Dem}$	Demodulation axis : min.→max.	16	28	39	deg.
B−Y ratio variable range (1) *	AB−Ymin.	Demodulation ratio : typ.→min.	—	0	0.25	times
B−Y ratio variable range (2) *	AB−Ymin.	Demodulation ratio : typ.→min.	1.25	1.5	1.75	times
G−Y/R−Y ratio (1) *	e_G/e_{R2}	G−Y ratio change-over : 02	0.29	0.36	0.43	times
G−Y/R−Y ratio (2) *	e_G/e_{R3}	G−Y ratio change-over : 03	0.27	0.35	0.44	times
G−Y/B−Y ratio (1) *	e_G/e_{B2}	G−Y ratio change-over : 02	0.15	0.23	0.31	times
G−Y/B−Y ratio (2) *	e_G/e_{B3}	G−Y ratio change-over : 03	0.3	0.36	0.42	times
RGB output blanking voltage	E_{BLK}	Bright : typ. cut-off	0.7	1.1	1.5	V
Color control range max. *	A_{B-Y}cl max.	Cont : typ. Color : typ.→max.	3.4	5.0	6.6	dB
Color control min. value *	A_{B-Y}cl min.	Cont : typ. Color : typ.→min.	—	25	50	mV
Color difference contrast variable range *	$A_{B\,(CON)}$	Color : typ. Cont : typ.	3.5	6	8.5	dB
Drive control range	$A_{R\,(DR)}$	Drive SW : 00→04 Drive : min.→max.	4	6	8	dB
Cut-off R・B control range	$V_{(CO)}$	Cut-off SW Cut-off : min.→max.	1.6	2.1	2.6	V
Cut-off G control range	$V_{(CO)\,G}$	Cut-off : min.→max.	0.6	1.1	1.6	V
On-screen voltage gain	A_{yG}	Y_S=1V Contrast : max.	8	10	12	dB
On-screen contrast range	$A_{yG\,(ON)}$	Y_S=1V typ.→max.	0	1.5	3.5	dB
On-screen contrast min. value	$A_{yG\,(ON)}$ min.	0.5V input	0.1	0.3	0.5	V_{P-P}
On-screen frequency characteristics	Δe	Attenuation quantity of f=10MHz to f=3MHz	−6	−3	+1	dB
Deflection Signal Processing						
Standard vertical sawtooth output amplitude	V_{out}	Pin⑤0, ⑤4 short	2.2	2.6	3.0	V_{P-P}
Standard EW parabola output amplitude	V_{EW}		1.8	2.2	2.6	V_{P-P}

* The state in which R, B output amplitudes and G amplitude are made coincident, by means of drive I, II adjustments when Y signal is applied to Pin⑰.
** Refer to table 1

■ Electrical Characteristics (Ta=25±2℃) [Reference Value]

Parameter	Symbol	Condition	min	typ	max	Unit
Horizontal Signal Processing						
Synchronous separable input	V_{IN}	Input ; full black Sync. level	(0.2)	(1.0)	—	V_{P-P}
f_{HO} ambient temperature dependency	$\frac{\Delta f_{HO}}{Ta}$	Ta=−20 to +70℃	—	(5.5)	—	Hz/℃
Horizontal oscillation frequency control sensitivity	β_H		—	(1.2)	—	Hz/mV
AFC1 reference current (1)	$I_{30(1)}$	0D [30]*	—	(0.83)	—	mA
AFC1 reference current (2)	$I_{30(2)}$	0D [20]*	—	(1.33)	—	mA
AFC1 reference current (3)	$I_{30(3)}$	0D [10]*	—	(1.83)	—	mA
AFC1 reference current (4)	$I_{30(4)}$	0D [00]*	—	(2.33)	—	mA
F.B.P slice level (blanking)	V_{FBP-1}		—	(0.7)	—	V
F.B.P slice level (AFCI)	V_{FBP-2}		—	(2.5)	—	V
F.B.P delay time range	T_{H-FBP}	H center ; Typ. Hout rise to FBP center	—	—	(19)	μs
B.G.P start position	—	Horizontal Sync. rear edge to burst gate pulse front edge	—	(0.3)	—	μs
Sandcastle pulse output temperature characteristics	$\Delta V_{27\,(Ta)}$		—	(1.8)	—	mV/deg
Sandcastle pulse input thresh level temperature characteristics	$\Delta V_{26\,(Ta)}$		—	(0)	—	mV/deg
FBP input threshold level temperature characteristics HBLK	$\Delta V_{28\,(Ta)}$		—	(−1.8)	—	mV/deg
FBP input threshold level temperature characteristics AFC1	—		—	(1)	—	mV/deg
X−ray inner reference temperature characteristics	—	Zener temperature characteristics+1.8mV/deg	—	(0)	—	mV/deg
Sandcastle pulse output supply voltage dependency BGP	—	V_{CC2} 5V±0.5V	—	(1)	—	V/V
Sandcastle pulse output supply voltage dependency HBLK	—	V_{CC2} 5V±0.5V	—	(0.74)	—	V/V
Sandcastle pulse output supply voltage dependency VBLK	—	V_{CC2} 5V±0.5V	—	(0.44)	—	V/V
Vertical Signal Processing						
Vertical BLK phase wide	PVBLK (W)	Period from VBLK rise to vertical Sync. fall	—	(3.87)	—	ms
Vertical BLK phase normal	PVBLK	Period from VBLK rise to vertical Sync. fall	—	(0.2)	—	ms
CRT neck break operation Pin㉗ voltage	V_{27}	Pin㊴ : 1.5V	(1.5)	—	—	V
Vertical BLK pulse width wide	TVBLK (W)		—	(5.05)	—	ms
Y Signal Processing						
Contrast variable range	$A_{yG(CON)}$ min.	Contrast : min./max.	—	(40)	—	dB
Y output amplitude V_{CC} dependency	Δy_G (V_{CC})		—	(0.4)	—	dB/V
Y output DC voltage V_{CC} dependency	ΔY_G (V_{CC})		—	(0.18)	—	V/V
Y noise level	V_{YNL}		—	(7)	(50)	mV
Delay line dynamic range	$V_{DLmax.}$		—	(0.7)	—	V
Y output amplitude ambient temperature dependency R	Δy_R (Ta)	−20 to +70℃	—	(−6)	—	%
Y output amplitude ambient temperature dependency G	Δy_G (Ta)	−20 to +70℃	—	(−8)	—	%
Y output amplitude ambient temperature dependency B	Δy_B (Ta)	−20 to +70℃	—	(−6)	—	%
APL detection voltage	A_{APL}	APL50→100%	(1)	(2)	(4)	times
Sharpness output voltage	V_{31}	Sharpness : typ.	(1.8)	(2.1)	(2.4)	V
Sharpness output variable range	ΔV_{31}	Shrapness : min.→max.	(2.7)	(3.0)	(3.3)	V

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.
* Refer to table 1

■ Electrical Characteristics (Ta=25±2℃) [Reference Value]

Parameter	Symbol	Condition	min	typ	max	Unit
Chroma Signal Processing						
Demodulation output amplitude V_{CC} dependency	e_{0-V}		—	(0)	—	dB/V
VCO V_{CC} dependency	Δf_{CO-V}		—	(220)	—	Hz/V
Burst-chroma ratio tolerance	Δe_0 (bst)	Burst compression tolerance for color bar chroma	—	(−40)	—	%
Demodulation output ambient temperature dependency R−Y	Δe_{R-Y} (Ta)	−20 to +70℃	—	(−3)	—	%
Demodulation output ambient temperature dependency B−Y	Δe_{B-Y} (Ta)	−20 to +70℃	—	(−3)	—	%
RGB Signal Processing						
Y→RGB crosstalk	e_{CT1}	Cross-hatch signal (Y input)	—	(−45)	—	dB
RGB→Y crosstalk	e_{CT2}	Cross-hatch signal (OSD input)	—	(−40)	—	dB
Color difference input dynamic range	$AV_{max.}$		—	(2.2)	—	V
Internal·external pedestal difference voltage	$\Delta E_{(YS)}$		(−100)	(0)	(100)	mV
OSD input dynamic range	$AV_{max.}$		—	(1.5)	—	V
RGB output amplitude V_{CC} dependency	Δe_G (V_{CC})	V_{CC1} 8.5 to 9.5V V_{CC2} 4.5 to 5.5V	—	(0.4)	—	V/V
OSD output amplitude V_{CC} dependency	Δe_g (V_{CC})	V_{CC1} 8.5 to 9.5V V_{CC2} 4.5 to 5.5V	—	(0)	—	V/V
RGB color difference signal amplitude temperature dependency	Δe_G (Ta)	−20 to +70℃	—	(20)	—	%
OSD output amplitude temperature dependency	Δe_g (Ta)	−20 to +70℃	—	(6)	—	%
Color control range (external)	Δe_{color}	0Ei [40]* To DAC Control ratio	—	(28)	—	%
White character slice level range	V_W	Blooming DC 2.5V Color difference no input	(0.6)	(0.8)	(1.0)	V
White character correction quantity	ΔV_W	Blooming DC 2.5V Color difference no input	(0.6)	(0.8)	(1.0)	V
Deflection Signal Processing						
Vertical amplitude variation ratio (1)	ΔV_{amp}	Vertical amplitude : typ.→max.	(10)	(19)	(28)	%
Vertical amplitude variation ratio (2)	ΔV_{amp}	Vertical amplitude : typ.→min.	(−10)	(−19)	(−28)	%
Vertical linearity variation width max.	ΔV_{lin}	Vertical linearity typ.→max.	(5)	(12)	(19)	%
Vertical linearity variation width min.	ΔV_{lin}	Vertical linearity typ.→min.	(−5)	(−12)	(−19)	%
Vertical S character amplitude variation ratio	ΔV_{SC}	Vertical S-correction : min.→max.	(−33)	(−18)	(−3)	%
Vertical position variation width	ΔV_{shift}	Vertical position : min.→max.	(0.6)	(0.8)	(1.0)	V
Vertical EHT amplitude variation ratio	ΔV_{EHT}	Pin㊷=0V Vertical EHT : typ.→max.	(3)	(10)	(19)	%
Vertical EHT amplitude variation ratio	ΔV_{EHT}	Pin㊷=1V Vertical EHT : typ.→min.	(−3)	(−10)	(−19)	%
EW parabola variation width	$\Delta V_{parabola}$	EW parabola amplitude : min.→max.	(2)	(3.2)	(4.4)	V_{P-P}
Horizontal amplitude variation width	$\Delta V_{H-WIDTH}$	Horizontal amplitude : min.→max.	(3.4)	(4.6)	(5.8)	V
Trapezoidal distortion correction variation ratio 1	ΔV_{Trapz}	Trapezoidal distortion correction : typ.→max.	(48)	(72)	(96)	%
Trapezoidal distortion correction variation ratio 2	ΔV_{Trapz}	Trapezoidal distortion correction : typ.→min.	(−48)	(−72)	(−96)	%
Corner correction variation ratio 1	ΔV_{corner}	EW corner 1 : min.→max.	(−40)	(−28)	(−16)	%
Corner correction variation ratio 2	ΔV_{corner}	EW corner 2 : min.→max.	(−38)	(−26)	(−14)	%
Horizontal EHT correction variable range	ΔV_{H-EHT}	Pin㊷=1V Horizontal EHT : min.→max.	(1.4)	(2.2)	(3.0)	V
Deflection Signal Processing						
Corner correction slice level pin voltage	V_{67}		—	(0.55)	—	V

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.
* Refer to table 1

■ Electrical Characteristics (cont.) (Ta = 25 ± 2℃) [Reference Value]

Parameter	Symbol	Condition	min	typ	max	Unit
Corner correction gain adjustment pin voltage	V_{57}		—	(2.5)	—	V
EW output V_{CC} drift	ΔV_{EW} (V_{CC})	V_{CC1} 8.5 to 9.5V V_{CC2} 4.5 to 5.5V	—	(0)	—	%
EW amp. drive current	$I_{EW}-dr$		—	(1.4)	—	mA
Ramp wave form normal	ΔV_{ramp}	0D [00]*	—	(2.5)	—	V_{P-P}
Ramp wave form wide	$\Delta V_{ramp(W)}$	0D [40]*	—	(2.5)	—	V_{P-P}
AGC input output current	I_{48}	Service SW : ON Pin㊾ sweep	—	(±140)	—	μA
Ramp input output current (1)	I_{49}	Pin㊽ : 1.5V, Pin㊾ : 2.5V Vpulse : ON	—	(4.4)	—	mA
Ramp input output current (2)	I_{49}	Pin㊽ : 1.5V, Pin㊾ : 2.5V Vpulse : OFF	—	(−90)	—	μA
DC level of vertical scan stop-mode	V_{49-SW}	0D [80]*	—	(1.2)	—	V
Input Signal						
Chroma input tolerant level	e_{Cin}	Color bar chroma 330mV_{P-P} burst level	(90)	(150)	—	mV_{P-P}
Y input tolerant level	y_{in}	Sync. to white 100%	—	(0.5)	(0.7)	V_{P-P}
H Sync. input tolerant level	v_{Hin}	Sync. to pedestal	(0.5)	(1.0)	(2.0)	V_{P-P}
V Sync. input tolerant level	v_{Vin}	Sync. to pedestal	(0.5)	(1.0)	(2.0)	V_{P-P}
Sandcastle pulse external input BGP	$V_{BGP\ in}$	V_{CC} : typ.	(4.0)	(4.3)	(4.6)	V_{P-P}
Sandcastle pulse external input HBLK	$V_{HBLK\ in}$	V_{CC} : typ.	(2.7)	(3.0)	(3.3)	V_{P-P}
Sandcastle pulse external input VBLK	$V_{VBLK\ in}$	V_{CC} : typ.	(1.2)	(1.6)	(1.8)	V_{P-P}
FBP input	$V_{FBP\ in}$	V_{CC} : typ.	—	—	(3.5)	V
Ys input level	V_{63}	V_{CC} : typ.	(2.0)	—	(3.5)	V
On-screen input R	e_{69}		—	(0.71)	(1.0)	V_{P-P}
On-screen input G	e_{68}		—	(0.71)	(1.0)	V_{P-P}
On-screen input B	e_{66}		—	(0.71)	(1.0)	V_{P-P}
I^2C bus SDA input level H	V_{45}	V_{CC2} (=5V)	(4.0)	—	(V_{CC2})	V
I^2C bus SDA input level L	V_{45}	V_{CC2} (=5V)	(0)	—	(0.7)	V
I^2C bus SCL input level H	V_{47}	V_{CC2} (=5V)	(4.0)	—	(V_{CC2})	V
I^2C bus SCL input level L	V_{47}	V_{CC2} (=5V)	(0)	—	(0.7)	V

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.
* Refer to table 1

Table 1 I²C Bus Protocol

(1) Slave address : 1 0 0 0 1 0 1 0

(2) Slave address format :

S	SLAVE ADDR	0	A	SUB ADDR	A	DATA BYTE	A	P
↑ Start condition		↑ Write	↑ Acknowledge bit					↑ Stop condition

AN5306N DAC CONTROL

No.	DAC name	bit number	Sub address	Data address	Remarks	Standard measurement condition
1	Color control	7+offSW	00 (00000000)	00 to 40 to 7F	DATA : Color OFF with [00]	40
2	Tint control	7	01 (00000001)	00 to 40 to 7F	———	40
3	Brightness control	8	02 (00000010)	00 to 80 to FF	———	80
4	Contrast control	7	03 (00000011)	00 to 40 to 7F	———	7F
5	Sharpness control	7	04 (00000100)	00 to 40 to 7F	———	00
6	Cut-off R	8 (+2SW)	05 (00000101)	00 to 80 to FF	4 stage change-over by SW	FF
7	Cut-off G	8	06 (00000110)	00 to 80 to FF	———	FF
8	Cut-off B	8 (+2SW)	07 (00000111)	00 to 80 to FF	4 stage change-over by SW	FF
9	Drive R	7 (+SW)	08 (00001000)	00 to 40 to 7F	2 stage change-over by SW	7F
10	Drive B	7 (+SW)	09 (00001001)	00 to 40 to 7F	2 stage change-over by SW	7F
11	Vertical amplitude	7	0A (00001010)	00 to 40 to 7F	———	40
12	EW parabola amplitude	6	0B (00001011)	00 to 20 to 3F	———	20
13	Horizontal amplitude	6	0C (00001100)	00 to 20 to 3F	———	20
14	Y delay line change-over	1	0D (00001101)	01 (00000001)	For [00] ON, for [01] OFF,	08
15	Aper,con. delay quantity change-over	1	0D (00001101)	02 (00000010)	For [00] 50ns, 250ns [02] 0ns, 300ns	
16	DC transmission quantity change-over	1	0D (00001101)	04 (00000100)	For [00] −direction, for [04] +direction	
17	Output blanking ON/OFF	1	0D (00001101)	08 (00001000)	For BLK pulse, [00] has [08] not	
18	AFC1 gain change-over	2	0D (00001101)	10, 20	With [30] → [00] AFC1μ increases	
19	BLK pulse width change-over	1	0D (00001101)	40 (01000000)	For [00] normal screen for [40] wide screen	
20	Service SW ON/OFF	1	0D (00001101)	80 (10000000)	For [00] normal state, for [60] def V output DC	
21	Sand castle pulse change-over	1	0E (00001110)	01 (00000001)	For [00] internal SCP, for [01] external SCP	00
22	Vertical amp. polarity change-over	1	0E (00001110)	02 (00000010)	For FB terminal polarity of def Vertical amp., −in [00], +in [02]	
23	Color track ON/OFF	1	0E (00001110)	04 (00000100)	For color truck, OFF in [00], ON in [04]	
24	Mute ON/OFF	1	0E (00001110)	10 (00010000)	For [00] normal state, for [10] RGB output OFF	
25	Sharpness ON/OFF	1	0E (00001110)	20 (00100000)	For sharpness, ON in [00], OFF in [20]	
26	Black detection/color change-over	1	0E (00001110)	40 (01000000)	For black detection pin, black detection in [00], color terminal in [40]	

Table 1 (cont.)

No.	DAC name	bit number	Sub address	Data address	Remarks	Standard measurement condisiton
27	Cut-off R switch-1	1	0F (00001111)	01 (00000001)	Cut-off R level increased with 〔00〕→〔01〕→〔02〕→〔03〕	11
28	Cut-off R switch-2	1	0F (00001111)	02 (00000010)		
29	Drive R switch	1	0F (00001111)	04 (00000100)	Drive R gain increased with 〔00〕→〔04〕	
30	Drive B switch	1	0F (00001111)	08 (00001000)	Drive B gain increases with 〔00〕→〔08〕	
31	Cut-off B switch-1	1	0F (00001111)	10 (00010000)	Cut-off B level increases with 〔00〕→〔10〕→〔20〕→〔30〕	
32	Cut-off B switch-2	1	0F (00001111)	20 (00100000)		
33	H blanking change-over	1	0F (00001111)	40 (01000000)	For chroma BGP, H-BLK with 〔00〕, BBP1 with 〔40〕	
34	Pre-shoot/over-shoot quantity	3	10 (00010000)	00 to 04 to 07	—	04
35	Black eextension gain	4	11 (00010001)	00 to 08 to 0F	—	00
36	White γ level	4	12 (00010010)	00 to 08 to 0F	—	08
37	White γ gain	4	13 (00010011)	00 to 08 to 0F	—	08
38	Black elongation slice position	3+offsw	14 (00010100)	00 to 04 to 07	For contrast, interlock with 〔00〕→〔07〕, independent with 〔03〕→〔0F〕	04
39	Demodulation axis R−Y	5	15 (00010101)	00 to 10 to 1F	—	00
40	Demodulation ratio B−Y	6	16 (00010110)	00 to 20 to 3F	—	20
41	G−Y ratio change-over	2	17 (00010111)	00 to 02 to 03	〔00〕,〔01〕: TYPE1 〔02〕: TYPE2 〔03〕: TYPE1	00
42	White character correction	4	18 (00011000)	00 to 08 to 0F	—	00
43	White character slice voltage	4	19 (00011001)	00 to 08 to 0F	—	00
44	H center position	5	1A (00011010)	00 to 10 to 1F	—	10
45	Vertical S-correction	6	1B (00011011)	00 to 20 to 3F	—	20
46	Vertical linearity	6	1C (00011100)	00 to 20 to 3F	—	20
47	Vertical position	6	1D (00011101)	00 to 20 to 3F	—	20
48	Trapezoidal correction	6	1E (00011110)	00 to 20 to 3F	—	20
49	EW corner 1	3	1F (00011111)	00 to 04 to 07	—	04
50	EW corner 2	3	20 (00100000)	00 to 04 to 07	—	04
51	Vertical EHT	4	21 (00100001)	00 to 08 to 0F	—	08
52	Horizontal EHT	4	22 (00100010)	00 to 08 to 0F	—	08

Note : DAC default value is center (eg : 〔80〕 in 8bit)
SW default value is 〔00〕
G−Y ratio change-over TYPE1 : G−Y=−0.34 (R−Y) −0.28 (B−Y)
TYPE2 : G−Y=−0.33 (R−Y) −0.17 (B−Y)

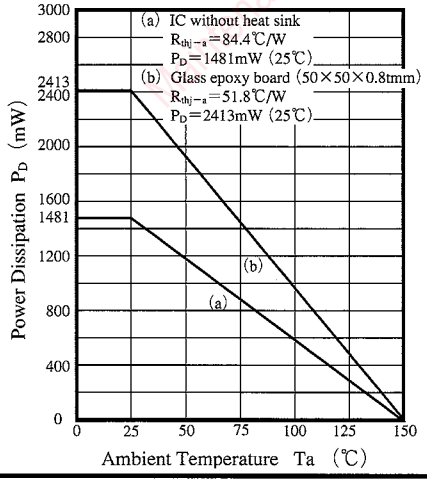
ICs for TV

■ Pin Descriptions

Pin No.	Pin name	Pin No.	Pin name
2	3.58MHz CW output	44	Hor. power supply (HV_{CC})
3	Killer filter	45	I^2C SDA input
4	Color track filter	46	I^2C GND
6	ABL input (Brightness control)	47	I^2C SCL input
7	Chroma input	48	Reference ramp waveform AGC filter
8	5V power supply (V_{CC2})	49	Reference ramp waveform generation
9	Blooming level input	50	Ver. deflection saw-tooth feedback input
10	Filter for APL detection	51	Sync. 9V power supply
14	Filter for white peak detection	54	Ver. deflection saw-tooth output
15	Black min. det. filter/color control	55	EW output
16	ACL input contrast control	56	9V power supply (V_{CC1})
17	Y signal input	57	R output
18	Slave address switching−1	58	Corner gain control
19	V sync. sep filter	59	G output
20	H sync. input	61	B output
21	Slave address switching−2	62	EHT voltage detection
22	V sync. input	63	Ys input
23	Lock det. filter	66	On-Screen B input
26	Sandcastle pulse input	67	Corner slice level control
27	Sandcastle pulse output	68	On-screen G input
28	Flyback pulse (FBP) input	69	On-screen R input
29	V pulse output	70	B−Y input
30	AFC1 filter	71	R−Y input
31	Sharpness control output	74	V/C/RGB GND
34	Sync. Def GND	76	R−Y output
35	503kHz VCO	77	B−Y output
37	ACF filter	78	3.58MHz VCO
38	High voltage det. input (X−ray)	79	Chroma APC filter
39	High voltage det. reference voltage	5, 11, 36, 42, 60, 75	No-connection
43	Hor. drive pulse output	1, 12, 13, 24, 25, 32, 33, 40	GND
—		41, 52, 53, 64, 65, 72, 73, 80	

■ Reference

P_D − Ta



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