



PULSE CONTROLLED INVERTER

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ABSTRACT

With the development of insulated gate transistors, interfacing digital control with a power inverter is becoming easier and less expensive.

This paper presents a new interface concept that takes advantage of digital based control to reduce the cost of the digital-to-power interface. The interface is greatly simplified by allowing the digital control to carry out a large part of the interface functions. This is one of the cheapest solutions available today and it has potential for further cost reduction.

A proposal for a Brushless DC Permanent Magnet motor drive is examined, although the technique can be easily applied to UPS or AC motor drives.

1. INTRODUCTION

Power MOSFETs and IGBTs, with their simple gate drive, make the design of DC/AC inverters relatively easy. For designers, the major problem is now to reduce the system cost while keeping the performance level high.

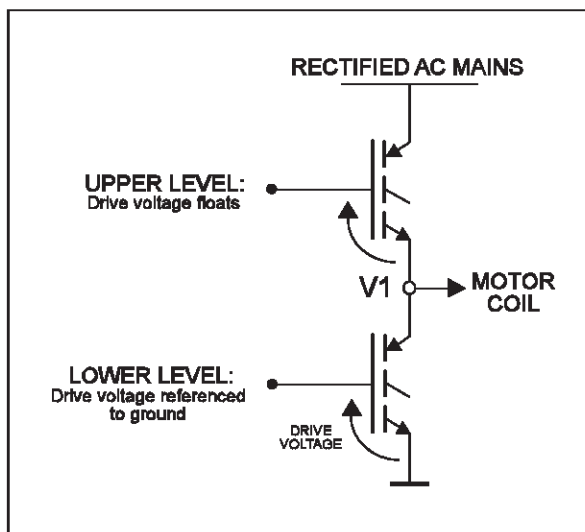
More difficult is the choice of the signal-power interface circuit from the variety of solutions available. For this type of circuit to be cost effective the design must use few components and cheap silicon technologies.

This paper proposes such an optimized interface based on a pulse control technique.

2. THE STATE OF THE ART

Digital controller based control circuits increasingly form the heart of high voltage/high frequency DC/AC inverters. As the cost of the interface is significant, keeping it to a minimum is a key issue. There are a number of methods of interfacing the controller to the power stage, which has a lower and an upper level - see figure 1.

Figure 1: Upper and lower levels of power stage



Generally the interface with the lower level is easy to design, as the gate-emitter/gate-drain drive voltage of the transistors is referenced to ground, as are the controller output voltages. However, upper level transistors are connected to the high side of the motor, and so their emitter/drain voltages (voltage V1 in figure 1) float. This means that there is a large difference in the voltage levels required for their drive and the output level of the digital controller, and so some form of isolation is required. The conventional solutions to this problem are as follows:

a) use of high voltage integrated circuit technology. This technique is at present expensive and cannot benefit from

shrink technology in the future, as the silicon area for this type of product is mainly defined by the size of insulation rings and buffer output current capability. Moreover, they required floating auxiliary power supplies as bootstrap or charge pump circuits.

b) the second technique consists of using a high frequency transformer interfacing each upper gate drive with the digital controller. The primary circuit is driven with a 1Mhz carrier, the secondary circuit rectifying this carrier to charge or discharge the Power MOSFET gate (see reference [1]).

c) the third technique exploits the opportunity of using the power MOSFET input capacitance as an ON state memory, the OFF state memory using another auxiliary capacitor. Then signals are no more provided continuously (see reference 2). Then the pulse transformer requires fewer turns than with the second proposal. Consequently this pulse transformer is small and versions are available for use with surface mounting techniques. If cost prevails, the very small operating duty cycle of this pulse transformer can allow construction using tracks on a Printed Circuit Board as its windings.

3. PULSE CONTROLLED INVERTER

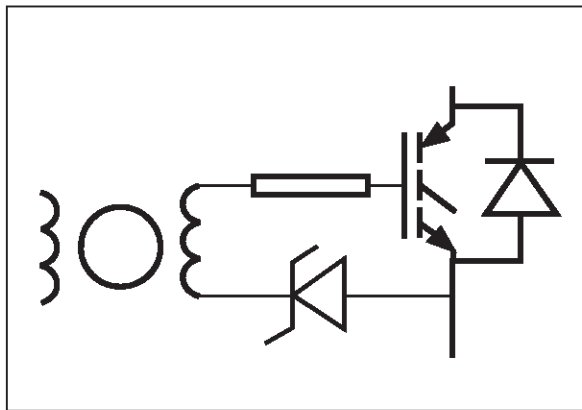
The major feature of this inverter is that the upper level interface is controlled by pulses in such a way that the gate drive is inexpensive and the pulse transformer can be implemented with PCB track windings.

This technique is amongst the cheapest available at present and has the advantage of being able to benefit from the trend to digital integration.

3.1 Drive Circuit

Because of its very small operating duty cycle the interface is able to use a pulse transformer built with a few turns around a small ferrite core. Triple transformer versions are now available in a plastic package for automatic assembly. This transformer provides reliable, low capacitance isolation between the control section and the upper level floating gate drive. It is used to transfer both energy and signals to the upper gate drive. The transformer secondary circuit is simplified, consisting of a zener diode and a series resistor (see figure 2).

Figure 2: Basic secondary circuit



The switching sequence is as follows:

- a positive pulse (ON pulse) applied to the transformer primary charges the gate through the zener diode. The resistance limits the charging current thus adjusting the switching time. The gate-to-source capacitance C_{GE} is used as a switch ON state memory.
- after the positive pulse a short circuit is applied across the primary transformer and the gate remains charged, as the zener diode is reverse biased.
- switching off requires the application of a negative pulse (OFF pulse) to overcome the zener voltage and discharge the gate

capacitance. During this negative pulse, the impedance across gate and source is defined by the series resistance.

The primary circuit requires only buffers to boost the digital signals to a current/voltage level compatible with the power MOSFET gate.

An interface like this does not require a floating auxiliary supply, nor does it limit the duty cycle which in this case has a pulse time of typically 500ns. Consequently the minimum ON and OFF times are about 500ns.

The sustaining voltage is determined by the pulse transformer which means that it can easily be much higher than the sustaining voltage of the power switches themselves. The same goes for the dV/dt immunity.

The total gate drive efficiency is unmatched due to the low transformer operation duty cycle and the non dissipative secondary circuit.

3.2 Digital controller features

The digital controller acts as a pulse generator providing two outputs (ON and OFF) for each upper switch and the direct gate drive for the lower switches. For high frequency operation, a typical pulse duration is less than 1 microsecond. For a three phase application, nine outputs are dedicated to the inverter drive; the digital controller generates three conventional output signals for the lower gate drives, the six others generating ON or OFF pulses for the upper gate drives.

Pulse timing

In bridge configuration, the upper switches are subject to dV/dt stresses during the commutation. To avoid cross-conduction, a low impedance must be applied across gate and source during a dV/dt .

Considering the secondary circuit shown fig.2, this condition requires the application

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of a negative pulse across the transformer during each critical dV/dt .

Figure 3 shows an example of such a timing for a three phase AC motor drive. Transistor T1 is operated by channels T1-on and T1-off. T1-on corresponds to the positive pulses applied across the pulse transformer primary to switch on T1. T1-off corresponds to the negative pulses turning off T1. These negative pulses are applied to switch off T1 at the appropriate point in the switching sequence, and also each time another transistor switches during the off period of T1, to prevent spurious turn-on.

4. USING A PULSED CONTROLLED INVERTER IN A BRUSHLESS PM DC MOTOR DRIVE

Figure 3: Inverter pulse timing

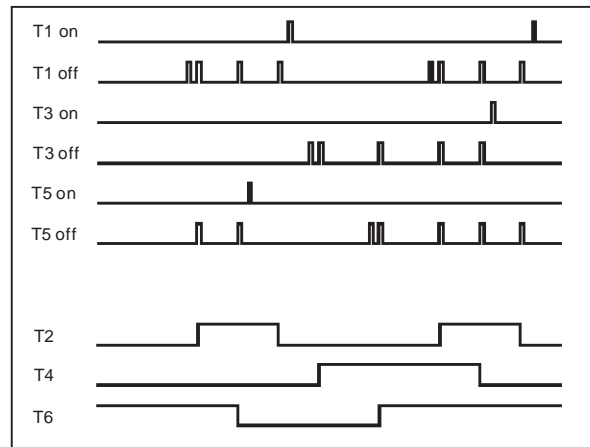
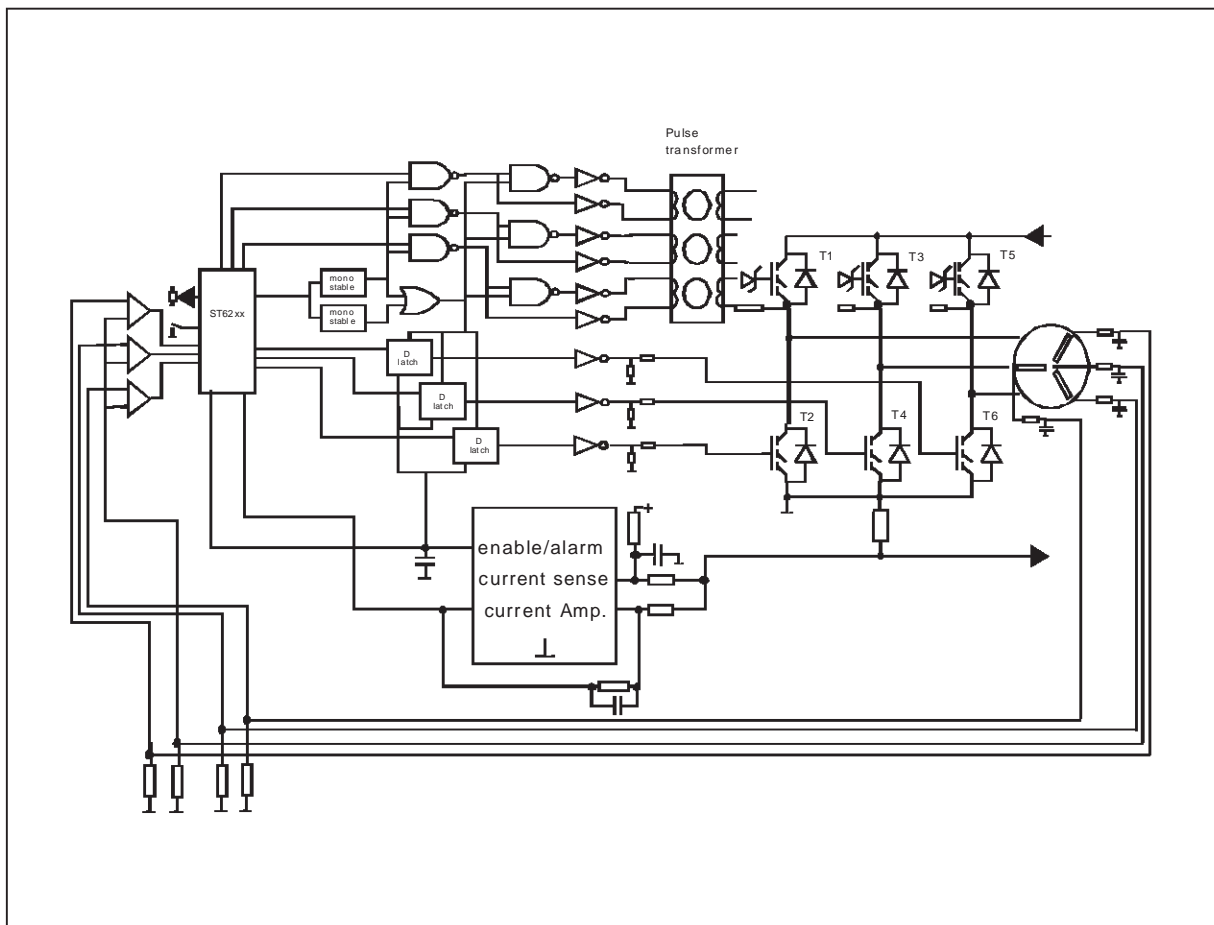


Figure 4 shows the block diagram of a DC PM brushless motor drive using this technique. The inverter uses six STGW20N50D TO-247 packages housing

Figure 4: DC PM brushless motor drive bloc schematic

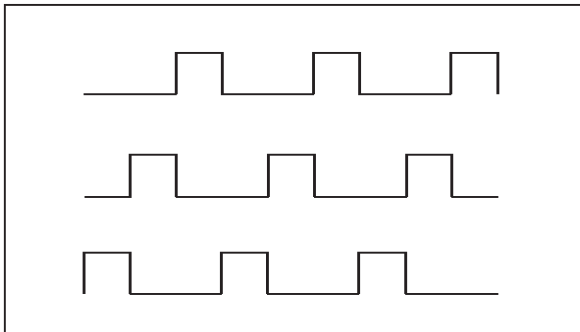


an IGBT and a discrete anti-parallel diode. The two devices are rated at 40A with $T_c = 25^\circ\text{C}$ and 20A with $T_c = 90^\circ\text{C}$. The triple pulse transformer is fully integrated in a plastic package (23Z284 from FEE-FIL-MAG Corp.). Nine push-pull buffers are required to interface the digital circuit with the power stage. The dedicated TD300/310 triple channel buffer is the ideal solution for interfacing the digital IC with these transformers.

The digital circuit is made of a low cost 8 bit CMOS micro-controller and a few logic gates. This ST6292 integrates 4kROM, 128bytes of RAM, 48 bytes of EEPROM, 21 fully software programmable I/O, one general purpose timer, one auto reload timer and one watchdog timer.

The micro-controller generates one PWM signal and six phase signals. Three of these are directly applied to the lower level buffers via a latch (see figure 5).

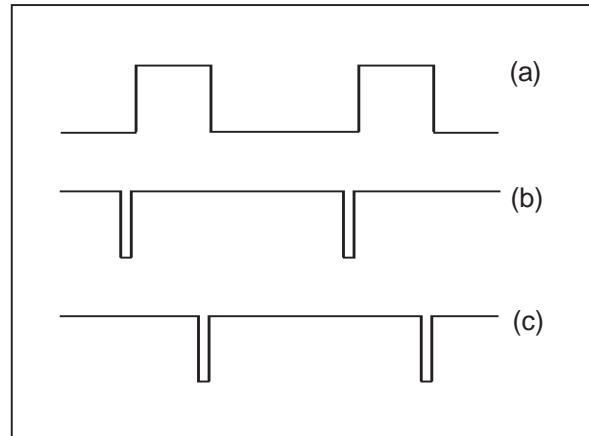
Figure 5: 120 degree 3 phase commutation signals



The three other phase signals are used to direct the PWM signal to the appropriate upper power switch to perform the current control. To operate the pulse transformers, this PWM signal is processed and only pulses are applied to the upper level buffer as following:

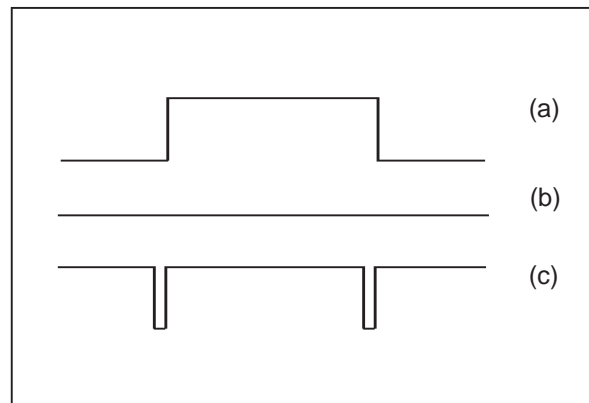
- figure 6 shows the PWM signal and the corresponding ON and OFF pulses driving the transformer buffer to turn ON/OFF the floating switches. Inputs of the transformer buffers are called channelON and channelOFF.

Figure 6: Basic PWM signal
ON channel signal
OFF channel signal



- when the upper switch has to be kept OFF (non activated phase), the PWM signal is processed in two OFF pulses via the OFF channel (see figure 7).

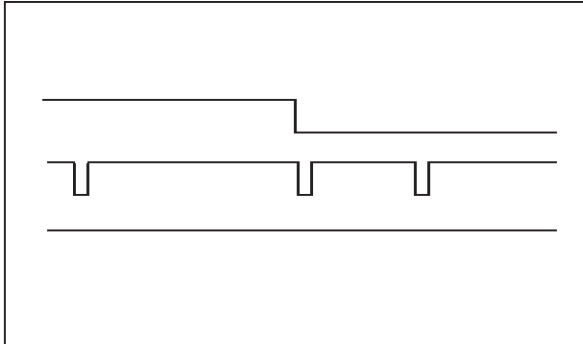
Figure 7: Basic PWM signal
ON channel (unoperated)
OFF channel



- when the lower switch is turned ON, there is a risk of cross conduction. At this point, the OFF channel generates a pulse synchronized with the phase signal in order to keep a low impedance across the gate and the source of the floating switch to prevent spurious turn-on (see figure 8).

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Figure 8: Low level phase commutation (inverted)
OFF channel (synchronized)
ON channel (unoperated)



This pulse controlled inverter has been successfully operated in DC PM brushless motor drive with the previous circuit and AC squirrel cage motor drive using a thru-sinusoidal control performed with a ST9 micro-controller. When low inductance packages are used, it is a very effective and cheap solution. It can be easily implemented with Power MOSFET or IGBT in ISOTOP package, in applications up to 10kW.

5. CONCLUSION

This pulse controlled inverter has been designed for AC and DC brushless motor

drives, but it is also suitable for UPS. It has the potential to reduce the digital to power interface cost while providing excellent performance. Driving Power MOSFET transistors by means of pulses only requires a cheap transformer and standard ICs resulting in a more cost effective solution.

This particular example takes advantage of a low cost ST6 micro-controller for large volume applications. In such a case product cost prevails on design time consideration, making this solution attractive.

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