

# AN5163K

## NTSC Color-TV Signal Processor IC

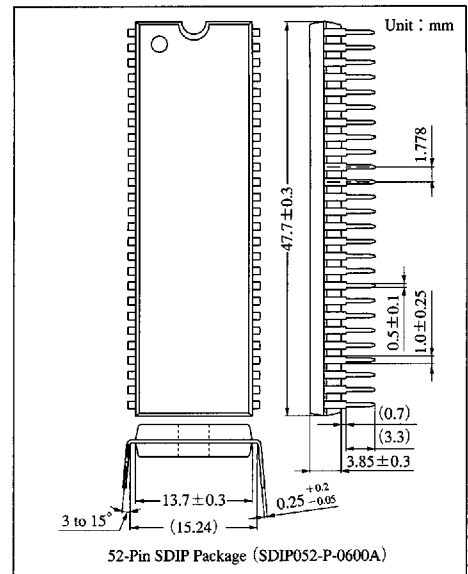
### Overview

The AN5163K is a single-chip IC which incorporates all functions needed for NTSC color-TV signal processing.

And sets production line will be rationalized by built-in I<sup>2</sup>C bus interface.

### Features

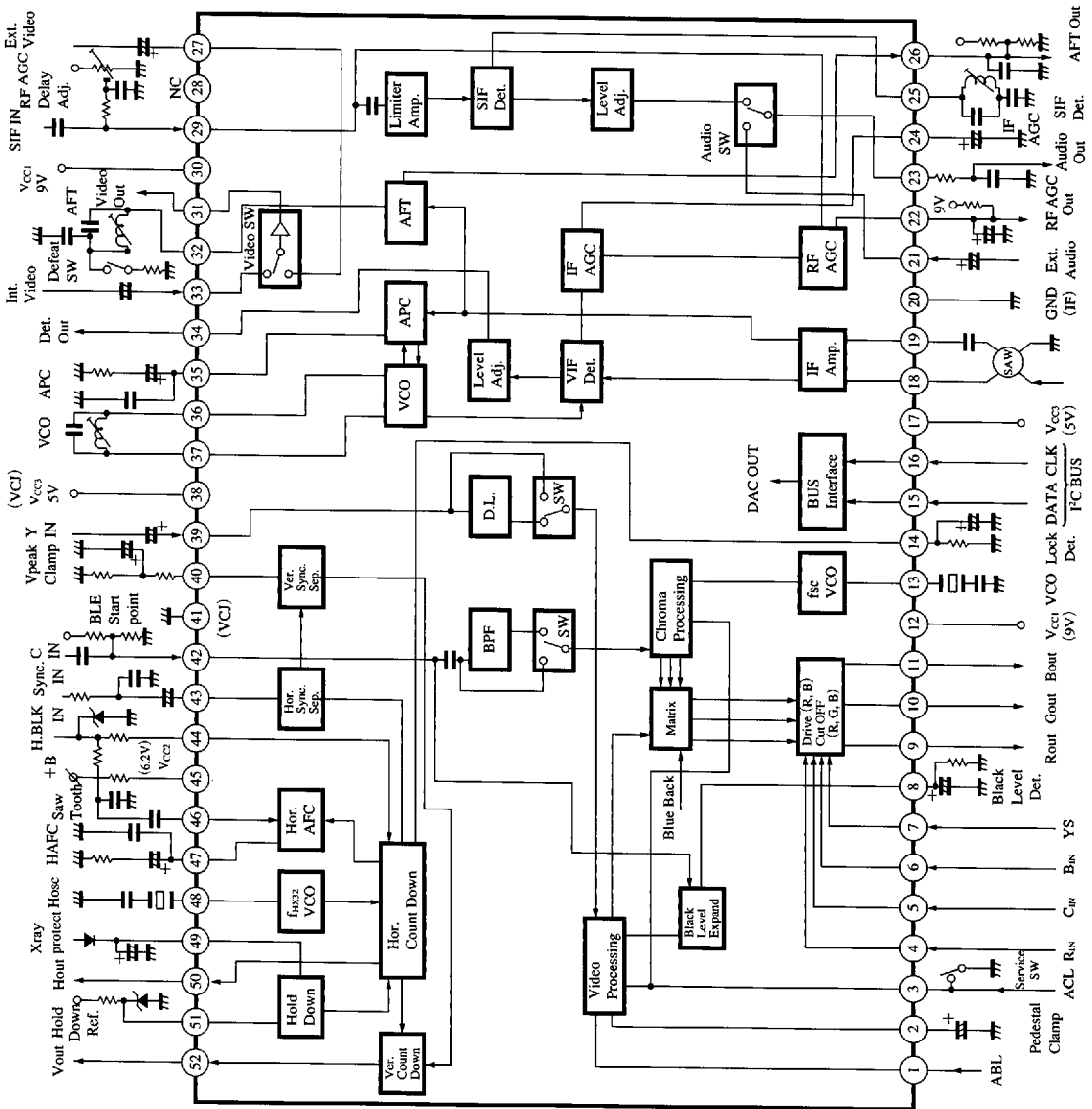
- Built-in VIF, SIF, video signal processing, chroma signal processing, and synchronization signal processing circuits
- Built-in an I<sup>2</sup>C bus interface circuit



### Pin Descriptions

Pin No.	Pin name	Pin No.	Pin name
1	ABL/Neck protection	27	EXT.Video input
2	Pedestal clamp	28	NC
3	ACL/Service switch	29	SIF In/RF AGC delay
4	R input	30	V <sub>CC1</sub> (2) VIF/SIF system
5	G input	31	Video output
6	B input	32	AFT coil
7	YS input	33	Int.Video input
8	Black Det. /Blank off/Sub Color	34	VIF detection output
9	R output	35	APC (VIF)
10	G output	36	VCO coil (1)
11	B output	37	VCO coil (2)
12	V <sub>CC1</sub> (1) video/chroma system	38	V <sub>CC3</sub> (1) video/jungle system
13	Chroma VCO	39	Y input
14	Lock detection	40	Ver. peak clamp
15	SDA	41	GND (1) video/chroma/jungle system
16	SCL	42	Chroma In/Black Level Start
17	V <sub>CC3</sub> (2) VIF/SIF system	43	Sync. input
18	VIF input (1)	44	FBP input
19	VIF input (2)	45	V <sub>CC2</sub> jungle system
20	GND (1) VIF/SIF system	46	Saw Tooth
21	Ext. Audio input	47	Hor. AFC
22	RF AGC output	48	Hor. OSC
23	Audio output	49	X-ray protection
24	IF AGC	50	Hor. output
25	SIF detection	51	Hold Down Ref.
26	AFT output	52	Ver. output

■ Block Diagram



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### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	
Supply voltage	$V_{CC}$	$V_{CC1(12,30)}$	10.5	V
		$V_{CC3(17,38)}$	6.0	
Supply current	$I_{CC}$	$I_{12+30}$	78	mA
		$I_{17+38}$	86	
		$I_{45}$	27	
Power dissipation <sup>Note 2)</sup>	$P_D$	1,480	mW	
Operating ambient temperature <sup>Note 1)</sup>	$T_{opr}$	-20 to +70	°C	
Storage temperature <sup>Note 1)</sup>	$T_{stg}$	-55 to +150	°C	

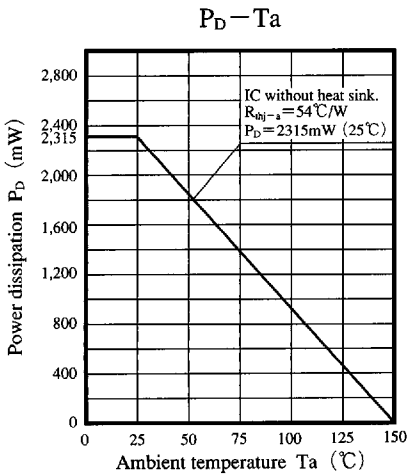
Note 1)  $T_a = 25^\circ\text{C}$  except operating ambient temperature and storage temperature.

Note 2) Allowable power dissipation of the package at  $T_a = 70^\circ\text{C}$ .

### Recommended Operating Range ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Range
Operating supply voltage range	$V_{CC1}$	8.1V to 9.9V
	$V_{CC3}$	4.5V to 5.5V
Operating supply current range	$I_{45}$	10mA to 25mA

### Reference



### ■ Electrical Characteristics (Ta=25±2°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current (1)	I <sub>30</sub>	Current when V <sub>30</sub> =9V	6	10	12	mA
Supply current (2)	I <sub>17</sub>	Current when V <sub>17</sub> =5V	22	28	34	mA
Supply current (3)	I <sub>12</sub>	Current when V <sub>12</sub> =9V	38	49	60	mA
Supply current (4)	I <sub>38</sub>	Current when V <sub>38</sub> =5V	26	33	40	mA
Stabilized supply current	I <sub>45</sub>	Current when V <sub>45</sub> =5V	3	5	7	mA
Stabilized supply voltage	V <sub>45</sub>	V <sub>45</sub> when I <sub>45</sub> =15mA	5.6	6.3	6.9	V
Video SW input terminal voltage	V <sub>27,33</sub>		2.2	2.6	3.0	V
External input terminal voltage	V <sub>21</sub>	DC measurement	3.5	4.0	4.5	V
Synchronous separation input clamp voltage	V <sub>CL</sub>		1.2	1.5	1.8	V
Output resistor (Pin②④)	R <sub>034</sub>	DC measurement	20	60	150	Ω
Input resistor (Pin②⑦, ③③)	R <sub>i27,33</sub>	DC measurement	27	37	47	kΩ
Output resistor (Pin③①)	R <sub>031</sub>	DC measurement	20	60	150	Ω
Output resistor (Pin②③)	R <sub>023</sub>	DC measurement	200	400	600	Ω
Input resistor (Pin②①)	R <sub>i21</sub>	DC measurement	55	65	75	kΩ
VIF Circuit (The test condition for below is f <sub>p</sub> =45.75MHz Vin=90dBμ)						
Video detection output (typ.)	V <sub>034</sub>	m=87.5% DATA 0B=8 (typ.)	1.3	1.6	1.9	V <sub>P-P</sub>
Video detection output (max.)	V <sub>034max.</sub>	DATA 0B=F, ratio to typ.	1.3	2.3	4.0	dB
Video detection output (min.)	V <sub>034min.</sub>	DATA 0B=0, ratio to typ.	-6.0	-3.0	-1.5	dB
Video detection output f characteristics	f <sub>pc</sub>	Frequency of output -3dB for 1MHz	5.5	8	11	MHz
Synchronous peak value voltage	V <sub>sp</sub>	m=87.5% DATA 0B=8	1.7	2.1	2.5	V
Video detection output DC voltage	V <sub>34</sub>	No input IF AGC min.	3.3	3.9	4.5	V
APC pull-in range (H)	f <sub>pph</sub>	Pull-in range of high band side	0.6	1.3	—	MHz
APC pull-in range (L)	f <sub>ppl</sub>	Pull-in range of low band side	—	-1.3	-0.6	MHz
VCO control sensitivity	β <sub>p</sub>	ΔV <sub>35</sub> =0.2V	1.3	2.2	3.1	kHz/mV
RF AGC sensitivity	G <sub>RF</sub>	Input level difference to become V <sub>22</sub> =1V→7V	—	3.0	4.5	dB
RF AGC maximum voltage	V <sub>22max.</sub>		8.9	9.0	9.1	V
RF AGC minimum voltage	V <sub>22min.</sub>		0	0.2	0.5	V
AFT discrimination sensitivity	μ <sub>AFT</sub>	Δf=±25kHz	18	29	40	mV/kHz
AFT center voltage	V <sub>26c</sub>	Vin no input	3.6	4.8	6.0	V
AFT maximum output voltage	V <sub>26max.</sub>	f=f <sub>p</sub> -500kHz	7.3	7.8	8.3	V
AFT minimum output voltage	V <sub>26min.</sub>	f=f <sub>p</sub> +500kHz	0	0.6	1.0	V
AFT detection terminal voltage	V <sub>32</sub>		2.3	2.8	3.3	V
Video SW voltage gain	G <sub>VSW</sub>	f=1MHz Vin=1V <sub>P-P</sub>	3.0	4.6	6.0	dB
Video SW f characteristics	f <sub>VSW</sub>	At -3dB from f=1MHz Vin=1V <sub>P-P</sub>	8.5	12	—	MHz
Sound IF output	V <sub>SIF</sub>	V <sub>p</sub> =90dBμ V <sub>s</sub> =70dBμ	94	100	106	dBμ
Video SW output difference voltage	ΔV <sub>VSW</sub>		-0.5	0	0.5	V
SIF Circuit (The test condition for below is f <sub>s</sub> =4.5MHz Vin=90dBμ)						
Audio detection output (standard)	V <sub>O23</sub>	Δf=±25kHz fm=400Hz DATA 0C=8 (typ.) R <sub>D</sub> =4.7kΩ	350	450	550	mVrms
Audio detection output (min.)	V <sub>O23max.</sub>	DATA 0C=F, ratio to typ.	2	2.8	4.5	dB
Audio detection output (max.)	V <sub>O23min.</sub>	DATA 0C=0, ratio to typ.	-9	-5	-2	dB
Audio output DC voltage (Ext.)	V <sub>23EX</sub>	DATA 0D-1=1 (external)	3.5	4.0	4.5	V
Audio SW voltage gain	G <sub>ASW</sub>	DATA 0D-1=1 (external)	-3	-1	+1	dB

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**Electrical Characteristics (cont.)** ( $T_a = 25 \pm 2^\circ\text{C}$ )

Parameter	Symbol	Condition	min	typ	max	Unit
<b>Video Signal Processing Circuit</b> (The test condition for below is established to be input 0.7V <sub>P-P</sub> stair step wave Gout)						
Video output (standard)	V <sub>YO</sub>	DATA 03=41 (typ.) (contrast)	1.8	2.4	3.0	V <sub>P-P</sub>
Video output (max.)	V <sub>YOmax.</sub>	DATA 03=7F (max.)	3.3	4.3	5.3	V <sub>P-P</sub>
Video output (min.)	V <sub>YOmin.</sub>	DATA 03=00 (min.)	0.3	0.5	0.7	V <sub>P-P</sub>
Contrast variable range	Y <sub>Cmax./min.</sub>	$\frac{03=7F}{03=00}$	15.0	19.0	23.0	dB
Video frequency characteristics	f <sub>YC</sub>	DATA 04=00 (sharpness) at -3dB	6.0	7.5	—	MHz
Sharpness variable range	Y <sub>Smax./min.</sub>	$\frac{04=7F}{04=00}$	7.0	10.5	14.0	dB
Pedestal level (standard)	V <sub>ped</sub>	DATA 02=81 (typ.) (brightness)	1.8	2.4	3.0	V
Pedestal variable range	$\Delta V_{ped}$	Difference between DATA 02=00 and FF	1.7	2.2	2.7	V
Brightness control sensitivity	$\Delta V_{BRT}$	Variation range of DATA 02=60 to A0	8.0	11.0	14.0	mV/bit
Video input clamp voltage	V <sub>39</sub>		3.2	3.7	4.2	V
ACL sensitivity	ACL		2.0	2.6	3.3	V/V
ABL sensitivity	ABL		0.9	1.1	1.3	V/V
Blanking level	V <sub>YBL</sub>	DC voltage of blanking pulse	0.5	1.0	1.5	V
DC restoration rate	T <sub>DC</sub>	APL10% to 90%	95	100	105	%
Service SW threshold voltage	V <sub>SSW</sub>		0.3	0.5	0.9	V
Neck protector threshold voltage	V <sub>NP</sub>		0.3	0.5	0.9	V
Blanking OFF threshold voltage	V <sub>BOFF</sub>		0.3	0.5	0.9	V
<b>Color Signal Processing Circuit</b> (The test condition for below is burst 150mV <sub>P-P</sub> , where B out as reference)						
Color difference output (standard)	V <sub>CO</sub>	Input : color bar DATA 00=41 (typ.)	1.4	1.9	2.4	V <sub>P-P</sub>
Color difference output (max.)	V <sub>COmax.</sub>	DATA 00=7F, amplitude on one side	2.5	3.2	3.9	V <sub>O-P</sub>
Color difference output (min.)	V <sub>COmin.</sub>	DATA 00=00	—	0	100	mV <sub>P-P</sub>
Contrast variable range	CC <sub>max./min.</sub>	$\frac{03=7F}{03=00}$	15	18	22	times
ACC characteristics (1)	ACC <sub>1</sub>	Burst 150→300mV <sub>P-P</sub>	0.9	1.0	1.2	times
ACC characteristics (2)	ACC <sub>2</sub>	Burst 150→30mV <sub>P-P</sub>	0.7	1.0	1.1	times
Tint center	$\Delta \theta_C$	Difference from DATA 01=41 (tint)	-13	0	+13	bit
Tint variable range (1)	$\Delta \theta_1$	DATA 01=7F	30	45	60	deg
Tint variable range (2)	$\Delta \theta_2$	DATA 01=00	-60	-45	-30	deg
Demodulation output ratio (R)	R/B		0.76	0.96	1.15	times
Demodulation output ratio (G)	G/B		0.27	0.34	0.41	times
Demodulation output angle (R)	$\angle R$		92	104	116	deg
Demodulation output angle (G)	$\angle G$		224	236	248	deg
Color killer tolerance	V <sub>KILL</sub>	0dB = 150mV <sub>P-P</sub> , BPF OFF	-49	-39	-33	dB
APC pull-in range (H)	f <sub>CPH</sub>		450	700	—	Hz
APC pull-in range (L)	f <sub>CPL</sub>		—	-1000	-450	Hz
<b>RGB Processing Circuit</b>						
Pedestal difference voltage	$\Delta V_{IPL}$	Difference voltage of RGB out pedestal	-0.3	0	0.3	V
Brightness voltage tracking	$\Delta T_{BL}$	DATA 02 (bright) difference between 02=41 to C1	0.9	0	1.1	times

**Electrical Characteristics (cont.)** ( $T_a=25\pm 2^\circ\text{C}$ )

Parameter	Symbol	Condition	min	typ	max	Unit
Video voltage gain relative ratio	$\Delta G_{YC}$	R,Bout output ratio to Gout	0.8	1.0	1.2	times
Video voltage gain tracking	$\Delta T_{\text{cont}}$	DATA 03 (contrast), ratio of 03=21 to 61	0.9	1.0	1.1	times/ times
Drive adjustment range	$G_{DV}$		4.0	6.0	8.0	dB
Cut-off adjustment range	$V_{\text{cut-OFF}}$		1.9	2.2	2.5	V
$Y_S$ threshold voltage	$V_{YS}$	Minimum level at which YS is ON	0.7	1.0	1.3	V
External RGB pedestal voltage	$V_{EPL}$		1.8	2.4	3.0	V
External RGB pedestal difference voltage	$\Delta V_{EPL}$		-250	0	250	mV
Internal/external pedestal difference voltage	$\Delta V_{PL/\Delta E}$	Internal-external	-250	0	250	mV
External RGB output voltage	$V_{ERGB}$		4.1	5.1	6.1	$V_{P-P}$
External RGB output difference voltage	$\Delta V_{ERGB}$		-0.6	0	+0.6	V
External RGB contrast variable range	$EC_{\text{max/min}}$		15	18	22	dB
Blue-back output voltage (1)	$V_{BB1}$	DATA 0D-0 (blue-back) Bout at 0D-0=0	2.5	3.5	4.5	$V_{P-P}$
Blue-back output voltage (2)	$V_{BB2}$	DATA 0D-0 (blue-back) R,Gout at 0D-0=0	-0.5	0	+0.5	V

**Synchronizing Signal Processing Circuit**

Horizontal free-run oscillation frequency	$f_{HO}$		15.45	15.75	16.05	kHz
Horizontal output pulse duty	$\tau_{HO}$		32	38	44	%
Horizontal pull-in range	$f_{HP}$		$\pm 500$	$\pm 650$	—	Hz
Vertical free-run oscillation frequency	$f_{VO}$		58	60	62	Hz
Vertical output pulse width	$\tau_{VO}$	$f_H=15.75\text{kHz}$ $f_V=60\text{Hz}$	0.57	0.64	0.71	ms
Vertical pull-in range	$f_{VP}$	$f_H=15.75\text{kHz}$	56	—	64	Hz
Vertical blanking pulse width	$\tau_{VB}$	Measure at RGB out	0.9	1.1	1.3	ms
Horizontal output voltage (H)	$V_{50H}$		2.4	2.7	3.0	V
Horizontal output voltage (L)	$V_{50L}$		—	0	0.3	V
Vertical output voltage (H)	$V_{52H}$		4.0	4.3	4.6	V
Vertical output voltage (L)	$V_{52L}$		—	0	0.3	V
Picture center variable range	$\Delta T_{HC}$		3.0	3.7	4.5	$\mu\text{s}$

**I<sup>2</sup>C Interface**

Sink current at ACK time	$I_{ACK}$		2.0	2.5	—	mA
SCL, SDA signal input High Level	$V_{HIGH}$		3.1	—	—	V
SCL, SDA signal input Low Level	$V_{LOW}$		—	—	0.9	V
Input maximum frequency	$f_{\text{max}}$		100	—	—	kbit/s

**VIF Circuit**

 (The test condition for below is  $f_p=45.75\text{MHz}$ )

Input sensitivity	$V_{PS}$	$V_{O34} = -3\text{dB}$	—	(46)	(52)	$\text{dB}\mu$
Maximum input	$V_{P\text{max}}$	$V_{O34} = +1\text{dB}$	(103)	(106)	—	$\text{dB}\mu$
SN ratio	$S/N_P$	$V_{in} = 90\text{dB}\mu$	(50)	(53)	—	dB
Differential gain	$DG_P$	$V_{in} = 90\text{dB}\mu$	(0)	(3)	(5)	%
Differential phase	$DP_P$	$V_{in} = 90\text{dB}\mu$	(0)	(3)	(5)	deg
Black noise detection level	$\Delta V_{BN}$		(-0.95)	(-0.75)	(-0.55)	V
Black noise clamp level	$\Delta V_{BNC}$		(0.28)	(0.48)	(0.68)	V
VCO switch ON drift	$\Delta f_p$	Oscillation frequency drift during 5 second to 5 minutes after sw. on	(-50)	(150)	(300)	kHz
Intermodulation	IM		(46)	(52)	—	dB
Input resistance (Pin⑱, ⑲)	$R_{18,19}$	$f=45.75\text{MHz}$	(1.0)	(1.3)	(1.6)	$\text{k}\Omega$
Input capacitance (Pin⑱, ⑲)	$C_{18,19}$	$f=45.75\text{MHz}$	(3.2)	(4.0)	(4.8)	pF

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### ■ Electrical Characteristics (cont.) (Ta=25±2°C)

Parameter	Symbol	Condition	min	typ	max	Unit
AFT defeat SW operation voltage	V <sub>AFTSW</sub>	Maximum voltage at V <sub>26</sub> =4.5±0.5V DC	(0.5)	(1.3)	(2.2)	V
Video SW crosstalk	CT <sub>VSW</sub>	f=1MHz	—	(-70)	(-60)	dB
<b>SIF Circuit</b>						
Input limiting level	V <sub>Lim</sub>	V <sub>O23</sub> = -3dB	—	(43)	(49)	dB $\mu$
AM rejection ratio	AMR	AM=30% Vin=90dB $\mu$	(45)	(55)	—	dB
Total harmonics distortion ratio	THD	Vin=90dB $\mu$	(0)	(0.3)	(0.5)	%
Audio SW crosstalk	CT <sub>ASW</sub>	Vin=90dB $\mu$	—	(-96)	(-90)	dB
<b>Video Signal Processing Circuit</b> (The test condition below is to be measured at G out)						
Delay line ON/OFF gain difference	$\Delta$ G <sub>DL</sub>	Ratio of $\frac{DL\ ON}{DL\ OFF}$	(0.9)	(1.0)	(1.1)	times
Y signal delay time	T <sub>DL</sub>	Phase difference between DATA 0D-4=0 (DL exists) and Y input (Pin <sup>Ⓒ</sup> )	(390)	(460)	(530)	ns
Delay time drift	$\Delta$ T <sub>DL</sub>	Phase difference between DATA 0D-4=0 and 0D-4=1	(200)	(240)	(280)	ns
Black level correction (1)	V <sub>BL1</sub>	Input : full black, difference between black correction SW 9V and OPEN	(-100)	(0)	(100)	mV
Black level correction (2)	V <sub>BL2</sub>	Input : full black, difference between black correction SW 3V and 9V	(400)	(700)	(1000)	mV
Black level correction (3)	V <sub>BL3</sub>	Input: approx. 20IRE, voltage difference between black correction SW open and 9V	(100)	(300)	(500)	mV
Black level correction start point (1)	V <sub>BS1</sub>	V <sub>42</sub> =2.5V	(40)	(45)	(50)	IRE
Black level correction start point (2)	V <sub>BS2</sub>	V <sub>42</sub> =4.5V	(27)	(32)	(37)	IRE
Black level correction start point (3)	V <sub>BS3</sub>	V <sub>42</sub> =6.5V	(15)	(20)	(25)	IRE
Contrast variation with sharpness	$\Delta$ V <sub>CS</sub>		(-300)	(0)	(+300)	mV
Brightness variation with sharpness	$\Delta$ V <sub>BS</sub>		(-250)	(0)	(+250)	mV
Input dynamic range	V <sub>Imax</sub>		(0.9)	(1.1)	—	V <sub>P-P</sub>
Y signal SN ratio	S/N <sub>Y</sub>		(53)	(59)	—	dB
Video output V <sub>CC</sub> variation	$\Delta$ V <sub>Y/Vcc</sub>	V <sub>CC1</sub> =8.1 to 9.9V	(0.0)	(0.1)	(0.25)	V <sub>P-P</sub> /V
Pedestal level V <sub>CC</sub> variation	$\Delta$ V <sub>PL/Vcc</sub>	V <sub>CC1</sub> =8.1 to 9.9V	(0)	(150)	(300)	mV/V
<b>Color Signal Processing Circuit</b> (The test condition below is burst 150mV <sub>P-P</sub> , where reference Bout)						
Demodulation output residual carrier	V <sub>car</sub>		—	(20)	(50)	mV <sub>P-P</sub>
BPF frequency characteristics (1)	f <sub>BPF1</sub>	BPF exists. $\frac{f=4MHz}{f=3.58MHz}$	—	(3)	—	dB
BPF frequency characteristics (2)	f <sub>BPF2</sub>	BPF exists. $\frac{f=3MHz}{f=3.58MHz}$	—	(-6)	—	dB
BPF frequency characteristics (3)	f <sub>BPF3</sub>	BPF exists. $\frac{f=2MHz}{f=3.58MHz}$	—	(-26)	—	dB
BPF frequency characteristics (4)	f <sub>BPF4</sub>	f=3.58MHz. $\frac{BPF\ lack}{BPF\ exists}$	(-3)	(0)	(3)	dB
VCO free-run frequency	f <sub>CO</sub>	No signal. Difference with f=3.579545MHz	(-300)	(0)	(300)	Hz
f <sub>CO</sub> V <sub>CC</sub> variation	$\Delta$ f <sub>CO/Vcc</sub>	Difference between V <sub>CC1</sub> =9.9V/ and V <sub>CC1</sub> =8.1V	(-300)	(0)	(300)	Hz
Demodulation output V <sub>CC</sub> variation	$\Delta$ V <sub>C/Vcc</sub>	V <sub>CC1</sub> =8.1V to 9.9V	(0)	(40)	(100)	mV <sub>P-P</sub> /V
Static phase error	$\Delta$ $\theta$	Tint deviation when f <sub>c</sub> = -300 to 300Hz change	—	—	(5)	deg/100Hz
Sub color control characteristics	$\Delta$ V <sub>subc</sub>	Color level fluctuation portion when DATA 0A-5=1 V <sub>8</sub> =4V	(1.2)	(1.5)	(1.9)	times
<b>RGB Processing Circuit</b>						
C-Y/Y ratio	R <sub>C/Y</sub>	Color bar input, measured at B out	(0.95)	(1.4)	(1.85)	times

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**Electrical Characteristics (cont.)** ( $T_a = 25 \pm 2^\circ\text{C}$ )

Parameter	Symbol	Condition	min	typ	max	Unit
Differential gain	DG <sub>Y</sub>		—	(3)	(5)	%
Pedestal level temperature variation	$\Delta V_{PLT}$	$T_a = -20$ to $+70^\circ\text{C}$	—	(-1.8)	—	mV/°C
Y <sub>s</sub> switching speed	f <sub>YS</sub>		(7)	(10)	—	MHz
External RGB input dynamic range	V <sub>DEXT</sub>		(2.2)	(2.5)	(2.8)	V
Spot killer operation	V <sub>SPK</sub>	V <sub>30</sub> =9V, V <sub>12</sub> voltage at which spot-killer operates	(7.8)	(8.1)	(8.4)	V
Internal/external crosstalk	CT <sub>RGB</sub>	Leak in f=1MHz 0.2V <sub>P.P</sub> Y <sub>s</sub> =5V	—	(-60)	(-50)	dB

**Synchronizing Signal Processing Circuit**

Horizontal output starting voltage	V <sub>fHS</sub>	f <sub>0</sub> >10kHz when horizontal oscillation output is above 1V <sub>P.P</sub>	(4.0)	(4.5)	(5.0)	V
Lock detection output voltage	V <sub>LD</sub>	In horizontal AFC lock	(5.7)	(6.0)	(6.3)	V
Lock detection charging and discharging current	I <sub>LD</sub>		(±0.6)	(±0.8)	(±1.1)	mA
FBP slice level	V <sub>FBP</sub>		(0.4)	(0.6)	(0.9)	V
Horizontal β curve	β <sub>H</sub>		(1.3)	(1.7)	(2.1)	Hz/mV
Horizontal AFC μ	μ <sub>H</sub>		(18)	(24)	(30)	μA/μs
Overvoltage protective operation voltage	V <sub>X-ray</sub>	Tolerance of minimum voltage (V <sub>6V51/2</sub> ) at which horizontal synchronization comes off	(-30)	(0)	(+30)	mV
Black-out operation voltage	V <sub>BLout</sub>	Difference voltage from hold-down to black-out	(0.13)	(0.18)	(0.23)	V

**IIC Interface**

Bus free before start	t <sub>BUF</sub>		(4.0)	—	—	μs
Start condition set-up time	t <sub>SU, STA</sub>		(4.0)	—	—	μs
Start condition hold time	t <sub>HD, STA</sub>		(4.0)	—	—	μs
Low period SCL, SDA	t <sub>LOW</sub>		(4.0)	—	—	μs
High period SCL	t <sub>HIGH</sub>		(4.0)	—	—	μs
Rise time SCL, SDA	t <sub>r</sub>		—	—	(1.0)	μs
Fall time SCL, SDA	t <sub>f</sub>		—	—	(0.35)	μs
Data set-up time (write)	t <sub>SU, DAT</sub>		(0.25)	—	—	μs
Data hold time (write)	t <sub>HD, DAT</sub>		(0)	—	—	μs
Acknowledge set-up time	t <sub>SU, ACK</sub>		—	—	(3.5)	μs
Acknowledge hold time	t <sub>HD, ACK</sub>		(0)	—	—	μs
Stop condition set-up time	t <sub>SU, STO</sub>		(4.0)	—	—	μs

**DAC**

4bit DAC DNLE	L <sub>4</sub>	1LSB = $\frac{\{\text{DATA (0F)} - \text{DATA (00)}\}}{15}$	(0.1)	(1.0)	(1.9)	$\frac{\text{LSB}}{\text{STEP}}$
7bit DAC DNLE	L <sub>7</sub>	1LSB = $\frac{\{\text{DATA (7F)} - \text{DATA (00)}\}}{127}$	(0.1)	(1.0)	(1.9)	$\frac{\text{LSB}}{\text{STEP}}$
8bit DAC DNLE	L <sub>8</sub>	1LSB = $\frac{\{\text{DATA (FF)} - \text{DATA (00)}\}}{255}$	(0.1)	(1.0)	(1.9)	$\frac{\text{LSB}}{\text{STEP}}$
7bit DAC DNLE (40)	L <sub>7-40</sub>	3F→40	(0.1)	(1.0)	(2.9)	$\frac{\text{LSB}}{\text{STEP}}$
8bit DAC DNLE (80)	L <sub>8-80</sub>	7F→80	(0.1)	(1.0)	(2.9)	$\frac{\text{LSB}}{\text{STEP}}$

Note) The characteristics value in parentheses is not a guaranteed value, but reference one on design.

## Operational descriptions

### • DAC CONTROL and SUB ADDRESS

SLAVE ADDRESS ; 8A

Control item	DATA BIT	Sub address	V <sub>CC</sub> -ON	Remarks
COLOR	7	00	41	DATA 00→chroma off
TINT (HUE)	7	01	41	41=0100 0001
BRIGHTNESS	8	02	81	81=1000 0001
CONTRAST	7	03	41	_____
SHARPNESS	7	04	41	_____
CUT OFF (R)	7+1+(1)	05	81	0D-5 for (1)
CUT OFF (G)	7+1+(1)	06	81	0D-6 for (1)
CUT OFF (B)	7+1+(1)	07	81	0D-7 for (1)
DRIVE (R)	7+1	08	81	81=1000 0001
DRIVE (B)	7+1	09	81	_____
Hor.CENTER	4	0A	09	09=0000 1001
VIDEO Adj.	4	0B	09	_____
AUDIO Adj.	4	0C	09	_____
BLUE BACK SW	1	0D-0	1	DATA 0→B BACK ON
AUDIO SW	1	0D-1	0	DATA 0→INT.
VIDEO SW	1	0D-2	0	DATA 0→INT.
BPF SW	1	0D-3	0	DATA 0→BPF ON
DELAY LINE SW	1	0D-4	0	DATA 0→D.L. ON
CUT OFF SW R	1	0D-5	0	DATA 0→OFF-SET OFF
CUT OFF SW G	1	0D-6	0	DATA 0→OFF-SET OFF
CUT OFF SW B	1	0D-7	0	DATA 0→OFF-SET OFF
Sub Color SW	1	0A-5	0	DATA 1→Black correction off, sub-color ON

Note) (1) Values at power ON are not guaranteed, and initial setting should be required.

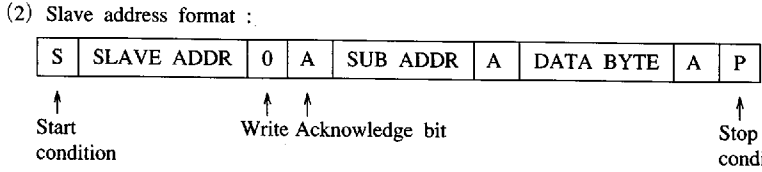
(2) For 7+1, the 7-bit DAC is changed over in two steps.

For 7+1+(1), the 7-bit DAC is changed over in four steps.

• I<sup>2</sup>C bus protocol

I<sup>2</sup>C-BUS Formats

(1) Slave address : 10001010



(3) Subaddress byte and data byte format :

Sub-addr <sup>(H)</sup>	functions	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
00	color	0	A06	A05	A04	A03	A02	A01	A00
01	tint	0	A16	A15	A14	A13	A12	A11	A10
02	brightness	A27	A26	A25	A24	A23	A22	A21	A20
03	contrast	0	A36	A35	A34	A33	A32	A31	A30
04	sharpness	0	A46	A45	A44	A43	A42	A41	A40
05	cutoff R	A57	A56	A55	A54	A53	A52	A51	A50
06	cutoff G	A67	A66	A65	A64	A63	A62	A61	A60
07	cutoff B	A77	A76	A75	A74	A73	A72	A71	A70
08	drive R	A87	A86	A85	A84	A83	A82	A81	A80
09	drive B	A97	A96	A95	A94	A93	A92	A91	A90
0A	H center	0	0	0	0	AA3	AA2	AA1	AA0
0B	Video Adj.	0	0	0	0	AB3	AB2	AB1	AB0
0C	Audio Adj.	0	0	0	0	AC3	AC2	AC1	AC0

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