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MICROELECTRONICS

APPLICATION NOTE

HOW THE TDE1897/8 BEHAVE IN EXTREME OVERLOAD CONDITIONS

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The circuit designer may be interested and get some insight on how the TDE1897/8 behave, if extreme overload conditions are forced on to them. Although the conditions may range outside the limits of the datasheet guarantieed performances, erroneous connections during an installation phase may occur and momentarily create such conditions. The performed tests confirm the extreme ruggedness of these devices and their ability to survive the accidental overload.

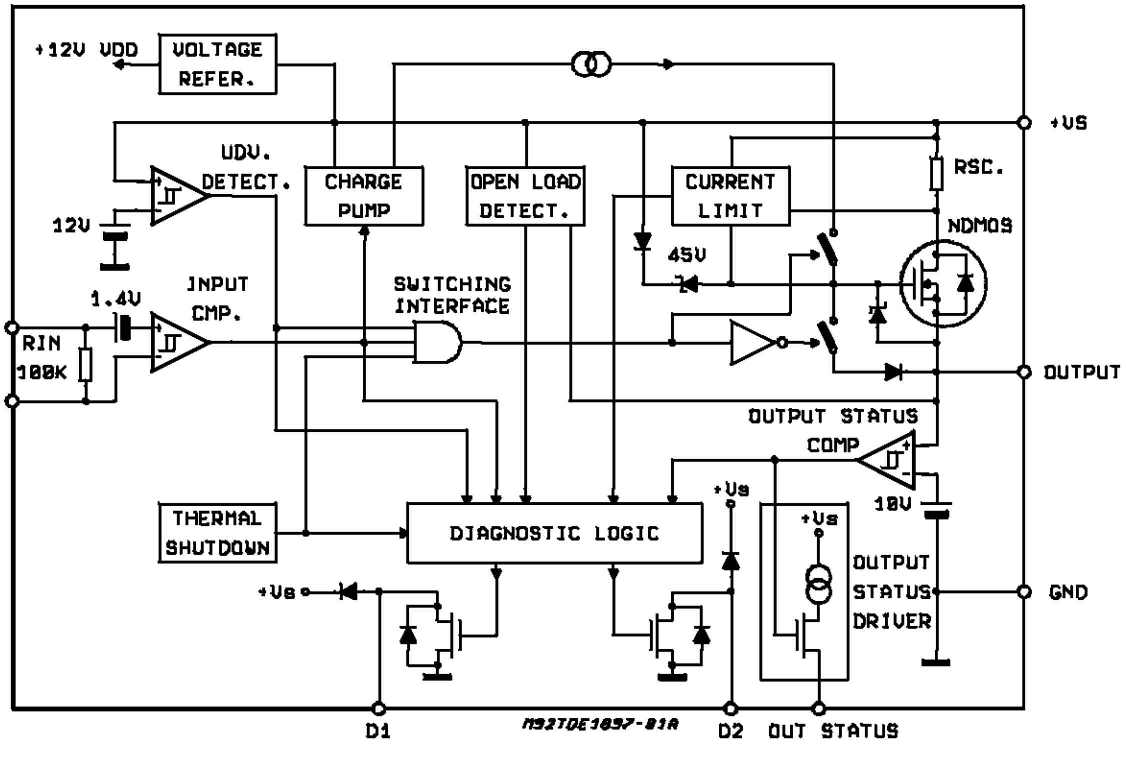
The TDE1897/8 is a monolithic Intelligent Power Switch (IPS) in High Side Configuration and BCD tecnology (see fig.1),dedicated to drive resistive and inductive load such as lamps, Relays, electro-valves, etc. An internal voltage clamping diode to $+V_S$ creates, in inductive load, a fast demagnetization path without external components.

Suitable for industrial application, it operates in the 18 to 35V supply range delivering output current up to 500mA. In typical application it can drive up to 1 - 1.5H load coil (48 to 60Ω typical associated resistance).

OVERLOAD CONDITIONS

To investigate the behaviour of TDE1897/8 in extreme inductive overload conditions, that may occur when too big a load is connected to the device output, tests were performed, in bias conditions that lead the device to function out of the datasheet operatives and rated limits.

Figure 1: Block Diagram

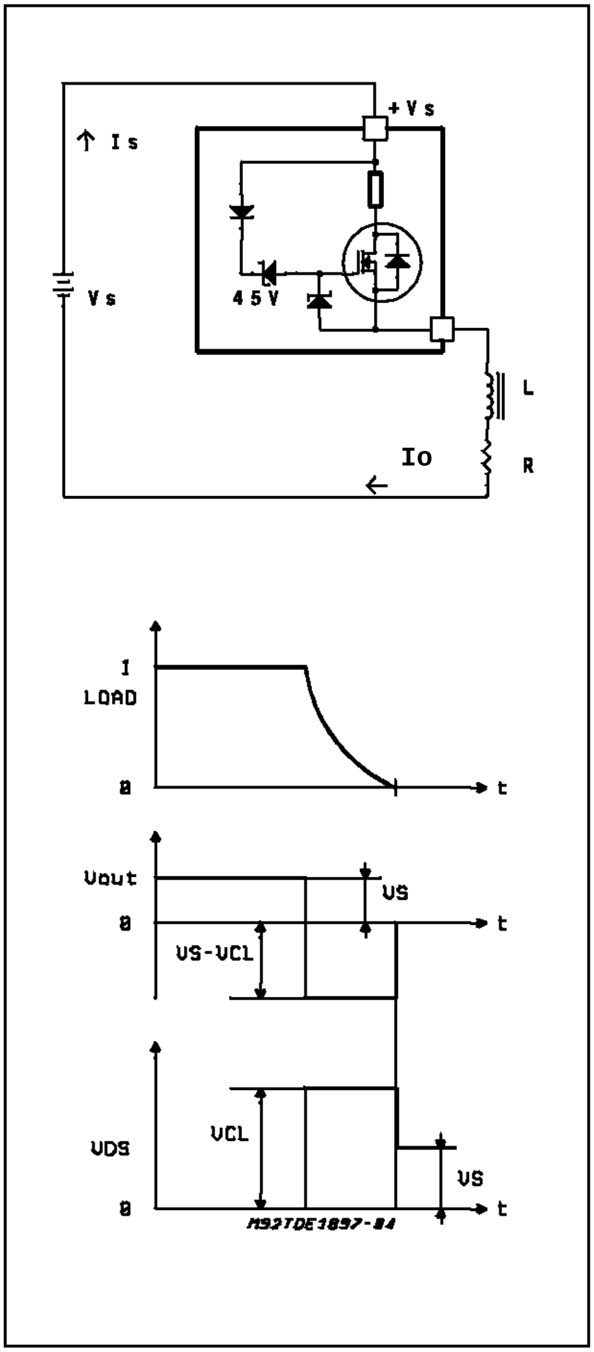


Test Conditions (referred to the circuit of fig. 2) V_S = +24V; I_O = Internal Limited; T_{amb} = 25°C; L = 1.4H (non saturating); R_l = 12Ω; Vi = 2V (Vih)(#); T_j = from øLim-Hy to øLim and above (*)

(#) The input signal asks for a permanent "on" state.

(*) øLim & Hy = thresholds of intervention and histeresis of the internal thermal protection circuit.

Figure 2: Inductive Load Equivalent Circuit and Demagnetization Cycle Waveforms



OVERLOAD OPERATION

Due to the internal limitation (I_{SC}), the output current (I_O) is not limited by the load (V_S/R_l = 2A; $I_{SC} \leq$ 1.5A) but by the device itself. As soon as the current reaches I_{SC}, the I.P.S. goes out of the minimum resistance state and increases its voltage drop so that $I_O = I_{CS}$. The silicon temperature of the D.U.T. increases rapidly up to the thermal protection threshold value (øLim) and such protection tries to cut-off the output DMOS. The turn-off of the output forces the demagnetization cycle, that discharges the energy of the inductive load (to V_S) through the device.

The higher clamped current value (I_{SC}) will produce, during the demagnetization, more stress conditions because of both:

- The higher energy in the magnetic load
- The higher peak power (1)

During the "on" state the power (P_{don}) on the D.U.T (see the 225msec. interval in fig.3) is defined by the I_O (I_{SC}) and R_l values. The chip temperature rapidly increases and reaches the upper thermal protection threshold value (øLim); at that moment the protection is triggered on, inducing the attempt of switch-off, the associated demagnetization phase (some 50msec. after the 225msec. interval), and finally the switch-off.

The D.U.T. starts then to cool down staying in the off-state, until the chip temperature goes down to lower thermal threshold value (øLim-Hy). When lower limit (øLim-Hy) value is underpassed, the thermal protection circuit withdraws itself, the chip resumes its normal functions and restarts another cycle. In facts its input has been connected permanently to a voltage level of more than 2V, meaning a continuos request for conduction. A new overload cycle is so started, and a periodic repetition of:

- load charging
- current limitation
- overtemperature and demagnetization
- cooling down in the off state .

It can be noted that, for given thermal parameters (Z_{th}, Thermal protection levels and hysteresis), differences in P_{don} affect only the "T_{ON}" and "T_{OFF}" duration and ratio of such periodic repetition.

The Minidip device ("DP" suffix) suffers heavier stress conditions than the SIP9 option ("SP" suffix) because of the package differences (Minidip vs. SIP9 involves higher thermal gradients).

Note(1)
During the demagnetization phase , the power dissipated inside the I.P.S. Chip is: $I_O(t) * V_{CL}$
-$I_O(t)$ decays to zero from I_{SC}.
-V_{CL} is set by the I.P.S. itself to about 50V

SOME MEASUREMENTS AND CALCULATIONS

For a typical TDE1897 sample in Minidip package (see Fig. 3) in "thermal" periodic repetition, the current (self-limited region) is limited to 1.1A and the voltage across the D.U.T. is = 10.8V for 225msec. "on" time. The energy dissipated on the D.U.T. in the demagnetization cycle is = 1.28 J (**) The repetition cycle rate is = 0.27Hz(t = 3.7sec.).

P_{don} (average) = 1.1A · 10.8V · 0.225sec/3.7s = 0.72W

P_{dem}. (average) = 1.28J · 0.27cycles/s = 0.346W

Adding the small power dissipated for operating quiescent current and for I_O(t)^2*R_{ON} in load-charging region, the total power $P_{(tot)}$= 1.1W is a realistic value.

Minidip (on the test-socket) $R_{thj\text{-}amb}$ is about 85 °C/W that leads the average temperature in the hot region of the chip) to 115-120°C (the chip isn't homogeneous in temperature. Higher temperatures are reached, during dissipation, in the area of the output DMOS).

Figure 3: TDE1897 in Minidip package Output Voltage (CH2) and Output Current (CH1) vs. Time in Thermal Periodic Repetition.

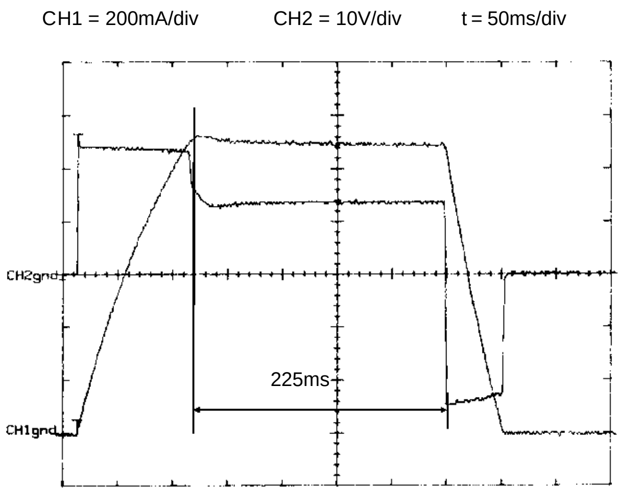
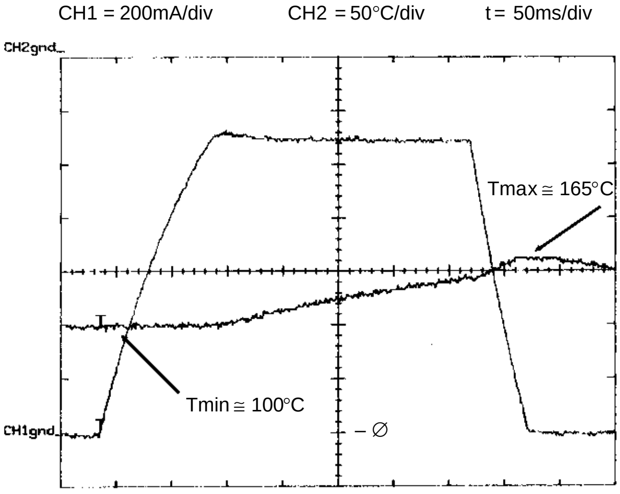


Figure 4: TDE1897 in Minidip package Output Current and Temperature in the Test Point, vs. Time.



For a typical TDE1898 sample in SIP9 package (see Fig. 5) in "thermal" periodic repetition, the current (self limited region) is limited to 1.15A and the voltage across the D.U.T. is = 10.2V for 300msec. "on" time. The energy dissipated on the D.U.T. in the demagnetization cycle is = 1.38J (**). The repetition cycle rate = 0.52Hz (t = 1.92sec.).

P_{don} (average) = 1.15A · 10.2V · 0.3s/1.92s = 1.83W

P_{dem} (average) = 1.38J · 0.522 cycles/s = 0.72W

The total power = 2.6W

The $R_{th\ j\text{-}amb}$ for SIP9 "on socket" is about 50 °C/W that leads the average temperature on the hot region of the chip to 150°C.

Note(**) The formula to use is :

$W = V_{CL} \cdot L/R_l * \{I_O - [(V_{CL} - V_S)/R_l] \cdot \log[1 + (I_O * R_l)/(V_{CL} - V_S)]\}$

It is also interesting to see (Fig. 4 and 6) the temperature versus time (mesaured monitoring the forward voltage drop of an internal diode placed 1.5mm from the center of the power DMOS) in a region of the chip at lower average temperature.

On the "hot" region, the estimated temperature is quite higher (up to + 60°C. on the peak temperature, during the demagnetization phase)

However no failure could be observed on the cheked devices also reducing the R_l value down to 8Ω, on some Minidip samples.

Figure 5: TDE1898 in SIP9 package Output Voltage (CH2) and Output Current (CH1) vs Time in Thermal Periodic Repetition

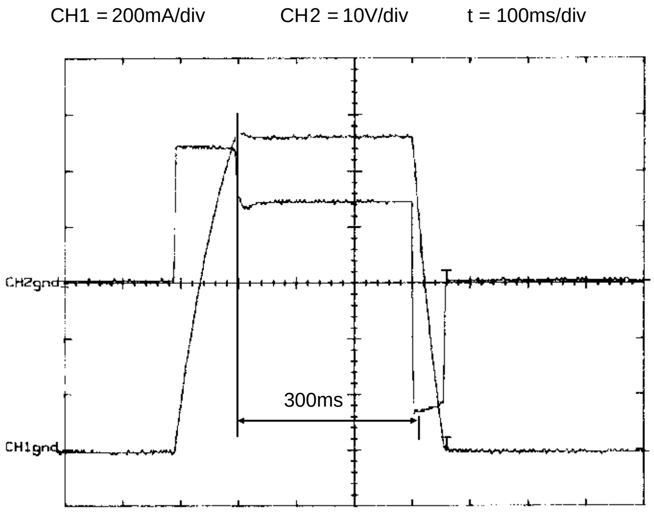
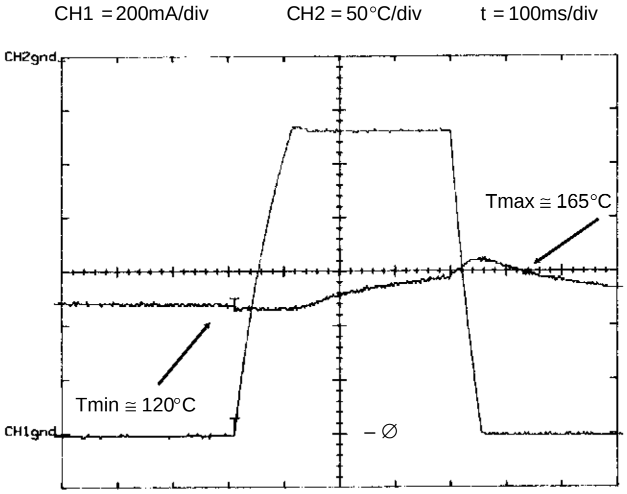


Figure 6: TDE1898 in SIP9 package Output Current and Test Point Temperature vs. Time



CONCLUSION

The complex protection sistem of TDE1897/8 proves effective also in extreme overload conditions. Althougth the behaviour of such devices in those conditions cannot be guaranteed due to the high temperatures that accelerate the intrinsic ageing mechanism, the test performed show that there is a lot of margin beyond the guaranteed limits of the device datasheet. These test also show that it is very likely that such devices will survive to non permanent overloads like the ones possible in practice during the installation or modification of an industrial control system.

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