
USING ST62xx I/O PORTS SAFELY

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INTRODUCTION

All members of the ST62 Series of Microcontrollers from SGS-THOMSON Microelectronics feature I/O ports with configurable bit functions. In addition many I/O bits may be set as inputs to the on-chip Analog to Digital Converter. This port bit function is in addition to the normal I/O functions of input (with or without internal pull-up resistor), output (open drain or push-pull) or edge/level selectable interrupt input (with pull-up). This flexibility makes the ST62 series suitable for many industrial control applications (and for many other uses).

This application note explains the architecture of the the I/O bit associated with these port functions and provides some indications on the correct use of these features for functions such as keyboard scanning and analog inputs. The correct manner to switch between these function is also demonstrated in order to prevent potential malfunctions in operation.

I/O PORT STRUCTURE

The ST62 I/O Port with Analog Input (hereafter referred to as I/O port) is comprised of 8 identical bit structures as shown in Figure 1. These include the interface to the ST62 internal databus and the three registers selecting the programmable options. I/O Ports without the analog capability are identical with the exception of the analog input buffer and control logic.

The control registers are named the Data Register (DR), the Data Direction Register (DDR) and the Option Register (OR). The DDR and OR are accessed directly at their addresses for read and write cycles i.e. data is written to the register and can be read from the register. The OR Register has a different operation and care must be taken when reading and writing to this register.

Table 1. Input and output modes of an I/O cell

DDR	OR	DR	I/O pin input/output modes
0	0	0	input with pull-up
0	0	1	input no pull-up
0	1	0	interrupt input with pull-up
0	1	1	analog input
1	0	DR	open drain output
1	1	DR	push-pull output

For most microcontrollers which use programmable flexibility for I/O pins, it has been common, to reduce the number of registers, to use the data register address for 3 purposes:

- writing to the DR
- reading the DR content
- reading the state of the I/O pin.

With this convention, the data read from the DR register may come from two different sources, the DR output and the I/O pin. The source is selected by a multiplexer controlled by the state of the DDR.

If the DDR bit corresponding to the I/O pin contains a “1”, the port pin is set to output. Subsequent read accesses to DR will return the content of the DR.

If the DDR bit corresponding to the I/O pin contains a “0”, the port pin is set to input. Subsequent read accesses to DR will return the state of the I/O pin. This means that the DR bit is effectively Read Only when the bit is in Output mode. To read the content of any DR bit set to input mode a copy of the DR content previously written must be saved in Data RAM.

Writing to the DR bit is possible in both input and output modes. It is important to note this as in input mode, DR is used to set the input pin characteristics (table 1). Due to the flexibility of programming each I/O bit individually, some pins of a port may be configured to input mode and others to output mode. Reading the DR will return some DR bit contents (from pins in output mode) and some I/O pin states (from pins in input mode) combined in the one byte. As will be shown in a following section this can create serious system malfunctions if care is not taken.

I/O PIN OPTIONS

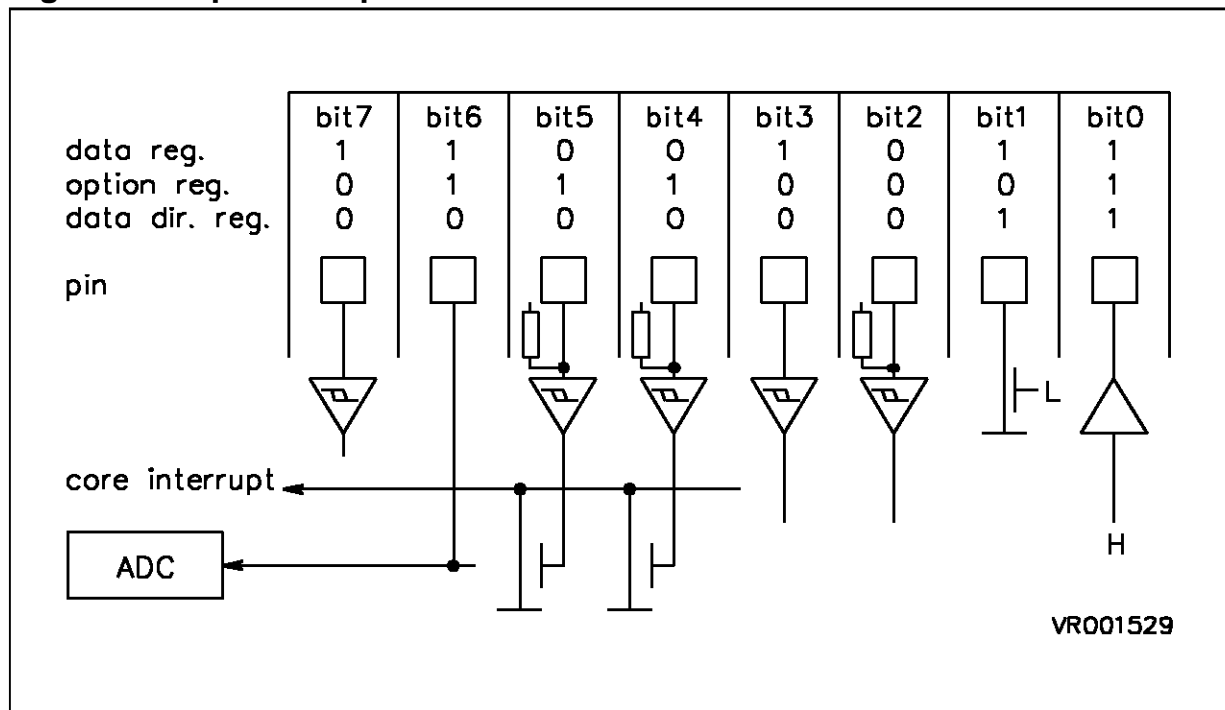
Each ST62 I/O pin with Analog capability can work as:

- a push-pull output
- an open drain output
- a schmitt trigger input with internal 100K pull-up
- a schmitt trigger input without pull-up
- an interrupt input with schmitt trigger and internal 100K pull-up
- an analog input (connected to the Analog to Digital converter)

As described in the previous section,

- each bit of the I/O port can have different characteristics
- each bit is completely independent of the others
- each bit has its own control bits defining its operation mode
- the bit operation modes can be changed by software at any time

Figure 4. I/O port with pins in different functions

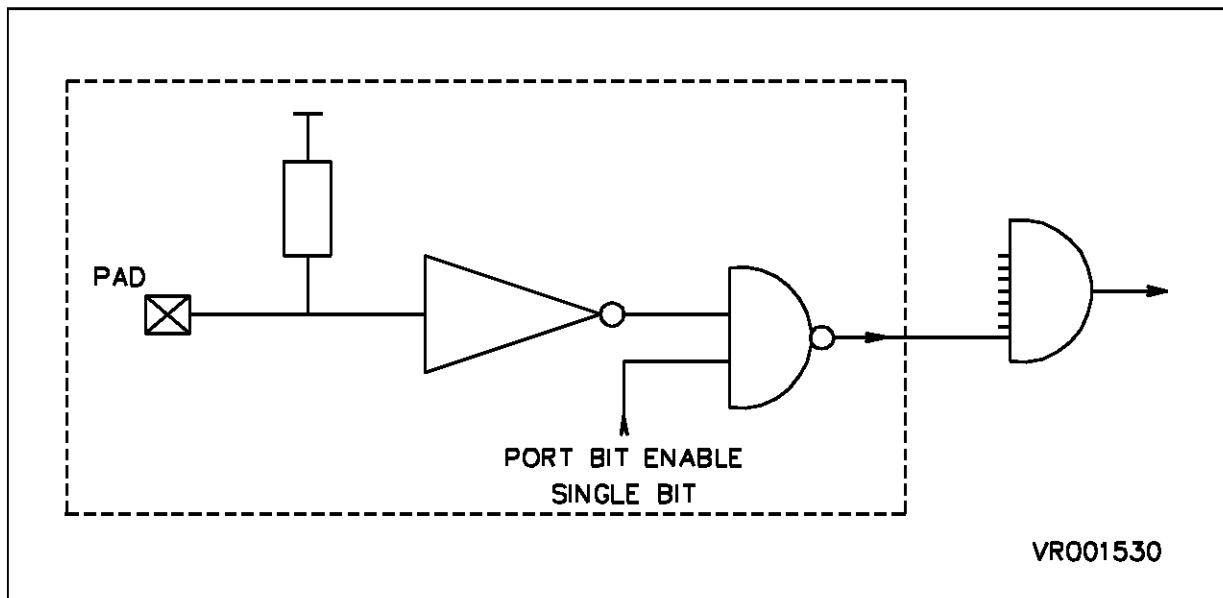


An example of a potential I/O port configuration is shown in figure 4. Pin 0 is in push pull output mode, outputting a high level, pin 1 is in open drain output mode and presents a high impedance (this is because DR is 1, causing the pull-down resistor to be turned off). Pin 2 is in input mode with pull-up, pin 3 is in input mode without pull-up, while pins 4 and 5 are interrupt inputs, pin 6 is analog input and pin 7 is an input without pull-up.

Only one pin of an ST62XX should be switched to analog input mode at any time. Otherwise, all pins switched to analog input mode will be connected together via the analog switches (RDSON = 1/4 kΩ)

When using the interrupt input with more than one pin configured for this function, all pins will be connected together in a logical “AND” function to the same core interrupt input line. A low signal at any of the inputs will pull the core interrupt line low, signifying an interrupt event. To get a high signal at the core interrupt line ALL interrupt inputs must be high.

Figure 5. Interrupt schematic for one I/O pin



OPERATION OF SINGLE BIT INSTRUCTIONS

The ST62XX instruction set includes four different instructions operating on single bits,

- SET Set Bit in Register
- RES Reset Bit in Register
- JRS Jump Relative IF Bit in Register is set
- JRR Jump Relative IF Bit in Register is reset

These instructions use a read-modify-write cycle.

The single bit instructions read a whole byte (8 bits), perform an “AND” (RES, JRR) or “OR” (SET, JRS) operation with a single bit mask operand (e.g 01h for bit 0, 04h for bit 2), and, in the case of SET and RES, write the result back to the source.

Thus the whole byte is processed, even if only one bit is modified or tested. This causes some constraints in using these instructions with the Data Register.

Table 2. Example for the operation of a single bit instruction

RAM (Before)			RAM (After)	
Address	Data		Address	Data
		SET 3,085h		
085h	055h	055h 01010101 B	085h	05Ch
		OR <u>008h 00001000 B</u>		
		05Ch 01011101 B		

Restrictions in using SET and RES instructions

As an example, let us assume that one or more of the pins of the port are set to input mode. A SET/RES operation on a bit of DR will read the state of the corresponding input pin instead of the content of DR. After modifying the specified bit, the result will be written (as a byte) back into DR.

Depending on the state of the specified inputs, the contents of DR may be changed. This can cause a change of the input mode by accident, that is, depending on the state of the corresponding bit in OR, the pin operation mode can be switched from input mode with pull-up to input mode without pull-up (or vice-versa) or from interrupt mode to analog input (or vice-versa). These side effects on the I/O port may be avoided if a copy of the DR content is kept in a RAM location. Now SET/RES instructions can be executed on the RAM location, and the result then written to DR as shown in Table 3.

Table 3. Example of a SET sequence with RAM buffer for DR

DRA	.def 00ch, 0ffh, 0ffh ; DR of IOP3
DRBUFF	.def 090h, 0ffh, 0ffh ; buffer for IOP3 DR
...	
SET 2, DRBUFF	
LD A, DRBUFF	
LD DRA, A	
...	

Such a sequence is only required for DR address when some bits are set to input. No restrictions apply for operating on OR or DDR.

It is recommended that the OR should be used primarily for switching of pin input operating modes. This register switches the port bits from input without pull-up to analog input, or switches from input mode with pull-up to interrupt input with pull-up. Transition diagrams showing the optimum coding sequence for modifying the states are shown in the following figures.

MODE TRANSITION DIAGRAMS

Figure 6 shows the recommended transfer sequence for changing from one state to another (no other transitions should be used).

Figure 6. Diagram for safe transitions

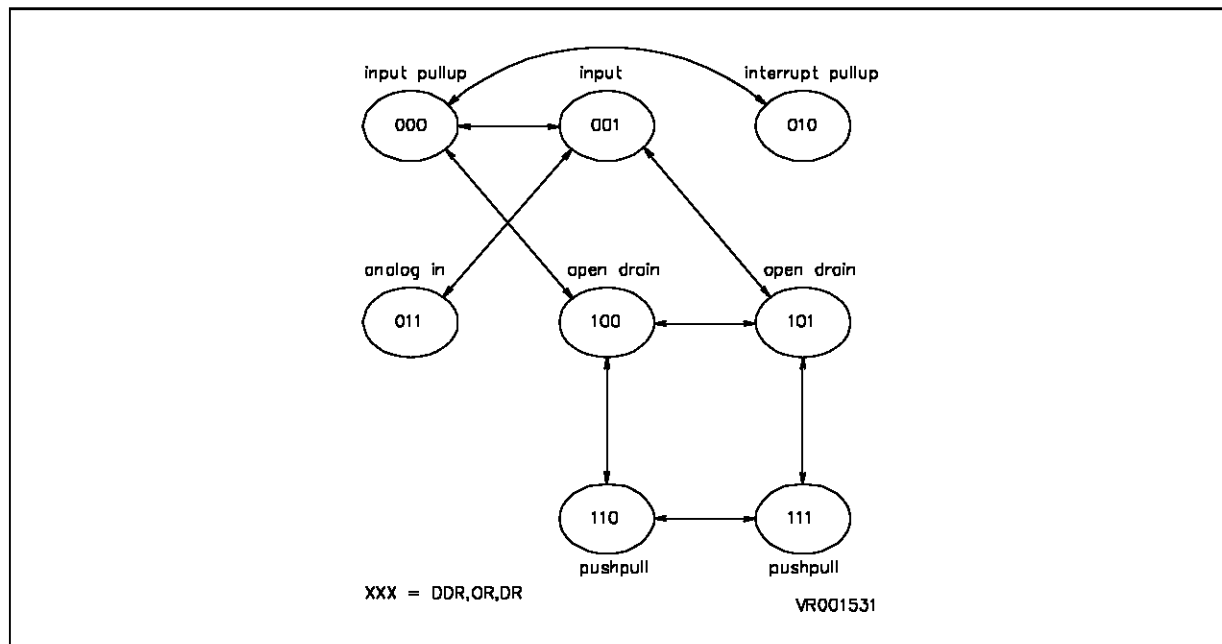


Figure 7 illustrates the transitions which are most likely to cause a change of operation mode causing unwanted side effects such as false interrupt generation or two pins being shorted together via the analog input line.

Figure 7. Diagram for risky transitions

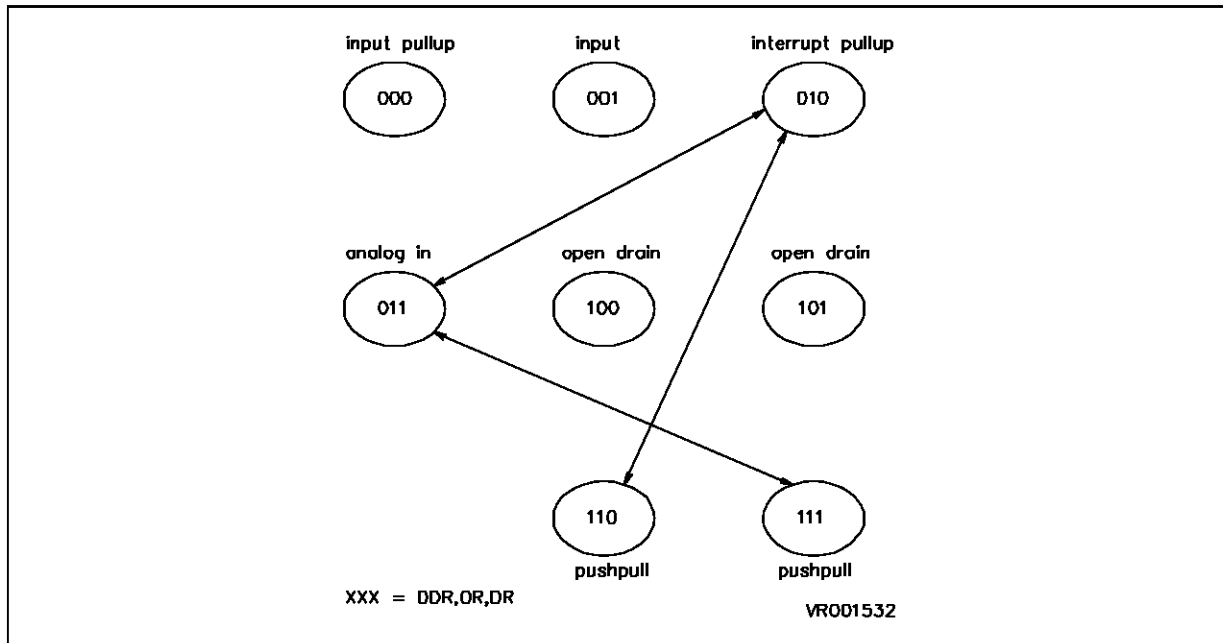
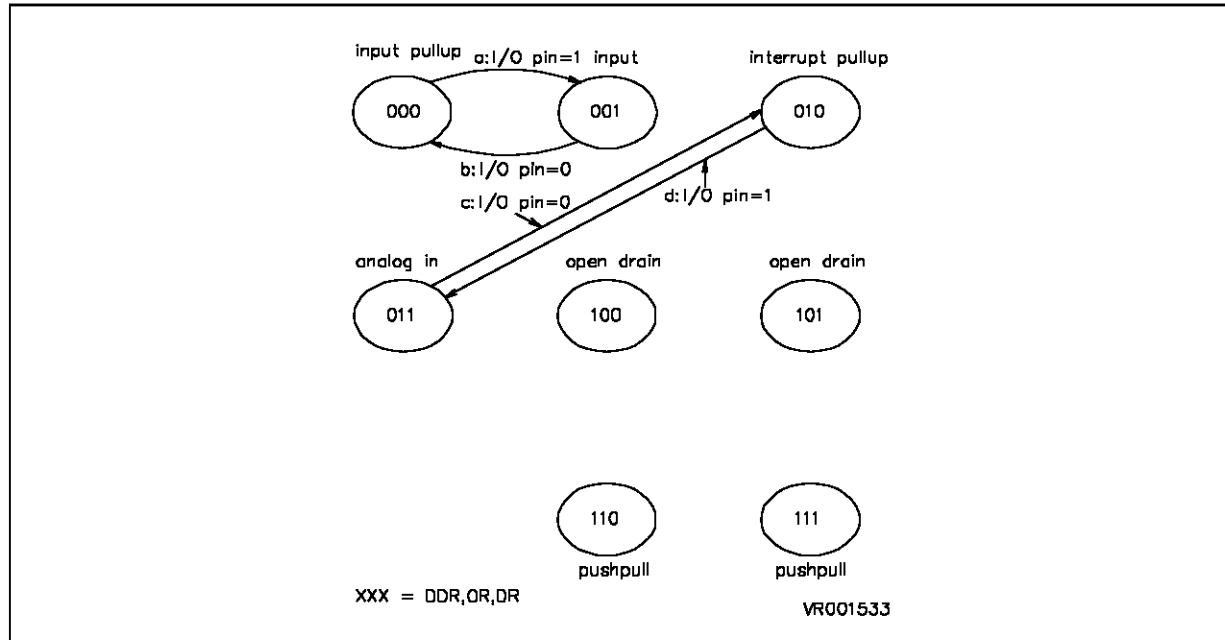


Figure 8 demonstrates the False transitions that can occur with SET/RES instructions depending on the state of the I/O pins.

Figure 8. Diagram for I/O data register False transitions



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