

# AN32502A

## Power Management IC for Intel PXA250 Application Processor

### ■ Overview

This IC is a power management IC developed for Intel PXA250 application processor.

### ■ Features

- AN32502A has 2-ch DC-DC converter, 3-ch linear regulator and an interface circuit for power management.

### ■ Applications

- PDA, Smart phone

### ■ Package

- HQFN 64 pin plastic package (HQFN-64)

### ■ Type

- Silicon monolithic Bi-CMOS IC



### ■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Storage temperature	Tstg	-55 to +125	°C	*1
2	Operating ambient temperature	Topr	-20 to +75	°C	*1
3	Operating ambient atmospheric pressure	Popr	$1.013 \times 10^5 \pm 0.61 \times 10^5$	Pa	—
4	Operating constant gravity	Gopr	9 810	m/s <sup>2</sup>	—
5	Operating shock	Sopr	4 900	m/s <sup>2</sup>	—
6	Supply voltage	VBAT	6.0	V	—
7	Supply current	I <sub>CC</sub>	—	mA	—
8	Power dissipation	P <sub>D</sub>		mW	*1, 2

Operating supply voltage range	VB, VDD1	2.8 V to 5.8 V
	BACKUP	2.0 V to 3.2 V

Note) \*1: Except for the storage temperature, operating ambient temperature, supply current and power dissipation, all ratings are for T<sub>a</sub> = 25°C.

\*2: Refer page 29

\*3: Care should be taken when insert this IC  
(inverted insertion cause destruction.)

\*4: Care should be taken this IC's surge breakdown voltage.

### ■ Electrical Characteristics at VB1 to VB5 = 3.6 V

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Ch.1									
1	DC-DC converter Output voltage 1	Vch1d1	1	VB = 3.6 V DAC = 1010100B Iout = 200 mA	1.26	1.3	1.34	V	—
2	DC-DC converter Output voltage 2	Vch1d2	1	VB = 3.6 V DAC = 1000000B Iout = 200 mA	1.07	1.1	1.13	V	—
3	DC-DC converter $\Delta$ output voltage	Vch1dd1	1	VB = 3.6 V DAC = 1010100B Iout = 200 mA/ 600 mA Output voltage difference	-30	0	30	mV	—
4	DC-DC converter Supply voltage characteristics	Vch1bb	1	VB = 3.4 V/ 5 V Iout = 200 mA Voltage characteristics setting	-30	0	30	mV	—
Ch.2									
5	LDO output voltage	Vch2	1	VB = 3.6 V Iout = 100 mA	3.1	3.2	3.3	V	—
6	$\Delta$ LDO output voltage	Vch2d	1	VB = 3.6 V Iout = 100 mA/ 250 mA Output voltage difference	-30	0	30	mV	—
7	Supply voltage characteristics	Vch2bb	1	VB = 3.4 V/ 5 V Iout = 100 mA Voltage characteristics setting	-30	0	30	mV	—

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Ch.2 backup circuit									
8	Backup output voltage	Vch2b1	1	COIN BAT = 2.5 V Iout = 2 mA	3.0	3.2	3.4	V	—
9	Charge voltage	Vch2c1	1	VB = 3.6 V Iout = 10 mA	2.7	3.0	3.3	V	—
10	Backup battery detection voltage	Vch2bkd	1	Threshold voltage of detection circuit	2.0	2.2	2.4	V	—
Ch.3									
11	LDO output voltage	Vch3	1	VB = 3.6 V Iout = 100 mA	3.2	3.3	3.4	V	—
12	$\Delta$ LDO output voltage	Vch3d	1	VB = 3.6 V Iout = 100 mA/ 500 mA Output voltage difference	-30	0	30	mV	—
13	Supply voltage characteristics	Vch3bb	1	VB = 3.4 V/ 5 V Iout = 100 mA Voltage characteristics setting	-30	0	30	mV	—
Ch.4									
14	DC-DC converter output voltage	Vch4	1	VB = 3.6 V Iout = 200 mA	3.1	3.2	3.3	V	—
15	DC-DC converter $\Delta$ output voltage	Vch4d	1	VB = 3.6 V Iout = 200 mA/ 500 mA Output voltage difference	-30	0	30	mV	—
16	Supply voltage characteristics	Vch4bb	1	VB = 3.4 V/ 5 V Iout = 200 mA Voltage characteristics setting	-80	0	80	mV	—

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
MOS switch									
17	V41 Output voltage	Vsw41	1	VB = 3.6 V VIN = 3.2 V, Iout = 100 mA I <sup>2</sup> C: 02H D2 bit: High VIN-V01	—	—	100	mV	—
18	V42 Output voltage	Vsw42	1	VB = 3.6 V VIN = 3.2 V, Iout = 100 mA I <sup>2</sup> C: 02H D1 bit: High VIN-V02	—	—	100	mV	—
General purpose output									
19	Output high level voltage	Vpoh	1	VB = 3.6 V VDD1 = 3.2 V Iout = 1 mA	VDD -0.3	—	—	V	—
20	Output low level voltage	Vpol	1	VB = 3.6 V VDD1 = 3.2 V Iout = -1 mA	—	—	0.3	V	—
Ch.5									
21	LDO Output voltage	Vch5	1	VB = 3.6 V Iout = 100 mA	2.716	2.8	2.884	V	—
22	ΔLDO Output voltage	Vch5d	1	VB = 3.6 V Iout = 100 mA/ 250 mA Output voltage difference	-30	0	-30	mV	—
23	Supply voltage characteristics	Vch5bb	1	VB = 3.4 V/ 5 V Iout = 100 mA Voltage characteristics setting	-30	0	30	mV	—

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Input/ output									
24	BAT_FLT detection voltage	Bflt	1	Lo BAT detection voltage	Typ -2.5%	3.4	Typ 2.5%	V	—
25	BAT_FLT return hysteresis	Bflth	1	Lo BAT detection reset voltage	Bflt 0.2	Bflt 0.3	Bflt 0.4	V	—
26	BAT_FLT low level output voltage	Bflt1	1		—	—	0.3	V	—
27	BAT_FLT high level output voltage	Bflt2	1		VDD1 -0.3	VDD1	VDD1 0.3	V	—
28	Reset detection voltage	Rset	1	Reset detection voltage	Typ -2.5%	3.1	Typ 2.5%	V	—
29	Reset return hysteresis	Rseth	1	Reset detection reset voltage	Bflt 0.2	Bflt 0.3	Bflt 0.4	V	—
30	nRESET low level output voltage	Rsetv1	1		—	—	0.3	V	—
31	nRESET high level output voltage	Rsetv2	1	At no load (pulled down only 3 M $\Omega$ resistor internally)	VDD1 -0.3	VDD1	VDD1 0.3	V	—
32	WAKEUP low level output voltage	Rwkv1	1		—	—	0.3	V	—
33	WAKEUP high level output voltage	Rwkv2	1		VDD1 -0.3	VDD1	VDD1 0.3	V	—
34	ChSW low level input voltage	Rswv1	1		—	—	0.3	V	—
35	ChSW high level input voltage	Rswv2	1		VDD1 -0.3	VDD1	VDD1 0.3	V	—
36	nRESETOUT low level input voltage	Rrsv1	1		—	—	0.3	V	—
37	nRESETOUT high level input voltage	Rrsv2	1		VB -0.3	VB	VB 0.3	V	—

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Serial interface									
38	DATA input high level	Datah	1		VDD1 -0.3	VDD1	VDD1 0.3	V	—
39	DATA input low level	Datal	1		—	0	0.3	V	—
40	LT input high level	Cth	1		VDD1 -0.3	VDD1	VDD1 0.3	V	—
41	LT input low level	Ctl	1		—	0	0.3	V	—
42	LT frequency	Ctf	1		—	—	400	kHz	—
43	ACK drive capability	Vack	1	Pull-up 4.7 k $\Omega$	—	—	0.3	V	—
44	Operating current 1	INC1	1	VDD = 3.2 V S2: Low Ch.2 only operation Charge circuit stopping At no load	70	100	130	$\mu\text{A}$	—
45	Operating current 2	INC2	1	VDD = 3.2 V S2: Low Ch.2 only operation Charge circuit operation At no load	80	120	150	$\mu\text{A}$	—
46	Operating current 3	INC3	1	VDD = 3.2 V PWR_EN: High Ch.1 only operation At no load	4	6	8	mA	—
47	Operating current 5	INC5	1	VDD = 3.2 V S3: High Ch.3 only operation At no load	70	100	130	$\mu\text{A}$	—
48	Operating current 6	INC6	1	VDD = 3.2 V S4: High Ch.4 only operation At no load	5	8	11	mA	—
49	Operating current 7	INC7	1	VDD = 3.2 V Serial 01H D2: High Ch.5 only operation At no load	70	100	130	$\mu\text{A}$	—
50	Operating current 8	INC8	1	VDD = 3.2 V All channels are operating At no load	10	15	20	mA	—

### ■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^\circ\text{C} \pm 2^\circ\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Ch.1									
51	DC-DC converter Transient response characteristics	Vch1ex	1	VB = 3.6 V DAC = 1000000B Iout: Change 0 mA to 200 mA Rising time 50 ns Output voltage difference $\Delta V$	—	$\pm 100$	—	mV	—
52	DC-DC converter output ripple voltage	Vch1rr	1	VB = 3.6 V DAC = 1000000B At no load	—	$\pm 40$	—	mV	—
53	DC-DC converter startup time	Vch1tr	1	VB = 3.6 V At no load from start up signal input till output bottom limit	—	2	—	ms	—
54	Oscillator frequency	fdv1	1	PWR_EN: High Oscillator frequency of the built-in oscillation circuit for ch.1	—	500	—	kHz	—
Ch.2									
55	LDO Ripple rejection 1	Vch2rr1	1	VB = 3.6 V VBpp = 0.3 V/ 1 kHz Iout = 150 mA	—	-40	—	dB	—
56	LDO Ripple rejection 2	Vch2rr2	1	VB = 3.6 V VBpp = 0.3 V/ 10 kHz Iout = 150 mA	—	-30	—	dB	—
57	LDO Transient response characteristics	Vch2ex	1	VB = 3.6 V Iout: 10 mA to 200 mA Rising time 1 $\mu\text{s}$ Output voltage difference $\Delta V$	—	$\pm 50$	—	mV	—
58	LDO start up time	Vch2tr	1	VB = 3.6 V At no load from start up signal input till output bottom limit	—	10	—	ms	—

Note) \*: The above values are reference values on design, but not guaranteed values.

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Ch.3									
59	LDO ripple rejection 1	Vch3rr1	1	VB = 3.6 V VBpp = 0.3 V/ 1 kHz Iout = 150 mA	—	-40	—	dB	—
60	LDO ripple rejection 2	Vch3rr2	1	VB = 3.6 V VBpp = 0.3 V/ 10 kHz Iout = 150 mA	—	-30	—	dB	—
61	LDO transient response characteristics	Vch3ex	1	VB = 3.6 V Iout: Change 10 mA to 200 mA Output voltage difference $\Delta V$	—	$\pm 50$	—	mV	—
62	LDO start up time	Vch3tr	1	VB = 3.6 V At no load from start up signal input till output bottom limit	—	10	—	ms	—
Ch.4									
63	DC-DC converter transient response characteristics	Vch4ex	1	VB = 3.6 V Iout: Change 10 mA to 200 mA Rising time 1 $\mu\text{s}$ Output voltage difference $\Delta V$	—	$\pm 100$	—	mV	—
64	DC-DC converter output ripple voltage	Vch4rr	1	VB = 3.6 V At no load	—	$\pm 40$	—	mV	—
65	DC-DC converter start up time	Vch4tr	1	VB = 3.6 V At no load from start up signal input till output bottom limit	—	3	—	ms	—
66	Oscillator frequency	fdv4	1	S4: High Oscillator frequency of the built-in oscillation circuit for ch.4	—	500	—	kHz	—

Note) \*: The above values are reference values on design, but not guaranteed values.

■ Electrical Characteristics at VB1 to VB5 = 3.6 V (continued)

Note)  $T_a = 25^{\circ}\text{C} \pm 2^{\circ}\text{C}$  unless otherwise specified.

B No.	Parameter	Symbol	Test circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Ch.5									
67	LDO ripple rejection 1	Vch5rr1	1	VB = 3.6 V VBpp = 0.3 V / 1 kHz Iout = 150 mA	—	-40	—	dB	—
68	LDO ripple rejection 2	Vch5rr2	1	VB = 3.6 V VBpp = 0.3 V / 10 kHz Iout = 150 mA	—	-30	—	dB	—
69	LDO transient response characteristics	Vch5ex	1	VB = 3.6 V Iout = Change 10 mA / 200 mA Rising time 1 $\mu\text{s}$ Output voltage difference $\Delta V$	—	$\pm 50$	—	mV	—
70	LDO start up time	Vch5tr	1	VB = 3.6 V At no load from start up signal input till output bottom limit	—	10	—	ms	—

Note) \*: The above values are reference values on design , but not guaranteed values.

## ■ Pin Descriptions

Pin No.	Pin name	I / O	Function
1	nRESET	O	Reset output
2	BAT_FLT	O	Low voltage detection output
3	LGND		GND for input/ output part
4	CT	I	Capacitor connection pin (internal oscillator)
5	RT	I	Resistor connection pin (internal oscillator)
6	SGND		GND (signal system)
7	SCP	I	Capacitor for circuit protection
8	VO1	O	V <sub>IN</sub> switch output 1
9	VIN	I	Stabilized DC voltage input
10	VO2	O	V <sub>IN</sub> switch output 2
11	PR2	I	Start up control (Ch.2)
12	PR3	I	Start up control (Ch.3)
13	SS4	I	Soft start (Ch.4)
14	IN4	I	Error amplifier inverted input (Ch.4)
15	FB4	I	Error amplifier output (Ch.4)
16	PGND4		GND (Ch.4)
17	LC4	O	Low side control output (Ch.4 )
18	HC4	O	High side control output (Ch.4 )
19	VB5		Power supply (for ch.4 output circuit)
20	FBR3	I	Feedback (Ch.3)
21	PGND3		GND (Ch.3)
22	LC3	O	External MOS gate control (Ch.3)
23	VB4		Power supply (Ch.3)
24	PGC2	O	External MOS gate control (Ch.2 reverse current protection)
25	FBR2	O	Feedback (Ch.2)
26	PGND2		GND (Ch.2 )
27	LC2	O	External MOS gate control (Ch.2)
28	VB3		Power supply (Ch.2)
29	PGND1		GND (Ch.1)
30	LO1	O	Low side control output (Ch.1)
31	HC1	O	High side control output (Ch.1)
32	VB2		Power supply (for ch.1 output circuit)

## ■ Pin Descriptions (continued)

Pin No.	Pin name	I / O	Function
33	FBR1	I	Feedback (Ch.1)
34	FB1	O	Error amplifier output (Ch.1)
35	IN1	I	Error amplifier inverted input (Ch.1)
36	SS1	O	Soft start (Ch.1)
37	FBC1	O	External MOS gate control (Ch.5)
38	FBD1	I	Feedback (Ch.5)
39	PR5	I	Start up control (Ch.5)
40	PB0	O	General purpose output 0
41	PB1	O	General purpose output 1
42	PB2	O	General purpose output 2
43	PB3	O	General purpose output 3
44	PB4	O	General purpose output 4
45	VREFDET1	O	Reference voltage filter
46	VB1		Power supply (control signal system)
47	FBB	I	Feedback for backup charging regulator
48	REGOUT	O	Output for backup regulator
49	BACKUP		Power supply (backup)
50	VBO	O	Through output of boost DC-DC for backup
51	VBI	I	Through input of boost DC-DC for backup
52	BO	O	Control of boost DC-DC for backup
53	VREFDET2	I	Reference voltage filter (for backup circuit)
54	PWR_EN	I	Start up control input
55	S2	I	On/off control (Ch.2)
56	S3	I	On/off control (Ch.3)
57	S4	I	On/off control (Ch.4)
58	DATA	I	Serial data input
59	LT	I	Serial clock input
60	VDD1		Power supply (input/ output)
61	TRIG	I	System switch
62	nRESETOUT	I	External reset signal input
63	PS	I	I <sup>2</sup> C/ hard pin priority setting
64	WAKEUP	O	Interruption signal for CPU

### ■ Technical Data

- Circuit diagrams of the input/ output part and pin function descriptions

Note) \*: The characteristics listed below are reference values based on the IC design and are not guaranteed.

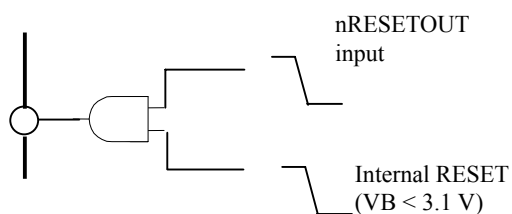
Pin name	Function	Inner circuit
TRIG (Pin 61)	It connect power supply voltage (VB).	
nRESETOUT (Pin 62)	External reset signal input: High: VB On Low : GND off (reset) CMOS input	
S1 (Pin 54)	On/off switch of ch.1: High: VDD1 On Low : GND Off CMOS input	
S2 (Pin 55)	On/off switch of ch.2: High: VB Off Low : GND On  Pulled down by 1 MΩ resistor internally. Pin 61 setting leads to determination of which to prioritize the setting of this pin or I <sup>2</sup> C serial setting.	
S3 and S4 (Pin 56 and pin 57)	On/off switch of ch.3 to ch.4: High: VDD1 On Low : GND Off CMOS input  Pulled down by 1 MΩ resistor internally Pin 61 setting leads to determination of which to prioritize the setting of these pins or I <sup>2</sup> C serial setting.	
PS (Pin 63)	Determining priority of I <sup>2</sup> C serial or external pin setting for ch.2, ch.3 and ch.4 on/off. High: VB I <sup>2</sup> C take priority over hard pin setting Low : GND Hard pin settings take priority over I <sup>2</sup> C  CMOS input	

### ■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin Name	Function	Inner circuit
DATA (Pin 58)	I <sup>2</sup> C data input CMOS input	
LT (Pin 59)	I <sup>2</sup> C clock input CMOS input	
nRESET (Pin 1)	Reset signal output Low active Pulled down by 3 MΩ internally	



### ■ Technical Data (continued)

- Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin Name	Function	Inner circuit
BAT_FLT (Pin 2)	Output of judgment on below-threshold voltage for VB1 (Pin 45).  Threshold level: 3.4 V Low active Pulled down by 1 MΩ internally	
WAKEUP (Pin 64)	Interrupt signal output in DVM mode  High active Pulled down by 1 MΩ internally	
P0 to P4 (Pin 40 to pin 44)	General purpose output  Initial setting: Low Can individual control by I <sup>2</sup> C data  △Output voltage is 0.3 V. (When output current is 1 mA.)	

### ■ Technical Data (continued)

#### 1. I<sup>2</sup>C command

##### 1) I<sup>2</sup>C address

This IC's address is '11100110'.

##### 2) I<sup>2</sup>C sub address

'\_' mark shows initial setting.

Sub	D7	D6	D5	D4	D3	D2	D1	D0
00H	CORE_I setting DAC 7 bit							
CORE DAC	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	<u>0 = Low</u> <u>1 = High</u>	0
01H	DVM	DVM change	Ch.2 mode	Ch.3 mode	Ch.4 mode	Ch.5 mode		
MODE CTL	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Non Real time</u> <u>1 = Real time</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	0	0
02H	P0	P1	P2	P3	P4	V01	V02	Backup circuit
GPO etc.	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>	<u>0 = Off</u> <u>1 = On</u>

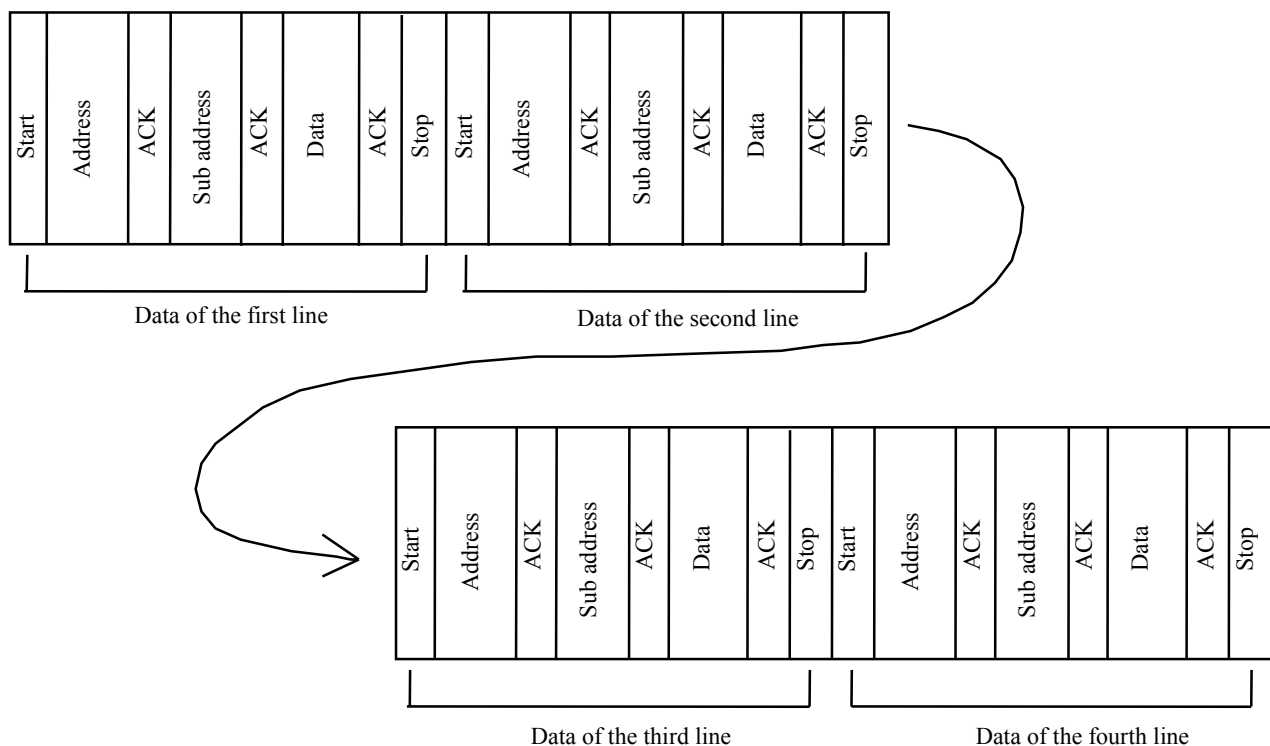
- Don't input another data except shown in this table.
- When set D7 bit of sub address 01H, it is possible to change output voltage of ch.1 shown in sequence chart (5).  
In this case, setting data is latched when PWR\_EN signal changes low to high.  
( Non real time mode )

■ Technical Data (continued)

2. Serial data transmission

Note) \*: When a line of data is transmitted, start/ stop condition is required each time.  
 When sub address is same, repetition of ACK and DATA allows for upgrade of settings in serial order.

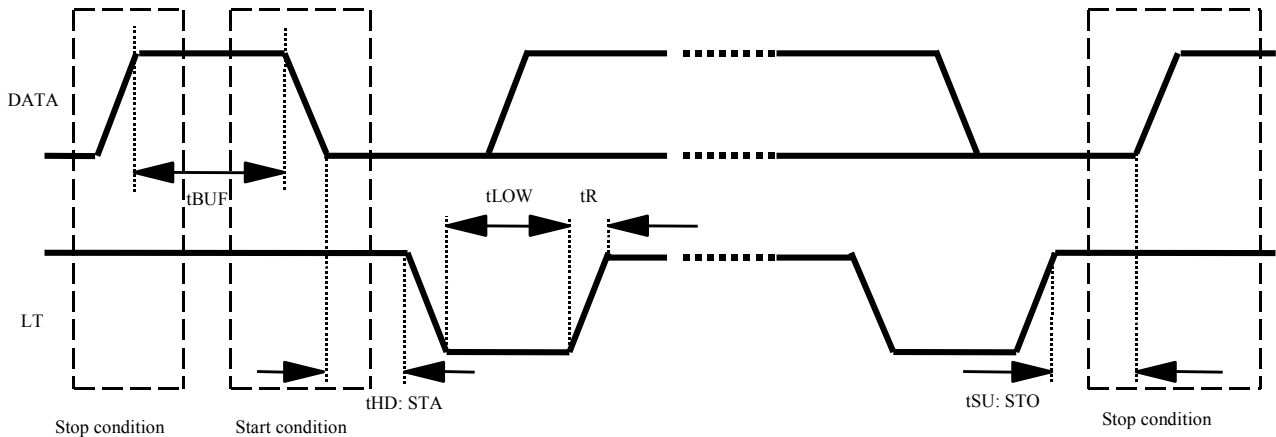
Example: When all data of four lines are transmitted



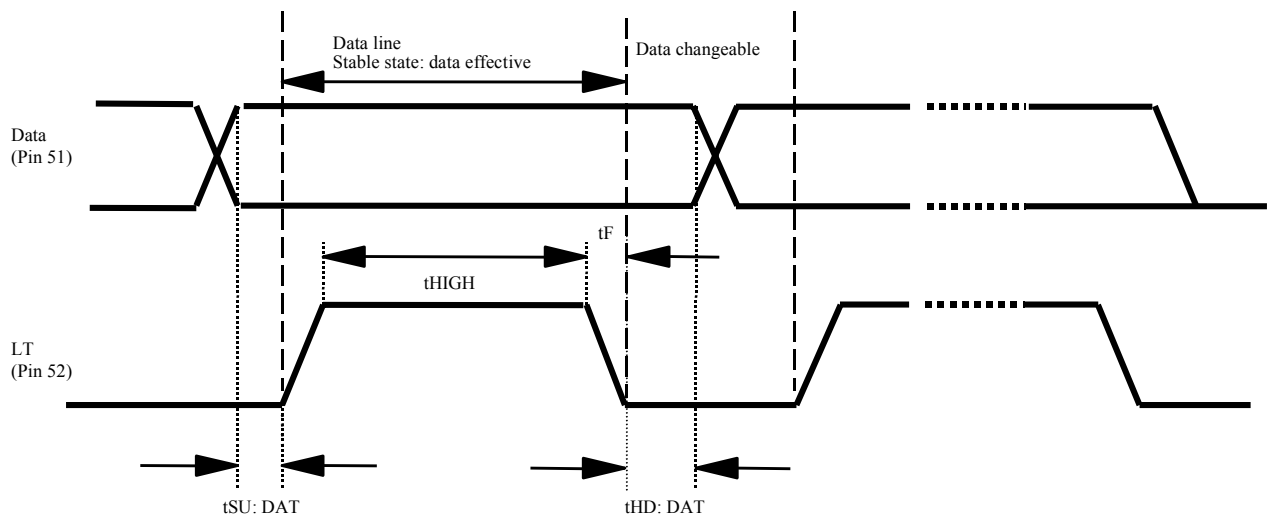
■ Technical Data (continued)

3. I<sup>2</sup>C serial data timing

- Start condition and stop condition



- Data recognition condition

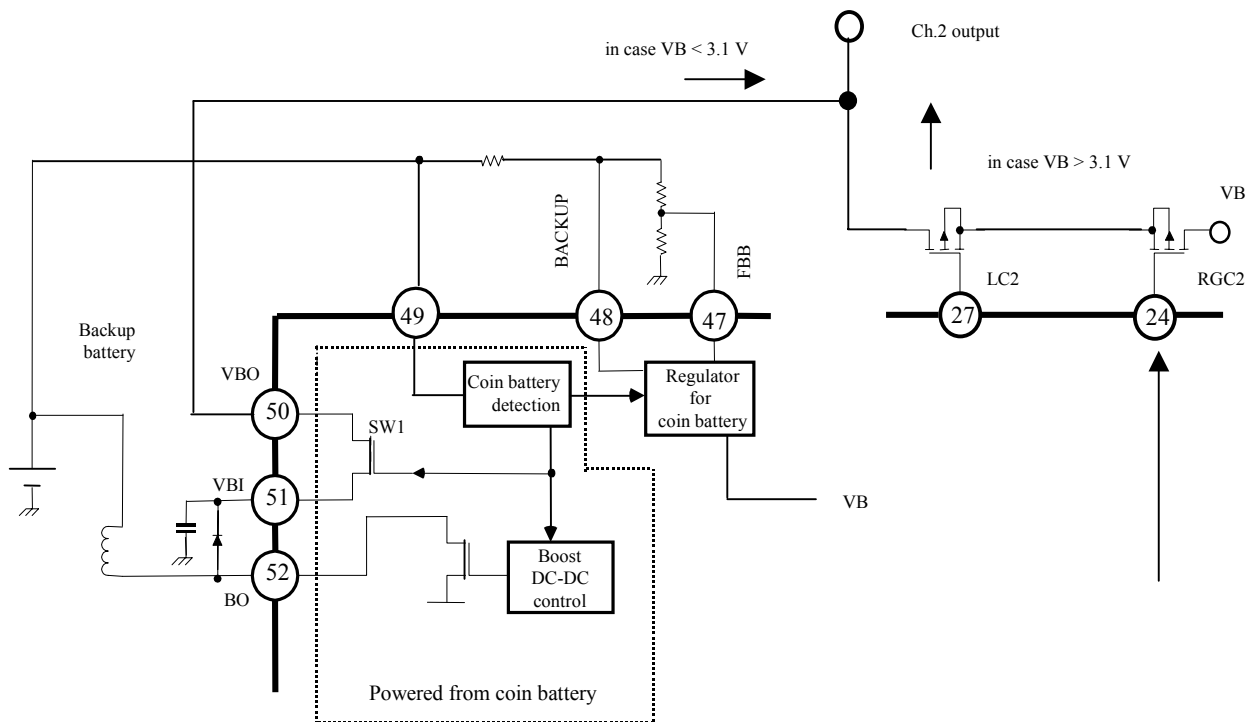


- Recommended operating condition

Parameter	Symbol	Min	Max	Unit
Time the bus must be free before a new transmission can start.	tBUF	1.3	—	microsec
Hold time start condition. After this period, the first clock pulse is generated.	tHD: STA	0.6	—	microsec
Low period of the clock..	tLOW	1.3	—	microsec
Rise time of both SDA and SCL lines.	tR	—	1000	n sec
Set-up time for stop condition.	tSU: STO	0.6	—	microsec
Set-up time data	tSU: DAT	100	—	n sec
High period of the clock.	tHIGH	0.6	—	microsec
Fall time of both SDA and SCL lines.	tF	20	300	n sec
Hold time data for I <sup>2</sup> C ICs.	tHD: DAT	0	0.9	microsec
SCL clock frequency.	fSCL	0	400	kHz

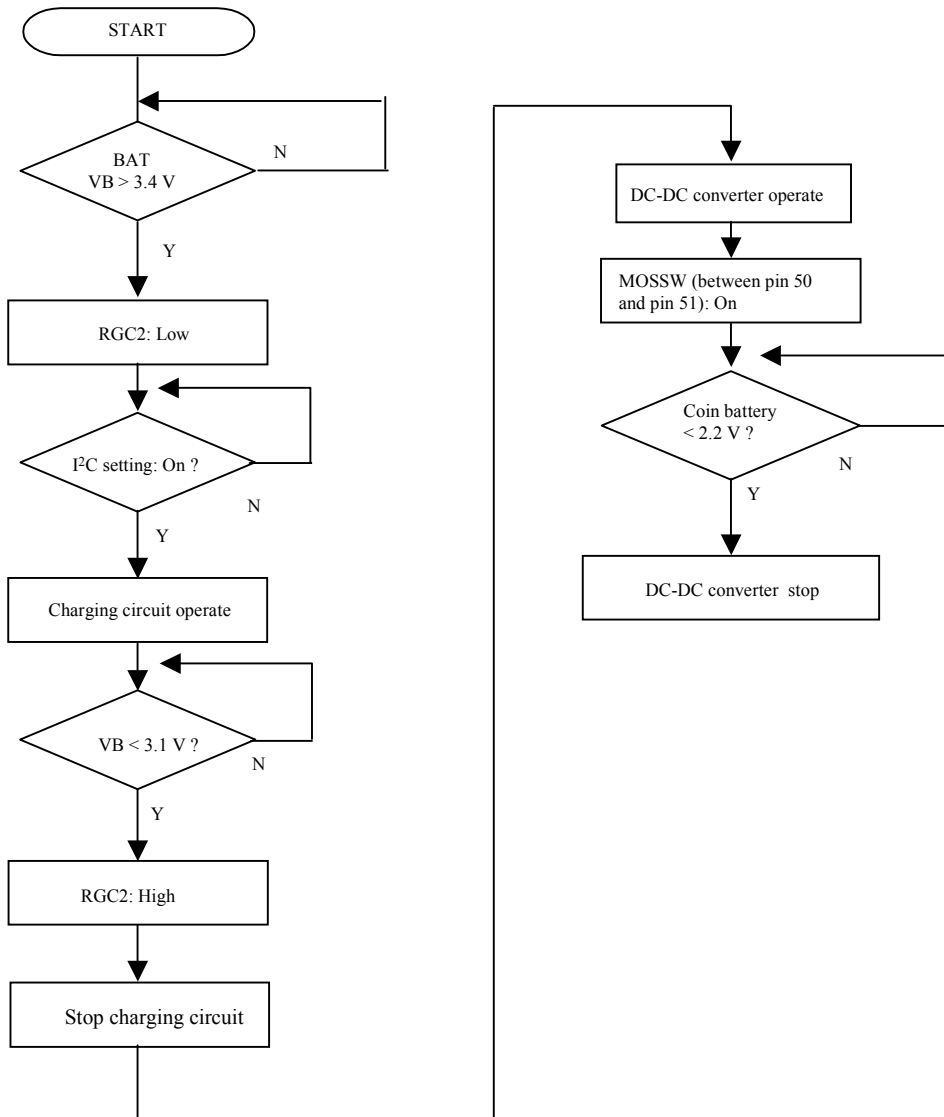
## ■ Technical Data (continued)

### 4. Backup circuit operation



- 1) Coin battery detection circuit monitors pin 49 voltage.  
When it becomes equal to or less than 2.2 V, it make switch 1 and boost DC-DC converter off.  
(To prevent over-discharge of the backup battery.)
- 2) Output voltage of regulator can set freely between 2.7 V and 3.3 V when set VB: 3.6 V through adjustment of feedback voltage of pin 47.
- 3) Boost DC-DC converter output is set 3.2 V internally.
- 4) Switching to ch.2 is exercised by the intra-judging circuit.

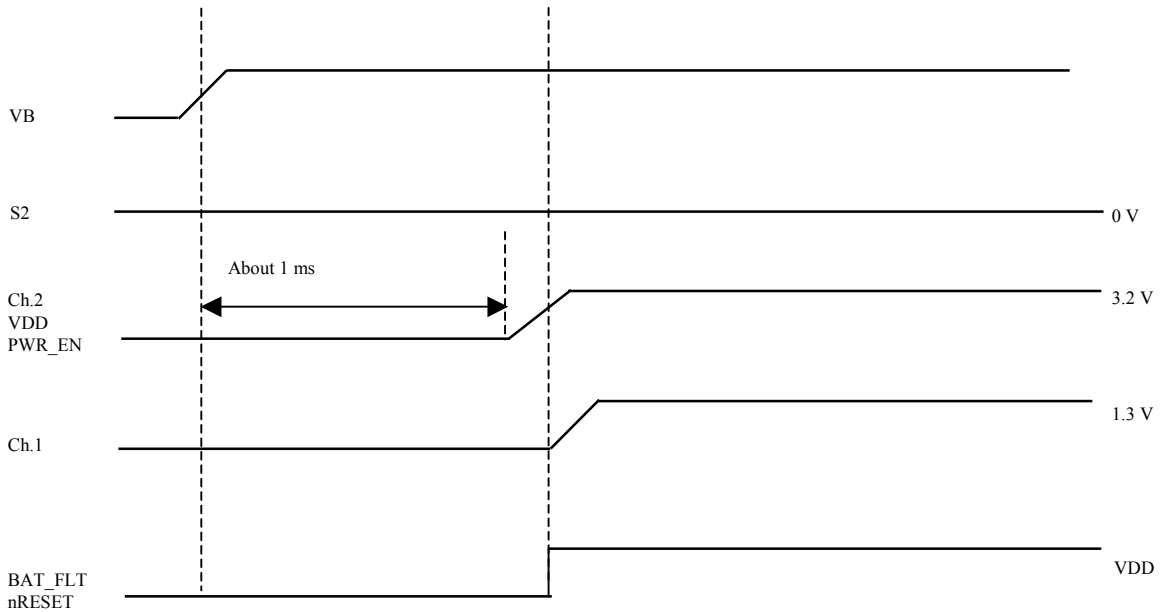
■ Technical Data (continued)  
 5. Backup circuit charging flow



■ Technical Data (continued)

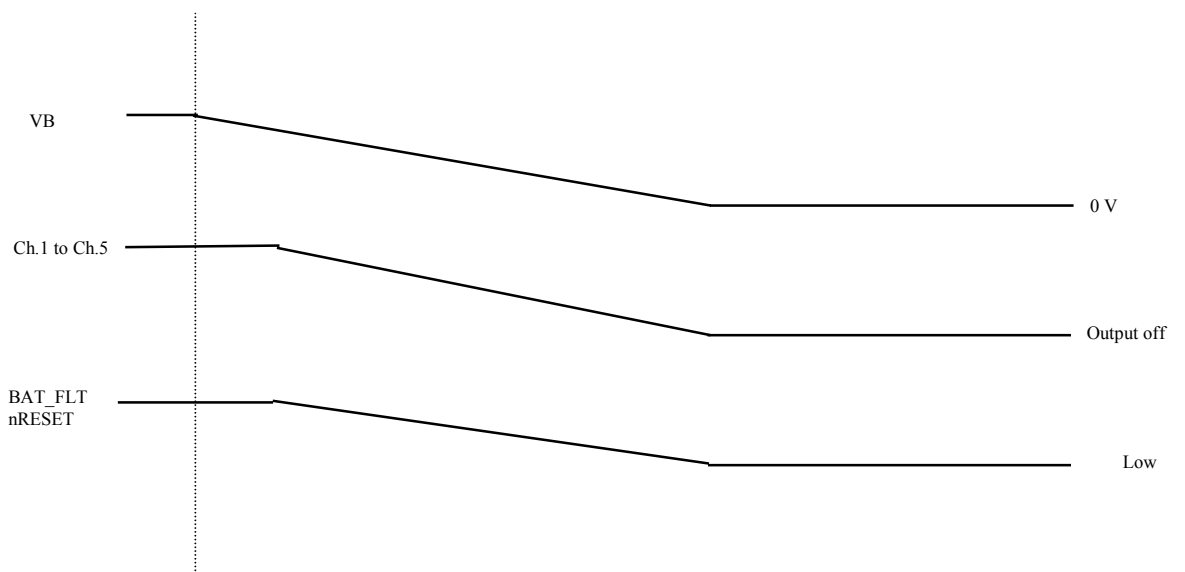
6-1. Sequence chart (1)

- Power on sequence



Power on reset operation depend on about 2 V.  
Ch.2 start up from this timing after 1 ms operation.

- Power off sequence

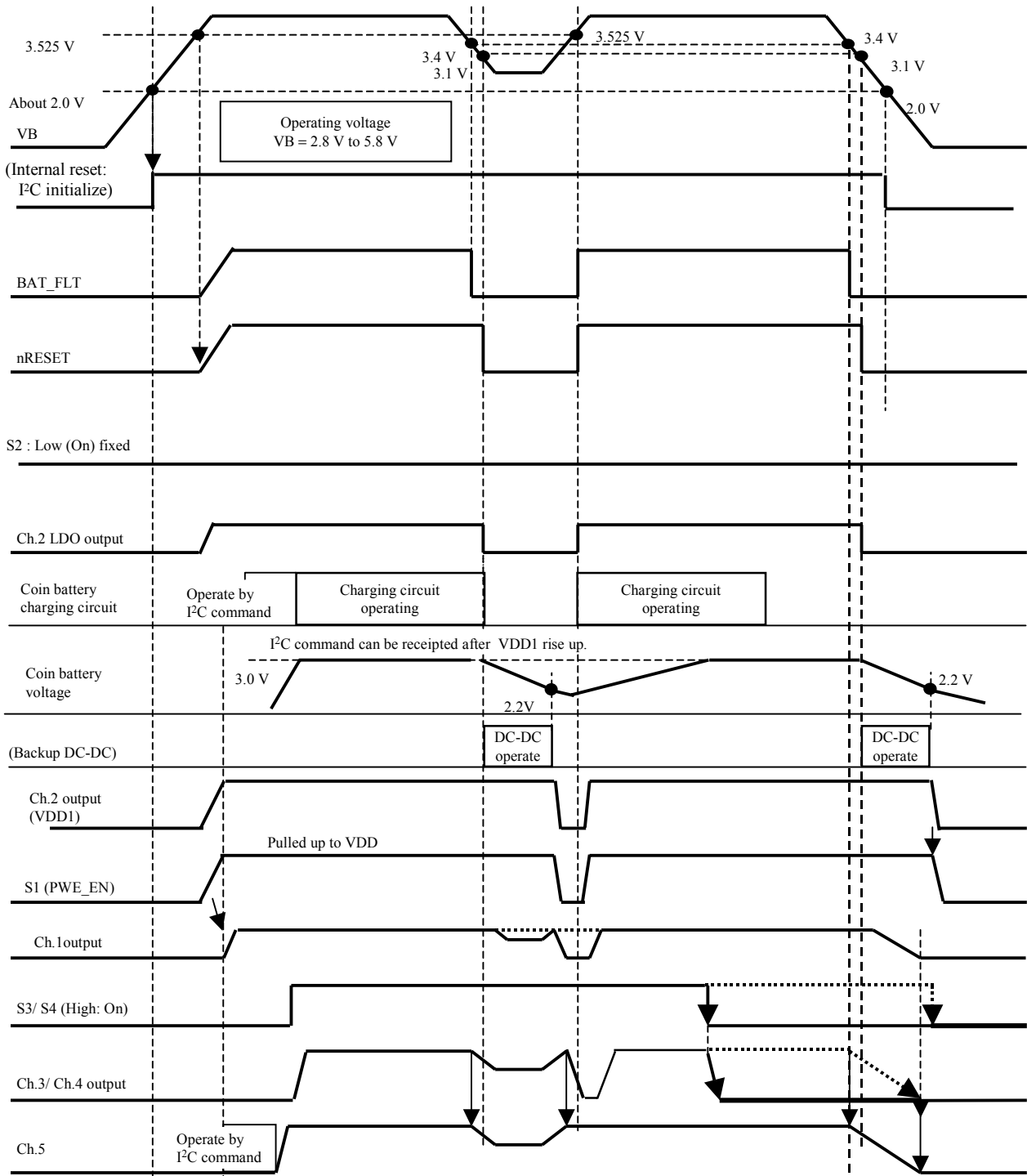


Note) \*: Power supply for input/output part is supplied from VDD, fall down same time as VDD.

■ Technical Data (continued)

6-2. Sequence chart (2)

- All channel operating sequence

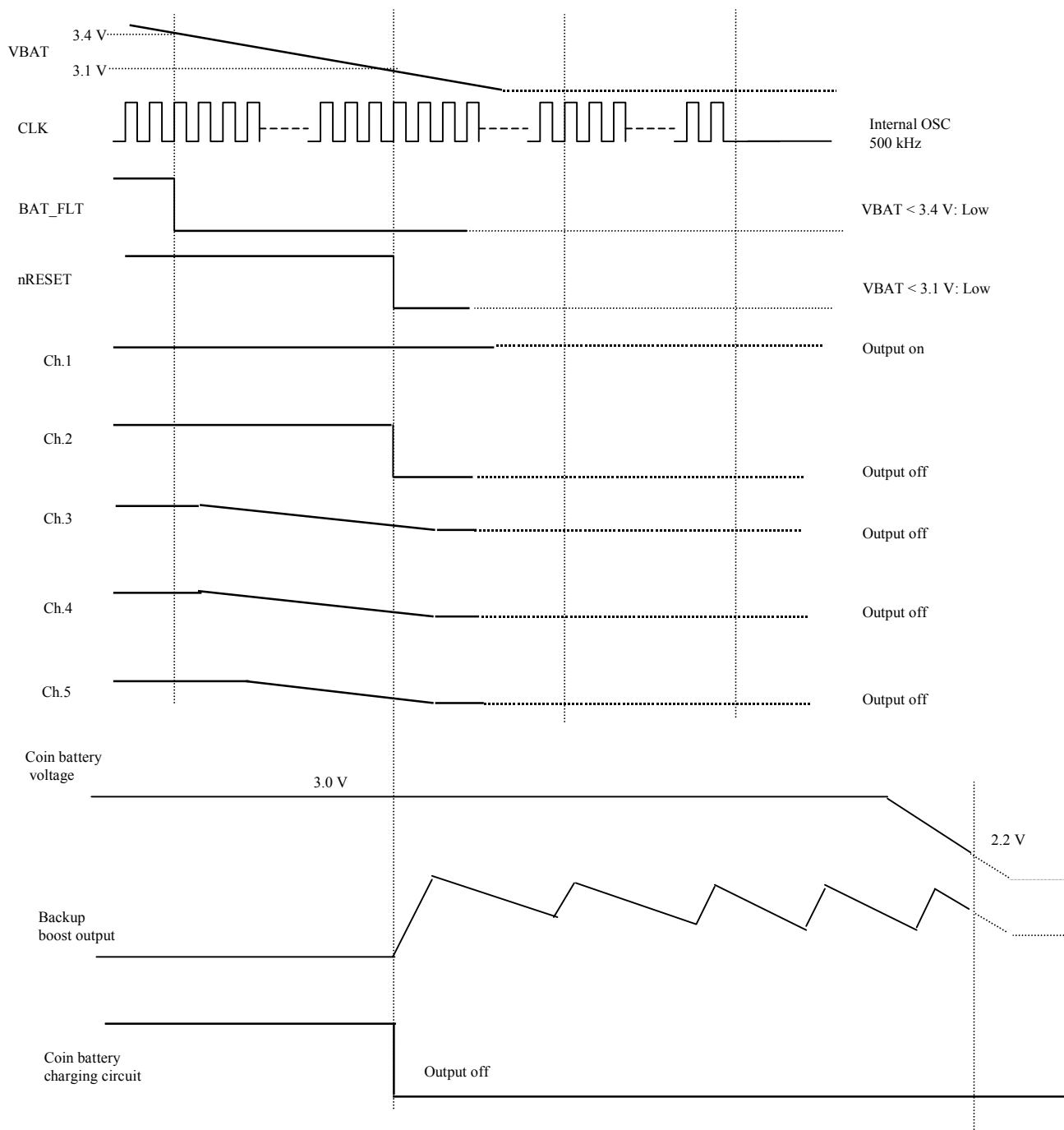


Note) \*: When power supply turns on, ch.2 output and charging circuit keep to off mode until battery voltage (VB) goes up to 3.525 V, even though I²C command can be received after power on reset operation.

### ■ Technical Data (continued)

#### 6-3. Sequence chart (3)

- Low battery detection sequence



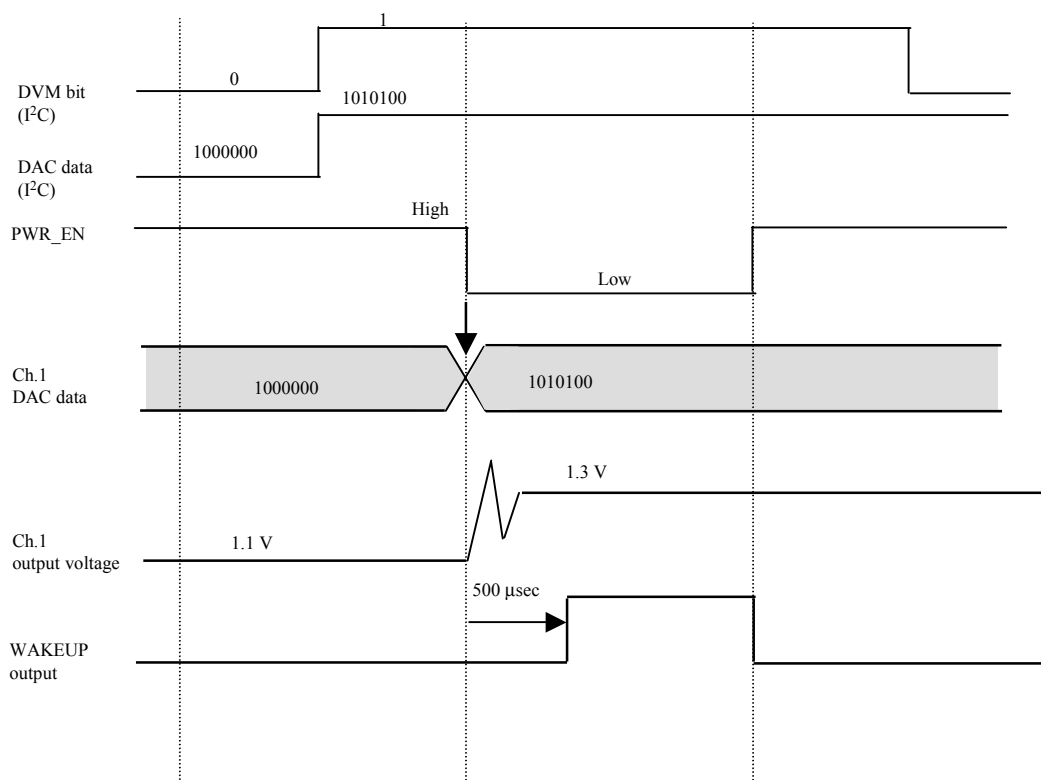
- BAT\_FLT output changes low to high when battery voltage becomes over 3.525 V.
- When RESET button is pressed, make RESET of PMIC pin output only low. Each power supply should be kept same.

## ■ Technical Data (continued)

### 6-4. Sequence chart (4)

- Ch.1 Sequence in case of switching ch.1 output voltage (Non real time mode)

DVM bit setting for serial data allows for judgment on which switching mode to be taken, CORE\_I voltage or normal on/off.



1) 500 μsec waiting time is controlled using internal oscillator (500 kHz), and counter after PWR\_EN changes high to low, and wakeup changes low to high.

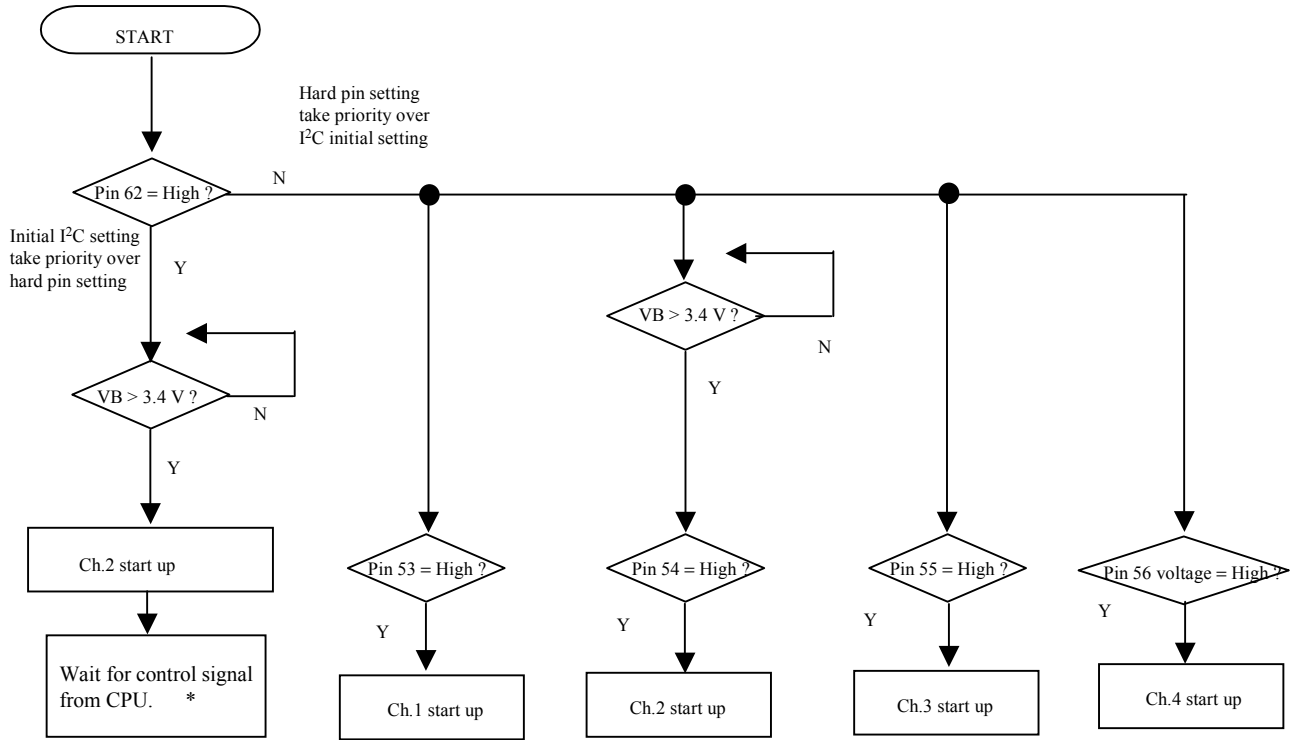
2) Internal resistor hold final data.

If you want to operate in voltage switching mode and normal on/off setting, need to set DVM bit '0' by sending I<sup>2</sup>C data.

■ Technical Data (continued)

6-5. Sequence chart (5)

- PMIC start up



Note) \*: Ch.2 only turns on with initial setting, when I<sup>2</sup>C start up is prioritized.  
 Ch.5 is can be controlled only by I<sup>2</sup>C command. ( Initial setting: Off )

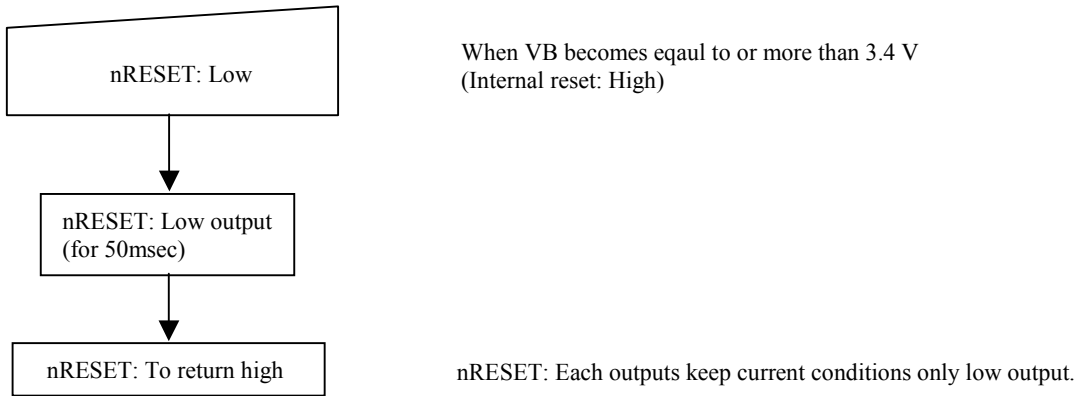
Hard pin setting table

	On	Off
Ch.1	High	Low
Ch.2	Low	High
Ch.3	High	Low
Ch.4	High	Low

■ Technical Data (continued)

6-6. Sequence chart (6)

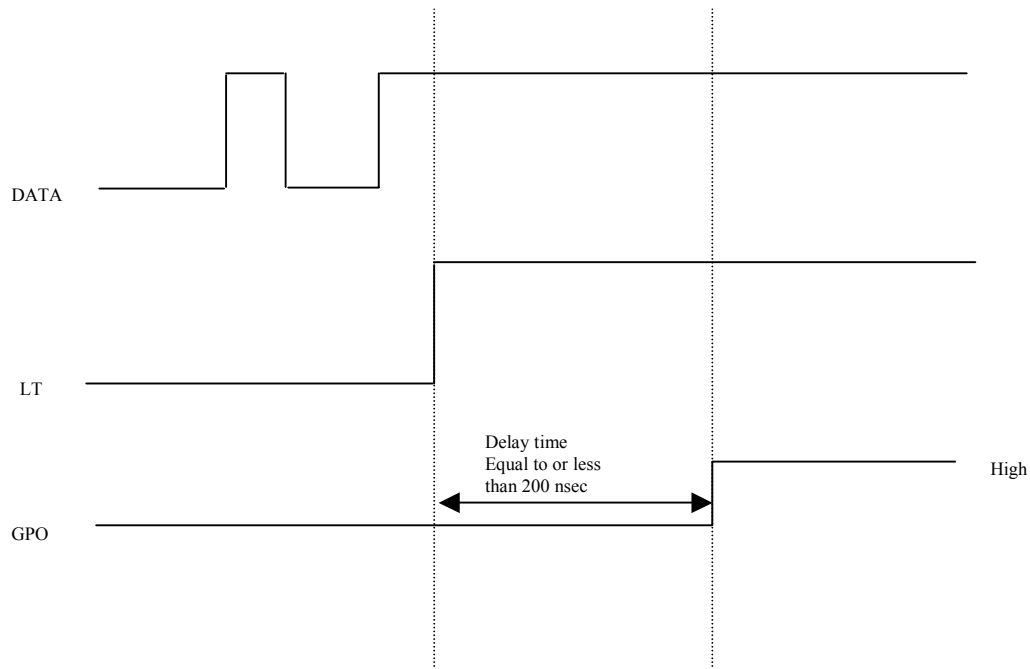
- nRESETOUT input



6-7. Sequence chart (7)

- GPO operation

Output setting change low to high



Delay in output setting of change low to high is same.

### ■ Technical Data (continued)

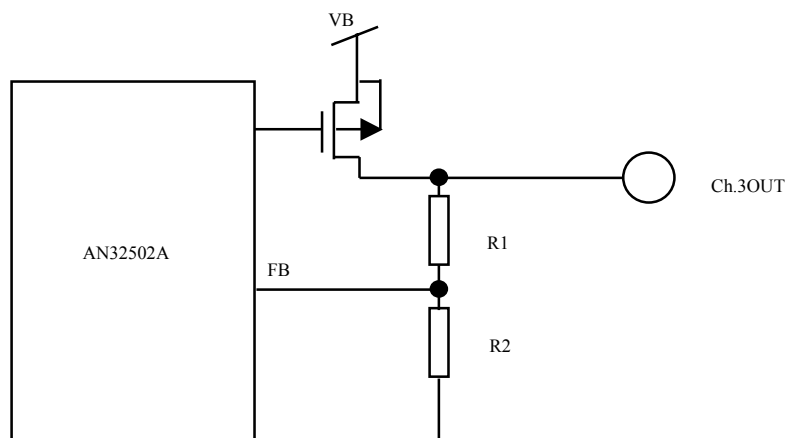
#### 7-1. Voltage setting (1)

$V_{REF}$  of each REG is set as listed below.

	$V_{REF}$ (reference value)
Ch.1	1.08 V
Ch.2, Ch.3, Ch.5	1.0 V
Ch.4	1.07 V

When changing output voltage, find a resistance ratio ensuring that feedback voltages become these values.

Example: Ch.3



$$\text{Ch.3OUT} = V_{REF} \times \frac{R1 + R2}{R2}$$

Note) \*: This  $V_{REF}$  (reference value) is value in case of design.

## ■ Technical Data (continued)

### 7-2. Voltage setting (2)

#### 1) Ch.1 voltage setting from I<sup>2</sup>C

Ch.1 voltage setting is possible with 7-bit DAC.

Sub Address 00H	Ch.1 output voltage	Ch.1 V <sub>REF</sub> (reference value)
6CH	1.0 V	0.83 V
80H	1.1 V	0.92 V
A8H	1.3 V	1.08 V

Refer to sheet No.17 for I<sup>2</sup>C serial setting list.

Refer to sheet No.25 for ch.1 voltage change procedure.

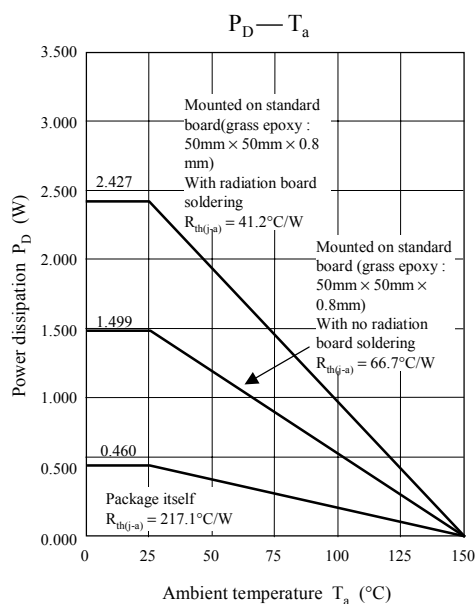
These values are based on the premise that feedback resistance values of ch.1 are identical with the ones described on the block diagram.

When this resistance ratio differs, the above-listed setting values vary.

Note)\*: This V<sub>REF</sub> (reference value) is value in case of design.

#### • Power dissipation of package HQFN064-P-0808

- 1) With no radiation board soldered, there are no other patterns than the ones to be connected from each pin to the pin lands on the outer rim of PCB.
- 2) With radiation board soldered, another pattern of 4mm is added on the rear side of the IC.





## ■ Application Notes

### 1. Overview

This IC is a power management IC developed for Intel PXA250/ 210 and features as follows:

- A single chip IC onto which to integrate ch.2 DC-DC converter, ch.3 LDO and an interface circuit for PXA250/210
- Charging circuit for backup battery, boost DC-DC converter and back-up MOS switch are built in.
- Built-in ch.5 general-use output and 1 input/2 outputs analog switch are built in.
- A high efficient synchronous rectifier circuit is employed for DC-DC converter.
- Power supply for PXA250/ 210 core can be controlled by software (I<sup>2</sup>C interface).  
(Intel Reference Number: 278530-001 Core voltage changing sequence described on the document is available.)
- Small-size high Pd leadless package adopted (HQFN-64)

### 2. Function overview

- Ch.1 (Step-down DC-DC converter for CPU core)  
Output voltage range: 0.5 V to 1.7 V to be set up with DAC (I<sup>2</sup>C)  
Synchronous rectifier type  
Maximum current : 600 mA  
Operating frequency: 500 kHz
- Ch.4 (Step-down DC-DC converter)  
Output voltage range: 1.8 V to 3.3 V  
Synchronous rectifier type 100% duty operation guaranteed  
Maximum current : 500 mA  
Operating frequency: 500 kHz
- Ch.2, Ch.3, Ch.5 (LDO)  
Output voltage range: 1.8 V to 3.3 V  
Maximum current : 500 mA

Note) \*: Maximum current conforms to a test circuit condition described on the specification.

#### 1) DC-DC converter for backup (Boost circuit)

Output voltage: 3.2 V

Output current: 2 mA (typical) 10 mA (maximum)

Built-in output switch MOS (Automatic on/off by main power supply)

Built-in charger circuit for backup battery is built in.

#### 2) Input/ output-related items

Input	I <sup>2</sup> C interface	Output	nRESET
	PWR_EN		
	TRIG		BAT_FLT
	External reset input		WAKEUP
	PS		General purpose output (Ch.5 I <sup>2</sup> C control)
	Analog switch input		Analog switch output

## ■ Application Notes (continued)

### 3. System block diagram

The block diagram for this IC is shown on figure 3 – 1.

- Output-stage MOSFETs for ch.1 to ch.5 are fit externally for its nature general purpose.
- Output current for each channel is a typical value for an evaluation board.
- Therefore, select an external MOSFET to meet the conditions needed in the application.
- Output voltages for ch.2 to ch.5 are available in the range of 1.5 V and more with constant setting of external feedback circuit.

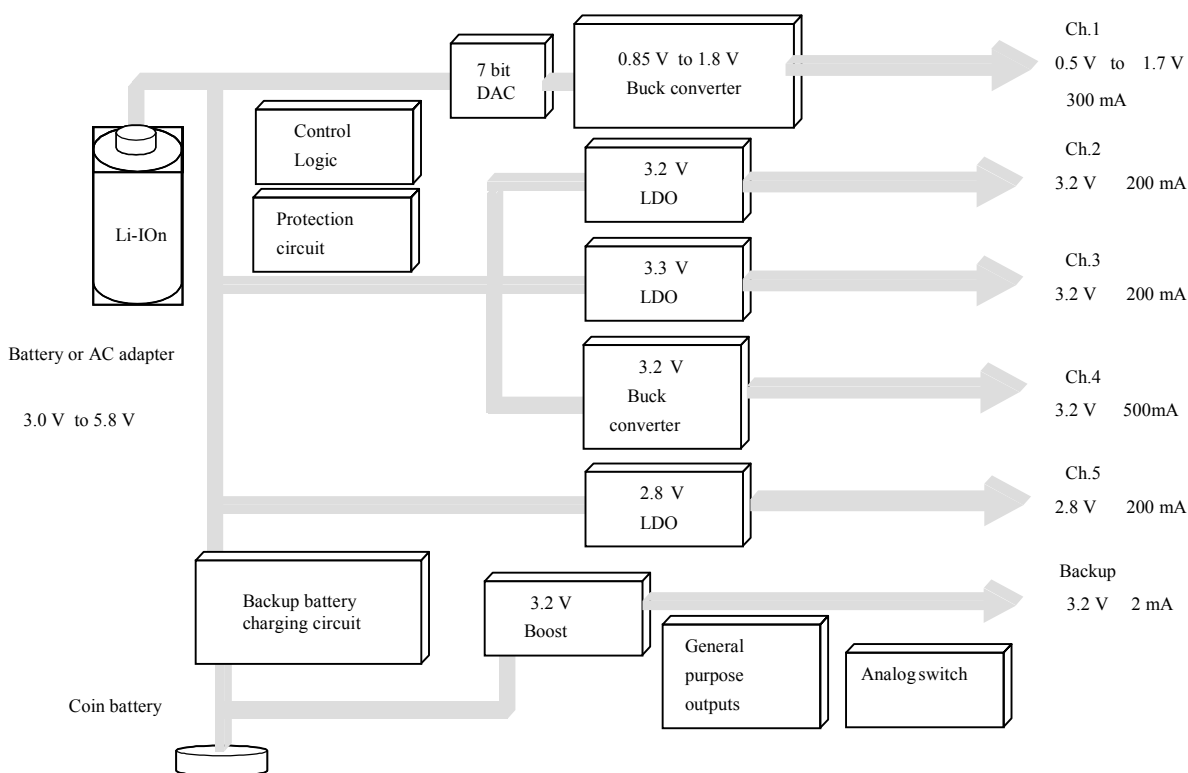


Figure 3 – 1

### 4. Output voltage setting

Output voltage of each channel is determined by the following equation.

$V_{REF}$  is an internal reference voltage and differs from every each channel differs values. Refer to table 4 – 1.

Ch.1 reference voltage can be controlled by DAC. 1.08 V is an initial setting value (DAC data '1010100').

A reference voltage can be set with 8.36 mV/ step in the range of 0.38 V to 1.45 V.

Output voltage change is multiplied by  $(R1+R2)/R2$ . For example, when output is set to 1.3 V, the output is able to adjusted by the step of about 10 mV.

$$V_O = V_{REF} \times \frac{(R1 + R2)}{R2}$$

## ■ Application Notes (continued)

### 4. Output voltage setting (continued)

- $V_{REF}$

Table 4 – 1

	$V_{REF}$ (V)
Ch.1	1.08
Ch.2, Ch.3, Ch.5	1.0
Ch.4	1.07

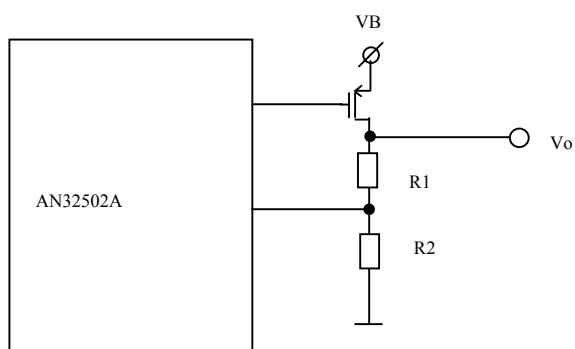


Figure 4 – 1

### 5. On/off control

- Ch.1 is controlled by the hard pin (Pin 54) only.
- Ch.2, ch.3 and ch.4 are controlled by both the hard pin and I<sup>2</sup>C command.  
PS pin (Pin 63) setting allows for which to prioritize.  
High: I<sup>2</sup>C take priority over hard pin.  
Low: Hard pin priority over I<sup>2</sup>C
- Ch.5 is controlled by I<sup>2</sup>C only.  
Initial setting at time of applying supply voltage turns off.

Table 5 – 1

	Pin control	I <sup>2</sup> C control
Ch.1	○	
Ch.2	○	○
Ch.3	○	○
Ch.4	○	○
Ch.5		○

## ■ Application Notes (continued)

### 6. Explanation of operation

- Ch.1

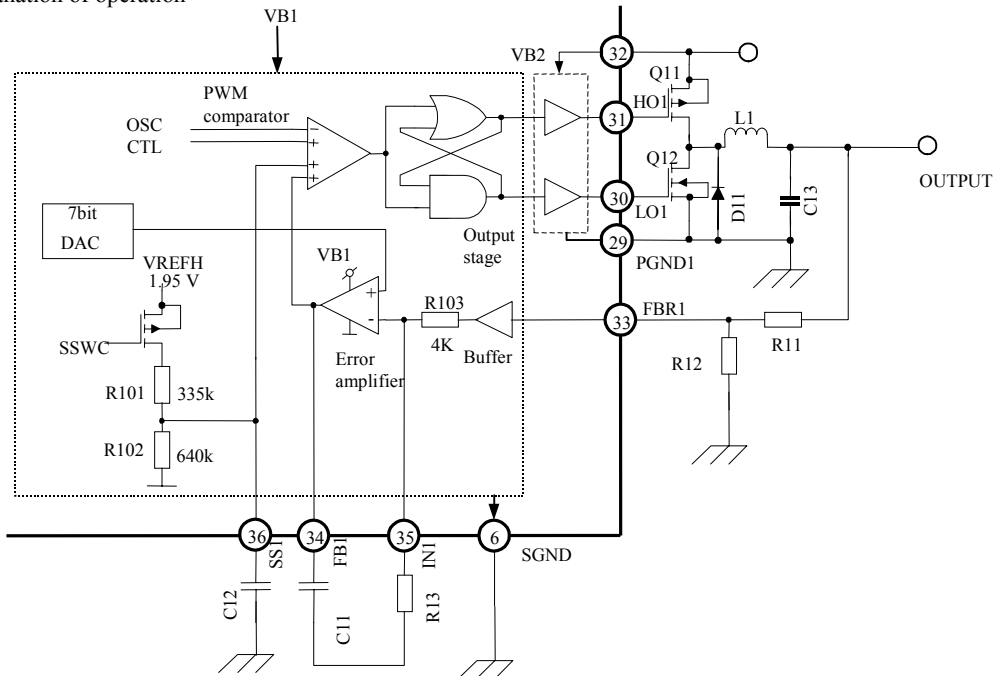


Figure 6 – 1

Ch.1 is a step-down DC-DC converter. Figure 6 – 1 shows an internal block configuration.

#### 1) Output setting

Built-in a 7-bit DA converter, it allows you to set a reference voltage by the step of about 8.36 mV. In comparison between this reference voltage and FBR1 pin input voltage, a feedback control functions. Therefore, output voltage is determined by the following equation:

$$V_{\text{OUT}} = \frac{R11 + R12}{R12} \times V_{\text{REF}}$$

$V_{\text{REF}}$  is 1.08 V of an initial setting. (DAC data '1010100')

A voltage variable range is 0.38 V to 1.45 V, allowing for setting with 8.36 mV/ step (value in case of design).

Refer to figure 6 – 3 for linearity of DAC.

When high precision is required for output voltage, use a high precision resistor for R11 and R12, respectively.

R11 and R12 are influenced not by absolute precision, but by relative precision. Therefore, when using a resistor of  $\pm 0.5\%$  precision resistor, output voltage varies for maximum  $\pm 1\%$ .

#### 2) PWM comparison block

PWM comparator controls the on period of output pulse depending on input voltage.

Set output voltage to "High" and power on N-channel output MOS while triangular wave oscillation voltage is lower than pin 36 (SS1) and pin 34 (error amplifier output) voltages.

Maximum duty is determined by maximum voltage of triangular oscillation and set voltage of pin 36 (SS1). This IC is set to about 88%.

Insertion of a capacitor between pin 36 and GND allows for a soft start operation enabling a gradual elongation of on period of output pulse and making overshoot and undershoot smaller at the time of startup. The constant at the soft start is determined by internal R101 and an external capacitor of pin 36.

## ■ Application Notes (continued)

### 6. Explanation of operation (continued)

#### • Ch.1 (continued)

#### 3) Output voltage

Output voltage from HO1 and LO1 is applied with a dead time of 80 nsec so that simultaneous on of Q11 and 12 may not cause a through-current to flow. Refer to figure 2 for timing.

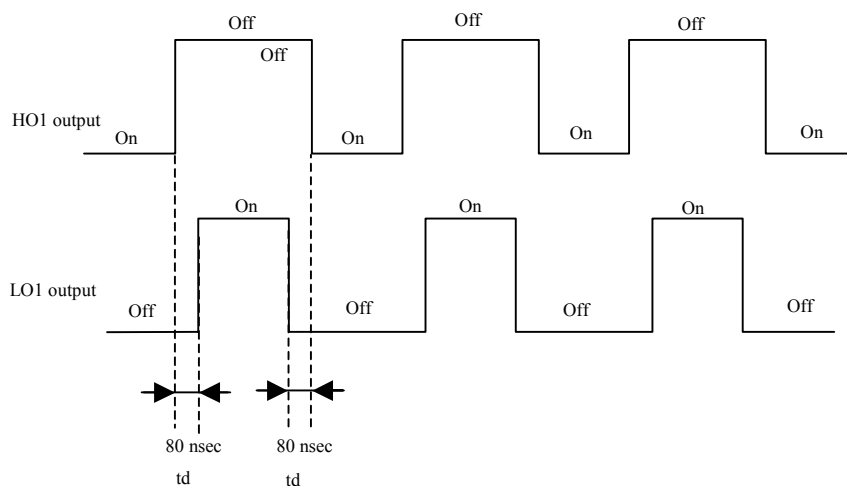


Figure 6 – 2

#### 4) Error amplifier

Error amplifier response characteristics are determined by the feedback C11 and R13 the built-in R103 between pin 34 and pin 35.

R13: 10 k $\Omega$

C11: 0.01  $\mu$ F

It is recommended to above

In actual pattern layout, it is recommended to make C11 and R13 lines as short as possible so as to reduce effect by noise.

#### 5) On/off control

Ch.1 can be controlled only by pin 54.

Control by serial data is unavailable.

#### 6) Power supply and GND

Power is supplied from pin 32 (VB2) only for the output drive stage and from pin 46 (VB1) for other parts. GND is connected for pin 29 (PGND1) only for the output drive stage. Other parts are connected to the signal system GND of pin 6 (SGND).

Connect Q12 source, D11 anode, C13GND with thick wires as near to pin 29 as possible.

#### 7) Peripheral parts

The characteristics of output capacitor C13 has an effect on output transient response characteristics.

It is recommended to use a high ESR capacitor like our SPCAP.

It is also recommended to select the constant of 10  $\mu$ H for inductor L1 in the supply voltage range of this IC (2.8 V to 5.8 V) considering efficiency degradation caused by size and DC resistance.

■ Application Notes (continued)

6. Explanation of operation (continued)

- Ch.1 (continued)

8) DAC linearity (Ch.1)

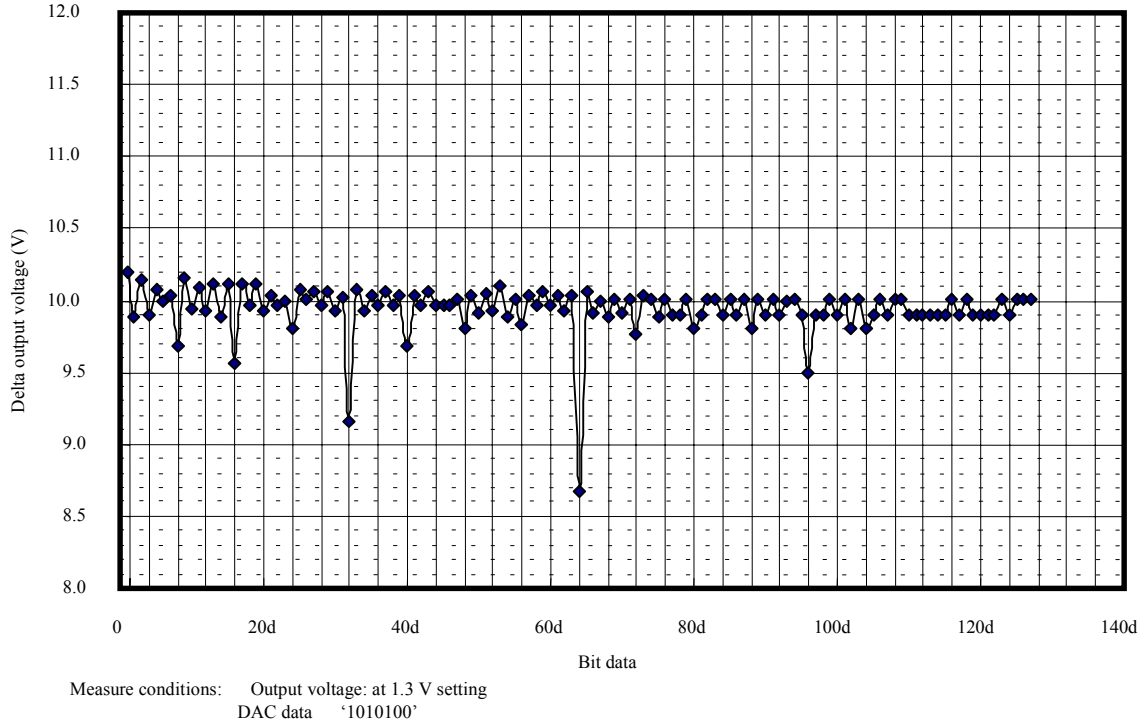


Figure 6 – 3

9) Soft start timing chart

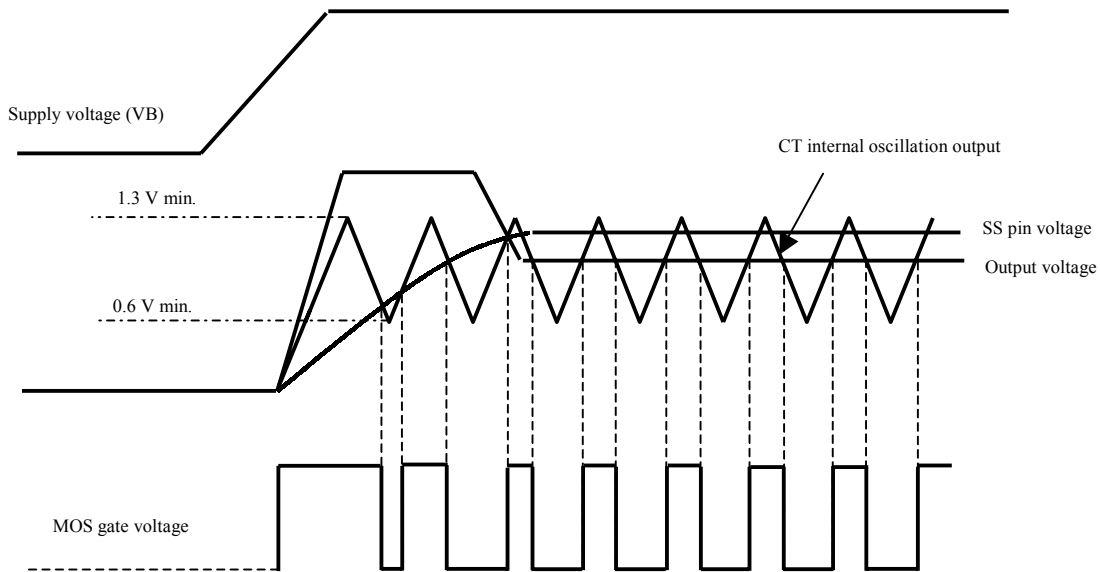


Figure 6 – 4

Oscillation frequency of internal oscillation circuit is determined by the capacitor between pin 4 and GND and the resistor between pin 5 and GND. Oscillation frequency is 500 kHz at capacitor 33 pF and resistor 33 kΩ (estimated constant).

## ■ Application Notes (continued)

### 6. Explanation of operation (continued)

#### • Ch.2

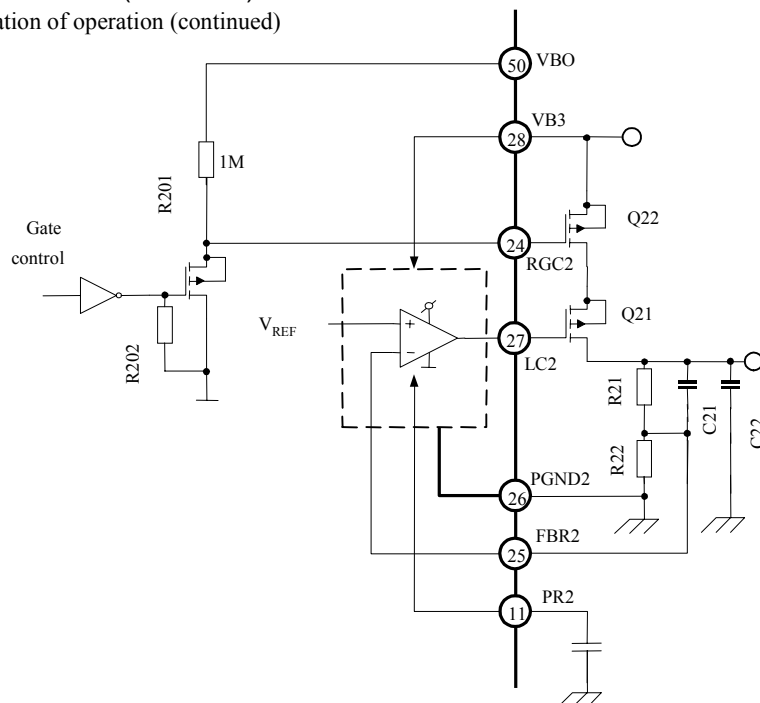


Figure 6 – 5

Ch.2 is a linear regulator. Figure 6 – 5 shows the ch.2 internal block configuration.

It runs a feedback control comparing the internal  $V_{REF}$  with pin 25 voltage. Output voltage is determined by the following equation.

$$V_{out} = \frac{R21+R22}{R22} \times V_{REF}$$

Internal  $V_{REF}$  is set to 1.0 V.

Ch.2 is intended to be used in the memory circuit and is automatically switched to the backup power supply circuit when supply voltage is lowered. (When VB1 gets below 3.1 V, ch.2 off, Q22 off and the backup power supply circuit on.)

Q22 functions as a switch that would prevent current from reverse-flowing from output to source when switching to a backup power supply circuit.

When power supply voltage (VB1) is equal to or less than 3.1 V, gate control signal becomes “High” and Q22 gate voltage becomes equal to backup for supply voltage.

VBO (3.1 V to 3.3 V) and is switched off. Simultaneously, a backup power supply circuit is actuated to keep output voltage to the constant level.

This switching response time is determined by Q22 gate capacitance and R201.

Output voltage is likely to drop at the switching time depending on the main power supply off conditions. In this case, connect a resistor of 500 kΩ between pins 24 and pin 50 so that R201 resistance can be kept small equivalently and response time is able to kept short.

#### 1) Rush current at power supply input

This regulator built-in a circuit limiting rush current at power supply input. Insertion of a capacitor between pin 11 (PR2) and GND allows to control rush current to approx. 500 mA. (At supply voltage: 5.8 V, C22 = 33 μF)

#### 2) On/off control

This regulator is able to on/off control with a serial data and pin 55.

### ■ Application Notes (continued)

#### 6. Explanation of operation (continued)

- Ch.2 (continued)

#### 3) Power supply and GND

Power supply of this regulator is pin 28 (VB3) and GND is pin 26 (PGND2).

$V_{REF}$  block is constituted by VB1 and SGND.

- Ch.3

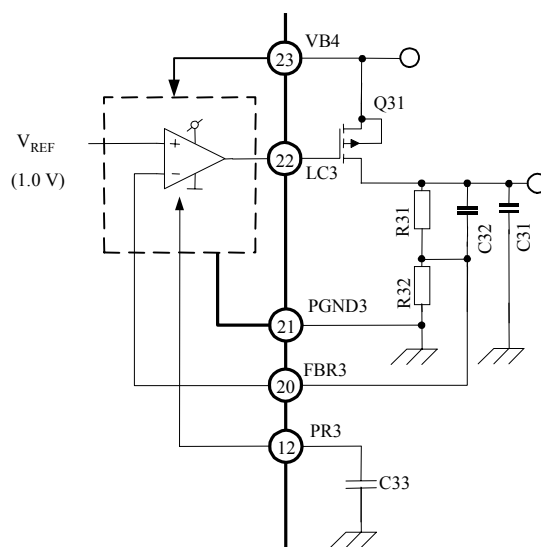


Figure 6 – 6

Ch.3 is a linear regulator circuit that is configured identically with ch.2 except for a backup switching circuit.

Figure 6 – 6 shows internal block configuration of ch.3.

Output voltage is determined by the following equation.

$$V_{out} = \frac{R31 + R32}{R32} \times V_{REF}$$

Internal  $V_{REF}$  is 1.0 V.

External capacitor of pin 12 is intended to control rush current on power supply.

#### 1) On/off control

This regulator is able to on/off control with serial data and pin 56.

#### 2) Power source and GND

Power supply of this regulator is pin 23 (VB4) and GND is pin 21 (PGND3).

$V_{REF}$  block is constituted by VB1 and SGND.

## ■ Application Notes (continued)

### 6. Explanation of operation (continued)

#### • Ch.4

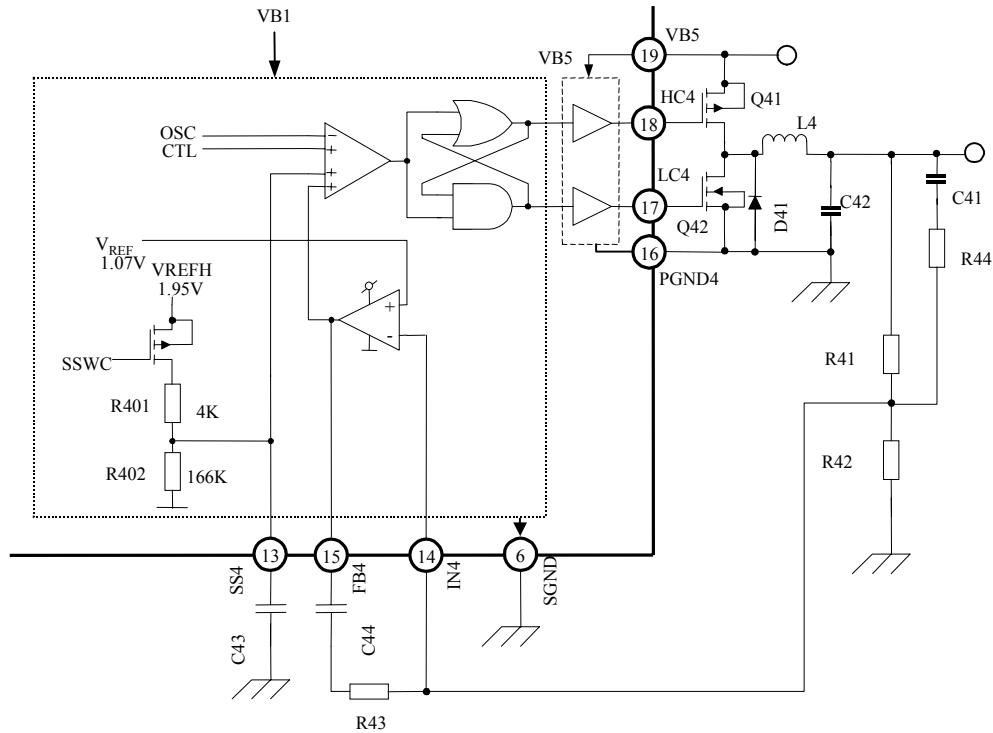


Figure 6 – 7

Ch.4 is a step-down DC-DC converter of synchronous rectifying type.

Figure 6 – 7 shows internal block configuration of ch.4.

Output voltage is determined by the following equation.

$$V_{out} = \frac{R41 + R42}{R42} \times V_{REF}$$

$V_{REF}$  is 1.07 V initially.

When high precision is required for output voltage, use a high precision resistor for R41 and R42, respectively.

R41 and R42 are influenced not by absolute precision, but by relative precision. Therefore, when using a resistor of  $\pm 0.5\%$  precision resistor, output voltage varies for maximum  $\pm 1\%$ .

#### 1) PWM comparison block

PWM comparator controls the on period of output pulse depending on input voltage.

Set output voltage to “High” and power on N-channel output MOS while triangular wave oscillation voltage is lower than pin 13 (SS4) and pin 14 (error amplifier output) voltages.

This circuit is able to operation up to maximum duty of 100%.

Insertion of a capacitor between pin 13 and GND allows for a soft start operation of gradually widening on period of output pulse at startup time so that overshoot and undershoot at startup time.

The constant at the time of soft start is determined by the internal R401 and the external capacitor of pin 13.

C41 and R44 are the additional components to improve transient response characteristics coming up when load current is suddenly changed.

On the condition of this test board, the control output voltage on sudden load change of 0 mA to 500 mA (changing time 10  $\mu$ sec)

Can be controlled approximately to 90 mV.

## ■ Application Notes (continued)

### 6. Explanation of operation (continued)

#### • Ch.4 (continued)

#### 2) Output voltage

Output voltage from HC4 and LC4 is applied with a dead time of 80 nsec so that simultaneous on of Q41 and 42 may not cause a through-current to flow. Refer to figure 6 – 8 for timing.

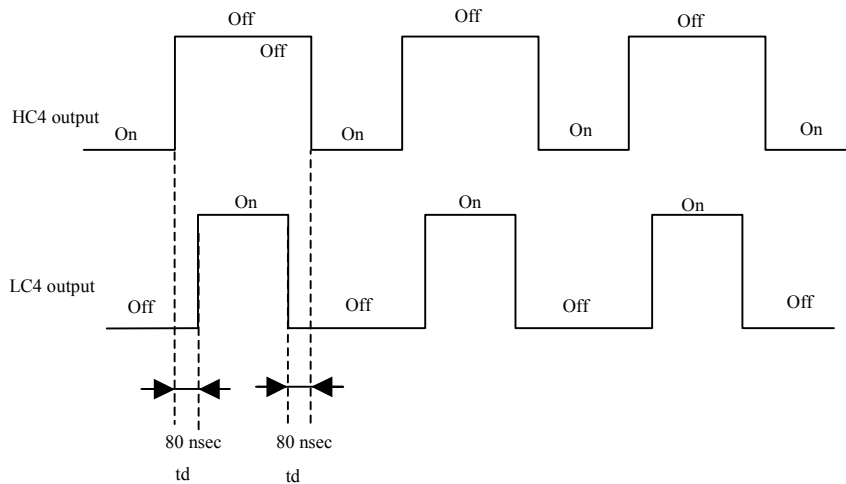


Figure 6 – 8

#### 3) On/off control

Ch.4 is able to on/off control by pin 57 and serial data.

#### 4) Power supply voltage and GND

Power is supplied from pin 19 (VB5) only for the output drive stage and from pin 46 (VB1) for other parts.

GND is connected from pin 16 (PGND4) only for output drive stage. Other parts are connected to the signal system GND of pin 6 (SGND). Q41 source, D41 anode and C42GND side should be connected with a fat wire as near to pin 16 as possible.

#### 5) Peripheral parts

The characteristics of output capacitor C42 has an effect on output transient response characteristics.

It is recommended to use a high ESR capacitor like our SPCAP.

It is also recommended to select the constant of 10  $\mu$ H for inductor L4 in the supply voltage range of this IC (2.8 V to 5.8 V) considering efficiency degradation caused by size and DC resistance.

## ■ Application Notes (continued)

### 6. Explanation of operation (continued)

- Ch.5

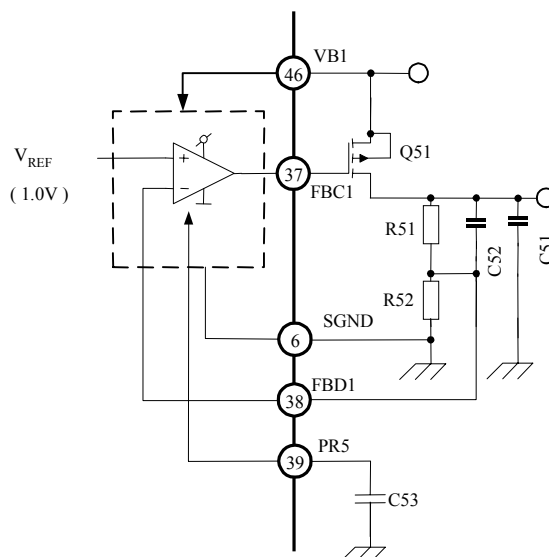


Figure 6 – 9

Ch.5 is a linear regulator circuit that is configured identically with ch.2 except for a backup switching circuit.

Figure 6 – 9 shows an internal block configuration of ch.5.

Output voltage is determined by the following equation.

$$V_{out} = \frac{R51 + R52}{R52} \times V_{REF}$$

Internal  $V_{REF}$  is 1.0 V.

External capacitor C53 of pin 39 is intended to control rush current on power supply.

#### 1) On/off control

This regulator is capable of on/off control only with serial data.

Initial setting turns off at IC startup.

#### 2) Supply voltage and GND

Power supply of this regulator is pin 46 (VB1) and GND is pin 6 (SGND).

$V_{REF}$  block constituted VB1 and SGND.

## ■ Application Notes (continued)

### 7. Backup charging current

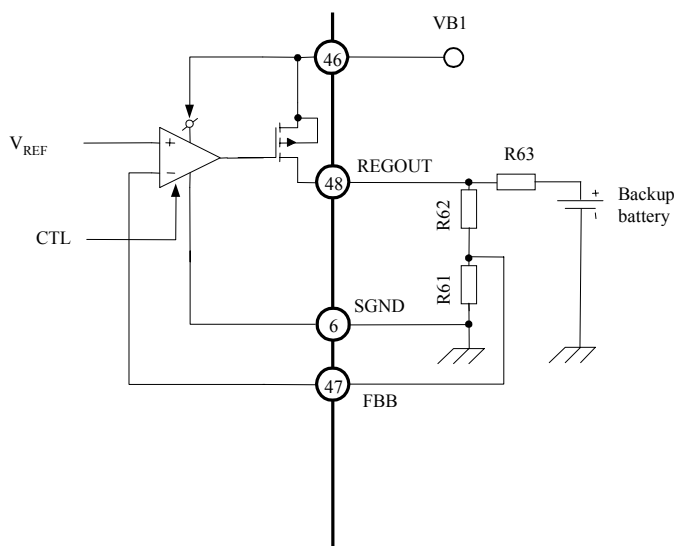


Figure 7 – 1

Figure 7 – 1 shows the configuration of a backup battery charging circuit.

The circuit configuration is identical with the general linear regulator and continues to supply charging current until a backup battery voltage reaches the voltage value shown by the following equation that is a balancing condition of regulator circuit.

$$\text{Backup voltage} = \frac{R61 + R62}{R61} \times V_{\text{REF}}$$

Internal  $V_{\text{REF}}$  is 1.0 V.

For a lithium ion coin battery, the above voltage is set to 3.0 V.

Determine R63 value according to the battery used, so as not to exceed maximum charging current specified.

This circuit is automatically switched off if the main battery voltage (Pin 46, VB1) becomes equal to or less than 3.1 V. Then, a backup boost circuit starts operating.

This circuit is able to setting on/off with serial data.

Initial setting turns off at startup.

Power supply for this circuit is supplied from pin 46 (VB1).

■ Application Notes (continued)  
8. Backup boost converter

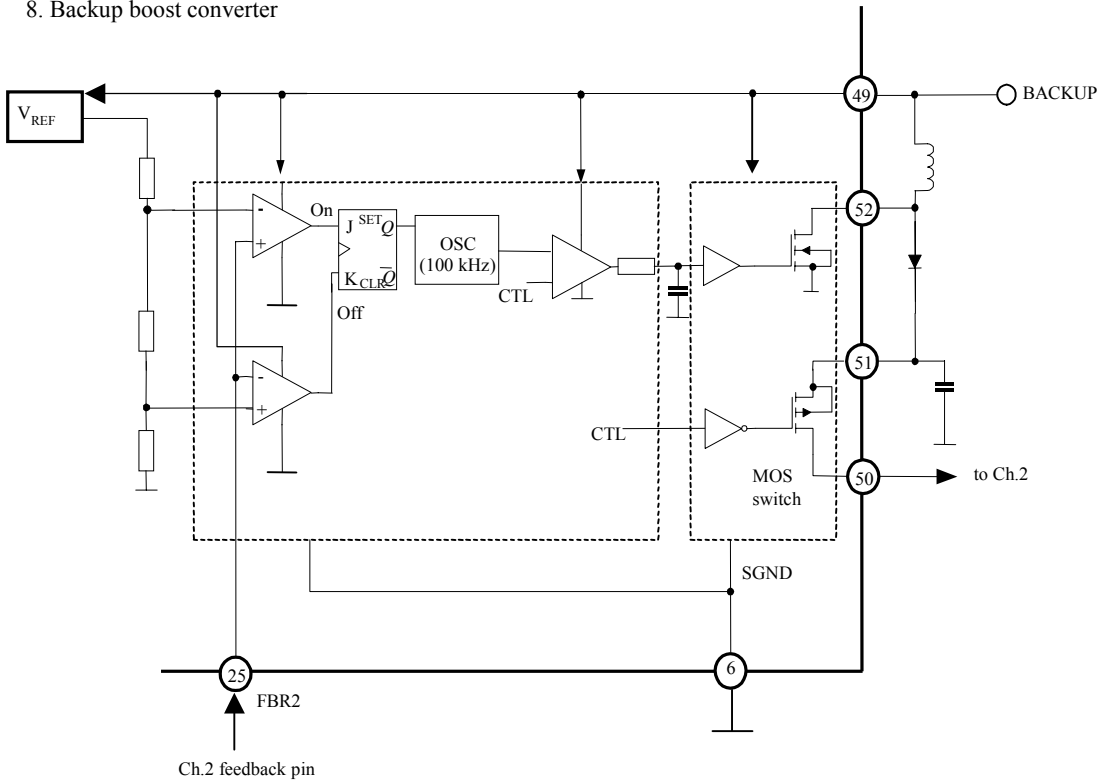


Figure 8 – 1

A backup boost circuit is boost circuit of burst mode operation.

Figure 8 – 1 shows internal block configuration.

When the main battery voltage becomes equal to or less than 3.1 V, this circuit starts operating.

Simultaneously, the internal MOS switch between pin 50 and pin 51 becomes on and this boost circuit output is supplied to the load circuit (memory circuit) on behalf of ch.2 regulator.

The internal oscillation circuit starts operating when pin 50 output voltage becomes below a low side detection threshold of equal to or less than 3.1 V and it stops operation when pin 50 output voltage becomes above a high side detection threshold of equal to or more than 3.3 V.

If a load current is constant, the output voltage goes down linearly. And when it reaches the above-stated low side detection voltage, the oscillating circuit operates again and starts charging an output capacitor. It stops operation when output voltage is equal to or less than 3.3 V. Then halting operation when output voltage reaches 3.3 V.

An output wave form of this circuit becomes a triangular wave variable between the thresholds of 3.1 V and 3.3 V.

For actual wave form, refer to figure 8 – 2 and figure 8 – 3.

Low and high side detection circuits are able to detect voltage by comparing pin 25 voltage with internal reference voltage.

Since pin 25 is a feedback pin for ch.2, its judging level varies according to ch.2 output voltage setting. The above-mentioned thresholds of 3.1 V and 3.3 V are based on output setting to 3.2 V.

This circuit automatically becomes off when a backup battery voltage is equal to or less than 2.2 V, so as to prevent a backup battery from being over-discharged.

1) On/off control

The circuit automatically operates when its main supply voltage (VB) is equal to or less than 3.1 V and its backup battery output voltage is equal to or more than 2.2 V.

2) Power supply and GND

All circuit blocks are supplied from pin 49 (backup) and pin 6 is for GND.

■ Application Notes (continued)

8. Backup boost converter (continued)

- Backup boost converter output waveform

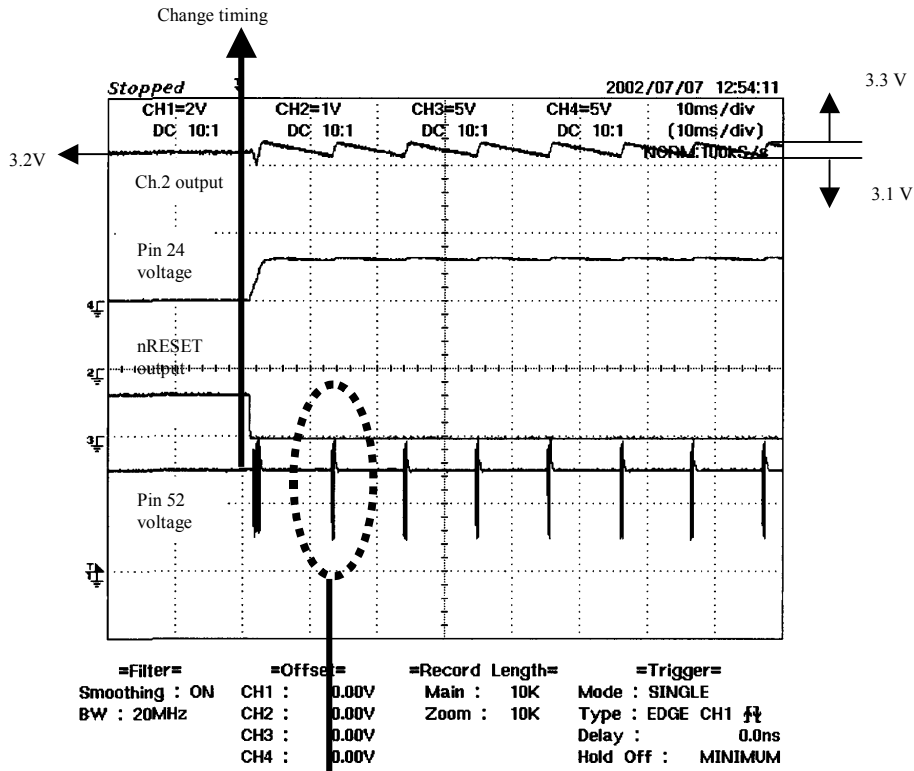


Figure 8 – 2

Switching at 100 kHz in the burst area.

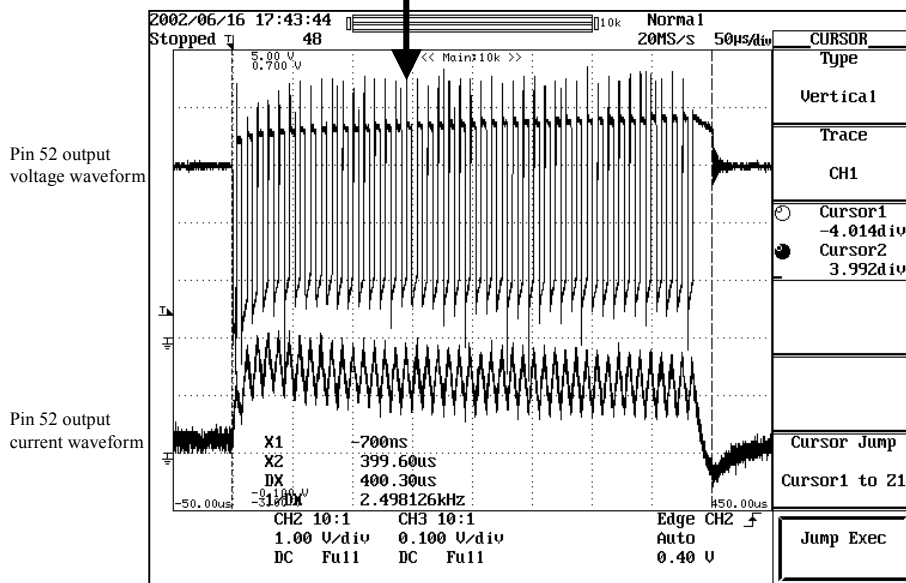


Figure 8 – 3

■ Application Notes (continued)  
 9. General purpose (GPO0 to GP05)

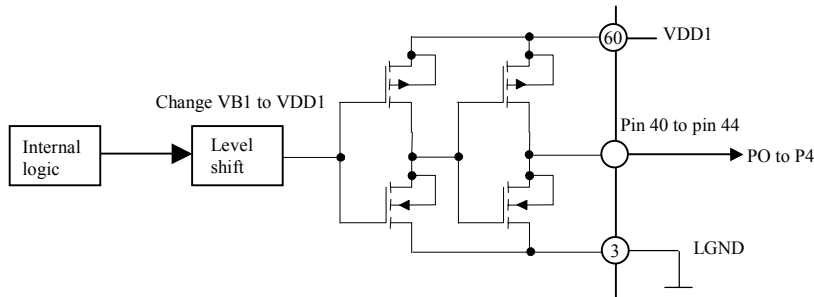


Figure 9 – 1

This IC is equipped with 5-system general purpose output pins.  
 Figure 9 – 1 shows circuit configuration. The output is CMOS mode.  
 Initial setting at startup is low for every outputs and high/ low settings are carried out by I<sup>2</sup>C control.  
 DC characteristics of output MOSFET become  $\Delta$ output voltage 0.3 V at 1 mA.  
 It is able to applied for on/off switch of external circuits or for driving LED. But care should be taken to voltage loss by the above-mentioned DC resistance of output MOSFET for actual application.

1) Power supply and GND

Power supply voltage of this regulator is pin 60 (VDD1) and GND is for pin 3 (LGND).  
 Internal logic block preceding level shift is VB1 and SGND.

10. Analog switch (VO1, VO2)

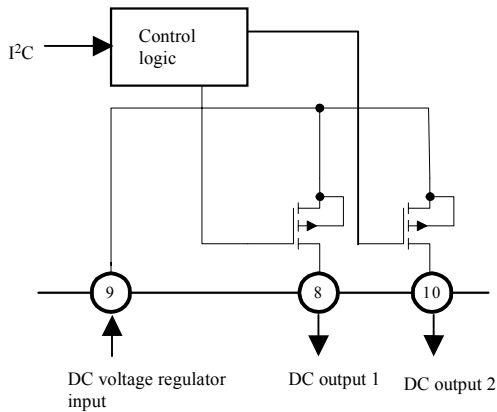


Figure 10 – 1

This IC built-in an analog switch of 1 input 2 outputs. This is pin 9 for input and pin 8 and pin 10 for outputs. Figure 1 shows circuit configuration. The MOS size between pin 8 and pin 9 is same as the one between pin 9 and pin 10.  
 P-channel MOSFET is connected between pin 8 and pin 9 and between pin 9 and pin 10. It is used as switch by logic control of gate. Suppose you have to supply the same stabilized supply voltage to both A and B circuit blocks. You can use this analog switch to halt B block to save the power while A block is operating.  
 Initial setting at power on turns off for both and on/off setting is able to done by I<sup>2</sup>C control.  
 DC resistance of switching MOS is about 1  $\Omega$ . Care should be taken to this influence for current and load fluctuation.



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