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Application Note

CS5516 and CS5520: Answers to Application Questions

by

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What determines the input span for the converter?

The input span of the CS5516/CS5520 AIN input signal is determined by a combination of the instrumentation amplifier gain (X25), the programmable amplifier gain setting (1,2,4 or 8), and the magnitude of the voltage between the VREF+ and VREF- pins. The voltage into the VREF pins can range from 2.0 to 3.8 volts and is determined by the resistor divider ratio selection of the resistor network which divides down the bridge excitation voltage. The CDB5516 and CDB5520 evaluation boards come with resistors which divide the excitation supply (nominally 10 volts total) down to 2.5 volts between the VREF+ and VREF- input pins. This 2.5 volt reference input is divided by the PGA gain setting and by the X25 instrumentation amplifier gain to determine the nominal full scale input span to the converter. For example, if the PGA gain is set for a gain of 8, then the input span to the instrumentation amplifier will be 2.5 volts (VREF+ - VREF-) divided by 8 X 25, or 2.5/(200) = 12.5 mV nominal in unipolar mode, or ± 12.5 mV nominal in bipolar mode. The specified calibration range is ± 20 % of nominal, therefore the device can be gain calibrated to handle a full scale input from a low of 10 mV (20% below 12.5 mV) or to a high of 15 mV (20% greater than the 12.5 mV nominal). To modify the input span, the user can either change the PGA gain setting or modify the resistor divider ratio on the bridge sense voltage which determines the VREF input voltage.

What happens if the full scale span is greater or less than the nominal full scale span by more than ± 20 %?

The calibration range of the gain register spans from 2^{-23} to 2.0 in decimal, and the converter can calibrate with inputs as great as ± 50% of the nominal value, but missing codes can occur in the output transfer function if the calibration range is extended. The intent of the ± 20 % calibration range specification is to insure proper code computation with no missing codes in the output transfer function, and that the analog signal does not saturate any portion of the signal path inside the device (see later discussion on the block diagram model of the converter).

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The resistor values shown in the data sheet for the excitation divider are too low in value and may cause gain error due to excessive loading of the excitation signal when used with remote transducers. How large can these resistors be?

The original data sheet showed the VREF divider resistors as 750 and 500 ohms. The current data sheet indicates these as 7500 and 5000 ohms if the associated filter capacitor is reduced to 470 pF. The AIN and VREF inputs to the converter are both switched-capacitor inputs. The RC-time constant associated with the inputs on the VREF+ and VREF- pins, and on the AIN+ and AIN- pins, should be such that the capacitor sampler settles to full accuracy in a sampling period. Figure 1 illustrates a simplified model of each of the pins for VREF+, VREF-, AIN+ and AIN-. The input has a dynamic current requirement based upon charging a sampling capacitor. The input current is a function of the sampling capacitor, the sampling clock, and the offset of the buffer. The offset of the buffer will not exceed 25 mV over the -55 to +125°C temperature range. Using this model, one can determine the value of the dynamic current and the effective input resistance. The model can be also be used to compute the errors contributed by external source impedances.

For example, the input current required by the AIN+ pin should be about 52nA plus leakage current when the converter is operated with XIN = 4.096MHz.

$$i_n = V_{os} f c_s = (25mV)(4.096MHz)(0.5pF) = 52nA$$

The application note *Switched-Capacitor A/D Converter Input Structures* explains the input current effects of the sampled capacitor circuit.

Can you provide an example of how the sense lines from a transducer can be buffered to reduce the loading effect of the reference divider resistors?

The sense lines from the bridge can be buffered as shown in figure 2 or figure 3. The drift in the amplifier offset is referenced to the VREF voltage, not to the input span of the converter and therefore will have a negligible effect on gain accuracy.

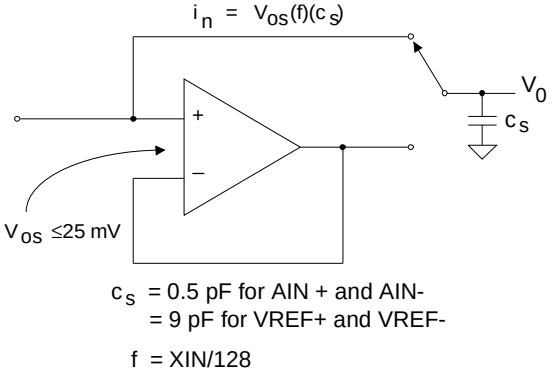

Figure 1. Simplified Model for AIN and VREF Inputs.

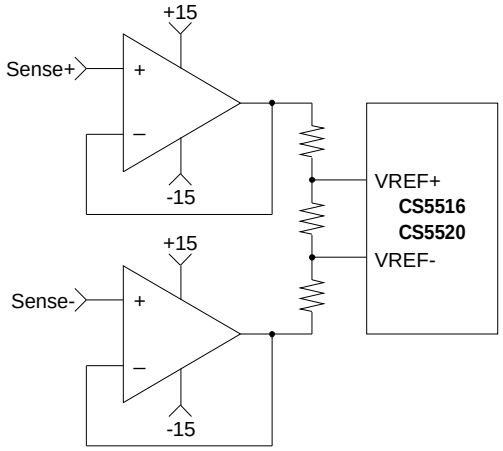

Figure 2. Using Op Amps to Buffer Sense Lines.

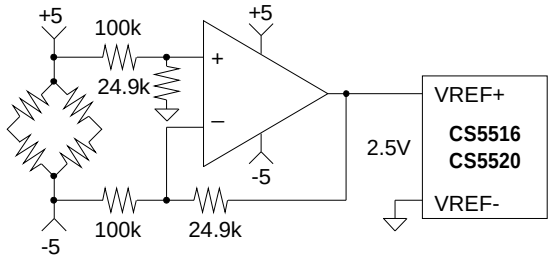

Figure 3. Single Op Amp Used to Buffer Sense Lines.

Explain the operating limitations of the CS5516/CS5520. For example, what happens if the bridge is excited with a single +5 volts rather than ± 5 volts?

Figure 4 illustrates the block diagram of the converter with some notes stating signal limitations at the various stages inside the converter. The instrumentation amplifier inside the CS5516/CS5520 has a differential gain of 25 (the amplifier is shown with a single-ended output in the figure; it actually has a differential output) and a common mode gain of 1. The easiest way to explain its signal limitations is to state that the output of the X25 instrumentation amplifier cannot exceed ± 3.75 volts; the maximum differential input signal must be less than 300 mV - | V_{cm}/12.5| where V_{cm} is the common mode voltage of the input signal. If the bridge is excited with only +5 volts (no -5V) then the common mode input to the instrumentation amplifier is +2.5 volts. So the maximum differential input signal is 300 mV - |2.5/12.5| = 100 mV. The common mode gain of one yields a common mode signal out of the X25 amplifier of 2.5 volts; the differential gain of 25 yields a differential signal out of the X25 amplifier of 2.5 volts differential, that is ± 1.25 volts. The 2.5 volts common mode plus the 1.25 volts differential together are at the limit of +3.75 volts.

The output of the gain block also has a saturation limitation of ± 3.75 volts, but the PGA does not amplify the common mode signal. The differential signal portion of the output of the X25 amplifier is ± 1.25 volts. Since the output of the PGA is limited to ± 3.75 volts maximum, gains of 1 or 2 can be used (if a gain of 2 is used, the gain calibration word will be outside the recommended range). Gains of 4 or 8 cannot be used, for in this example these would exceed the signal range limitation of the gain block output.

The actual input to the modulator is restricted to 5 volts total, that is ± 2.5 volts differential. Again the gain block, the DAC, and the modulator are all shown as single-ended, whereas they are actually fully-differential. The DAC must be used to trim any offset in the signal ensure that the span into the modulator does not exceed the ± 2.5 volts differential span. The DAC can trim up to ± 200 % of the maximum differential signal input into the X25 amplifier.

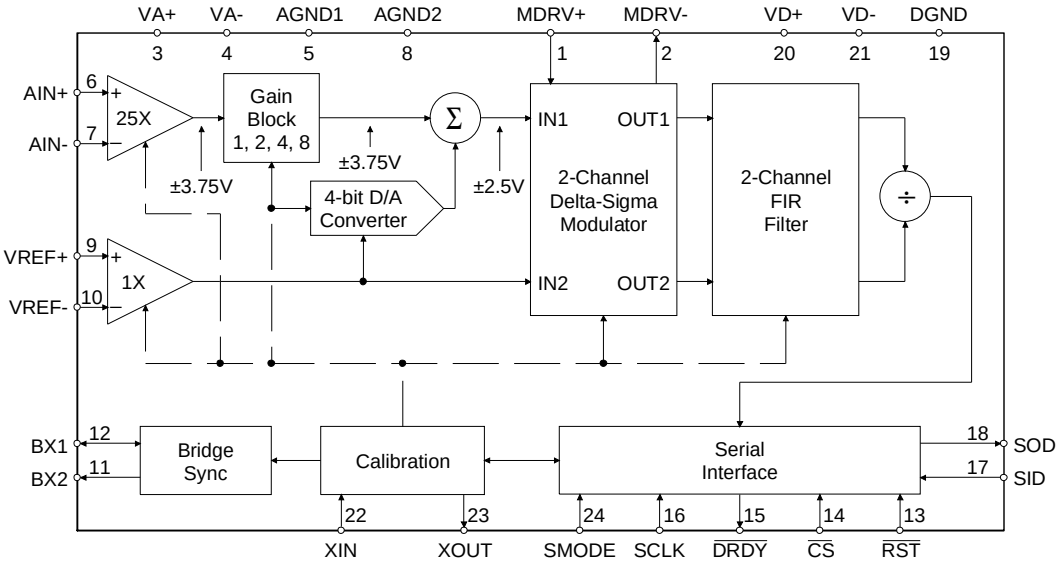

Figure 4. A/D Block Diagram Indicating Signal Path Limitations.

How does the XIN clock frequency affect the filter bandwidth?

The CS5516/CS5520 can be operated with any crystal between 1.0 MHz and 5.0 MHz with corresponding changes in the digital filter. The digital filter inside the converter is optimized to provide a very deep attenuation notch (-140 dB) at 50 Hz when using a 4.096 MHz crystal or a very deep filter notch at 60 Hz when operated from a 4.9152 MHz crystal. The device can be operated at other frequencies and still attain very good rejection (90 dB) attenuation at both 50 and 60 Hz. Figure 5 illustrates the magnitude plot of the digital filter. Note that the entire filter transfer function scales with a change in clock frequency. At frequencies above the first notch frequency, the out-of-band attenuation will be at least 90 dB for frequencies above the filter cut-off but below the modulator sampling frequency (XIN/256).

What is recommended if I need narrower bandwidth than provided by the on-chip digital filter?

The CS5516/CS5520 were designed to give high update rate (50 Hz with XIN = 4.096 MHz) with a 25 Hz usable bandwidth. The filter is designed to settle in less than six output words when the input changes in a transient manner. It is desirable in many weighing applications that the circuit have very low bandwidth (typically 1 to 4 Hz) to eliminate scale resonances and vibration. To accomplish this type of bandwidth with the CS5516/CS5520, the user should average several output words. Averaging 10 output words (XIN = 4.096 MHz) will result in a -3 dB filter bandwidth of about 2.5 Hz. This filtering was not included on the chip because many weigh scale designers prefer to design their own "adaptive" filter which can settle fast when the input signal changes in a transient manner, but implement more attenuation as the signal begins

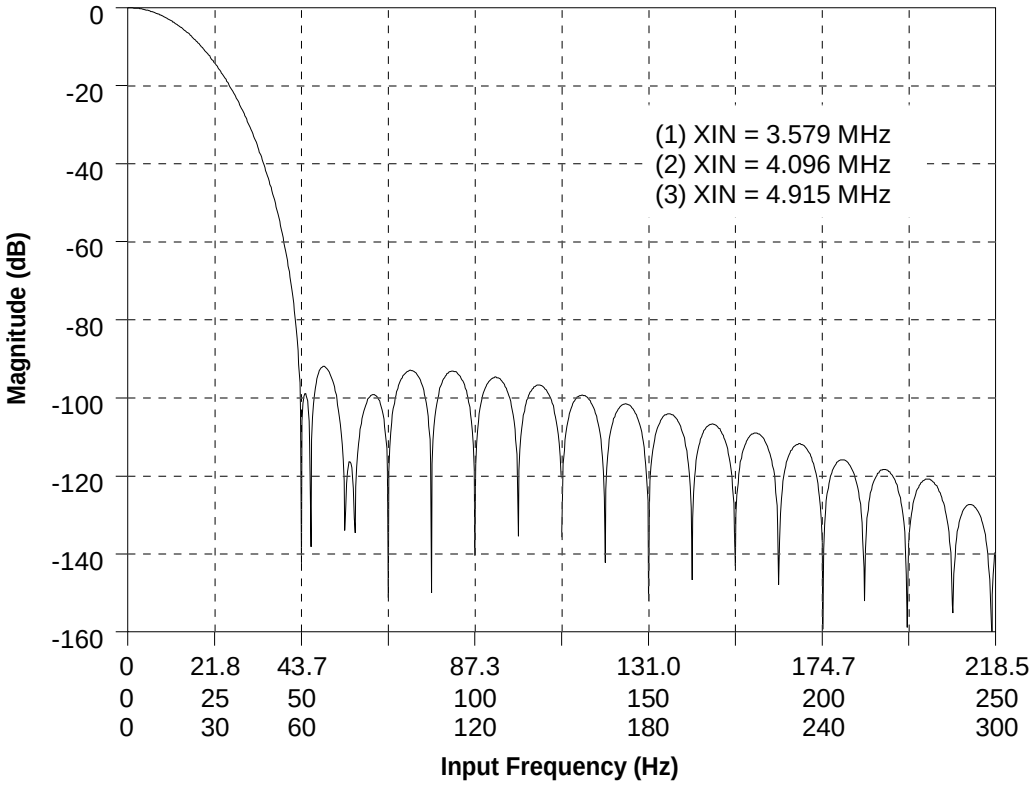

Figure 5. Filter Response at Various XIN Frequencies.

to settle. To accomplish this, use the 50 Hz update directly when the data suggest that the input signal is changing at a rapid rate (weight has just been placed on the scale). Then switch to averaging once the signal has settled to within a specified error band; typically some band slightly greater than the peak-to-peak noise of the signal. The exact requirements of the adaptive filter function will be dictated by the application; particularly the mechanical response of the weighing system.

The CDB5516 and CDB5520 evaluation boards include software which allows the user to read and write all registers in the converters, collect conversion data, perform averaging, save data to a file, and compute the standard deviation (one standard deviation is equivalent to the rms noise for gaussian type noise). The evaluation board may be of assistance in evaluating the amount of averaging to perform in your circuit.

Should I use a series or parallel type crystal?

Either crystal will work. Series or parallel designates the electrical configuration in which the crystal was calibrated. The CS5516/CS5520 converter uses a parallel configuration (Pierce oscillator). If a series crystal is used, it will oscillate reliably but its frequency will be slightly different than that of a parallel cut crystal (typically within 0.03% of the same frequency).

The converter seems to lock up or not respond to calibration instructions. Any suggestions?

When the device or the serial port is reset, the port is waiting for a command. Inside the port, there is a pointer register which counts SCLKs to keep track of whether the information being moved through the port is to be interpreted as a command or as calibration register data. After the converter is reset, the pointer will count the first 8 SCLKs and accept the data bits associated with these as a command. The pointer then counts the next 24 SCLKs and interprets the data bits associated with these as register data. The SCLKs must start low, transition high, and then return low to be counted properly. Problems can arise if the $\overline{CS}$ is released (returned high) before the falling edge of the last SCLK. The pointer will get confused and begin recognizing the bits of the commands words as data bits or vice versa. So watch your SCLKs.

When the CS5516/CS5520 is interfaced to a microcontroller, it is sometimes difficult to discern whether the converter is actually receiving commands. A simple way to assess whether the interface is working properly, is to reset the converter and then to transmit one 88(H) command (read conversion data) to the serial port. Do not attempt to read the data output, instead, use your oscilloscope to see if $\overline{DRDY}$ (pin 15) starts toggling. $\overline{DRDY}$ should start toggling if the interface is working properly.

When the converter is put in the read conversion data mode, it will output a conversion data word to its serial port register every 81,920 XIN clock cycles. Therefore, 81,920 XIN clock cycles elapse between $\overline{DRDY}$ falling, but the user must read the conversion data within 51,000 XIN clock cycles after $\overline{DRDY}$ falls. After the 51,000 XIN period, the converter is using its internal bus to perform calculations and to move data between registers. If a read is attempted during this time, the internal data bus can experience contention, which can cause the bus to lock up.

When reading the conversion data I get all zeroes no matter what the analog signal is. Please explain why.

Check your voltage reference between pins 9 and 10 (VREF+ and VREF-). If this voltage is zero, the converter will compute all zeros for the output conversion data. Remember an A/D converter computes a digital word which

represents the ratio of the input signal to the voltage reference. If the voltage reference is zero the output will be zero.

The conversion data out of the converter changes as the input signal changes, but is never correct. Any suggestions?

When the converter is configured for external bridge excitation, the BX1 input pin determines the phase of the internal detection circuitry for the AIN and the VREF input signals. For external dc excitation, the BX1 pin should be pulled up to +5 volts through a 10 k resistor to insure the proper phase of the input signals.

If ac excitation is used, be certain that the phase of the signals into the VREF and AIN pins is in phase with the BX2 signal. If either of the signals is not in phase with the BX2 signal the converter will not compute correct conversion data.

Is calibration required to use the converter? Must non-ratiometric calibration be performed?

When the CS5516/CS5520 is reset, the registers are set to known values. If the signal to be measured by the converter is within the nominal range, the converter can perform conversions without the need for calibrations. Some users apply their own calibration scheme using software and registers in their microcontroller.

After being reset, the CS5516/CS5520 will convert on the signal being measured. The only limitation of not using the converter's calibration functions is that the errors in the system remain present. This may be acceptable if the errors are insignificant to the measurement or if the errors are removed by some other means, such as software in the user microcontroller.

The CS5516/CS5520 offers a complete set of calibration features; non-ratiometric offset calibration, ratiometric offset calibration, and gain calibration. The converter can perform conversion without any calibration being performed. Just because the calibration feature is available does not mean the feature must be used. The user's application should dictate if calibration should be used to remove specific errors. It may be quite acceptable in a given application to not use the non-ratiometric calibration features of the converter. The user can evaluate the magnitude of the error source and its effects on the resulting conversion data by either analysis or by empirical investigation. The application note *Overcoming Errors in Bridge Measurement* discusses the various error sources and their contribution to the final error in the output data. Often the user can use the CDB5520 evaluation board to investigate these errors. The CDB5520 comes with PC-compatible software which allows the user to perform calibrations and read all of the registers in the converter. Once the calibrations are performed, the magnitudes of the numbers in the registers indicate an estimate of the magnitudes of the errors which have been calibrated.

How often do I need to recalibrate?

To answer this question one must ask: 1) What accuracy is required from the A/D converter? 2) What effects will temperature changes have upon the entire circuit, including components outside the A/D? Once power is applied to the converter, it will take about a minute for the chip to reach thermal equilibrium. It is best if calibration is performed after the chip has reached this stable operating temperature.

A higher accuracy measurement requirement will generally require calibration to occur more often, because, after the initial calibration has been performed, the converter is subject to some drift if the operating temperature changes. Typical offset drift (± 0.005 μV/°C) and gain drift (1 ppm/°C) are given in the data sheet tables. The

observed drift in the application circuit may be considerably greater due to parasitic thermocouple effects and gain drift caused by the limited tempco tracking of the VREF divider resistors. Once an estimate of drift is determined for the entire application circuit (drift will usually be dominated by error sources external to the converter), one can assess how this will affect measurement accuracy as temperature changes. Once the amount of drift is known, it can be determined if a new calibration is required. Using AC-excitation removes the effects of parasitic thermocouples and offset drifts and therefore will require less recalibration as the operating temperature changes.

The CS5516/CS5520 has been subjected to 1000 hour burn-in at 125°C to investigate the effects of aging. The converter was tested with a full scale signal using AC excitation mode with maximum PGA gain and maximum DAC offset. The devices showed drift over the test period of about 10 ppm, but it was inconclusive how much of the drift was attributable to the converter. The laboratory measurement equipment has limited stability over the 1000 hours also (6 1/2 digit voltmeters are only guaranteed to 10-20 ppm drift over a 90 day period at room temperature).

Explain the difference between non-ratiometric and ratiometric.

Load cells are ratiometric devices, meaning that their output signal is proportional to their excitation voltage. For example, if the excitation voltage increases by three per cent, then the output signal from the load cell will also increase by three per cent. A ratiometric offset is an offset, such as the offset of the load cell, which changes proportionally to the load cell excitation voltage. A non-ratiometric offset is one which does not change proportionally with changes in the load cell excitation voltage. The offset of an operational amplifier which amplifies the bridge signal is non-ratiometric; if the bridge excitation changes, the offset does not change in proportion to it. Non-ratiometric offsets become an issue if the magnitude of the bridge excitation voltage changes due to drift.

What do the numbers in the calibration registers actually mean?

There are two non-ratiometric offset calibration registers, one for the AIN input and one for the VREF input; one 4-bit offset trim DAC; one ratiometric offset calibration register for the AIN input; and one gain calibration register. When the calibrations are performed, they should be performed in the following sequence: The non-ratiometric offsets should be calibrated first (if you choose to calibrate them); then the ratiometric offset; followed by gain calibration.

When the non-ratiometric offsets are calibrated, an LSB in the 24-bit digital calibration words represents 2^{-23} proportion of an internally-scaled MDRV (Modulator Differential Reference Voltage). At the MDRV+ and MDRV- pins, the MDRV has a nominal value of 3.75 volts. This voltage is internally scaled to a nominal 2.5 volts for use with the non-ratiometric calibration. The 24-bit calibration word is stored in 2's complement form with one count equal to approximately 300 nV at the input of the internal A/D converter. For the AIN channel this will be scaled down by the gain of the instrumentation amplifier (X25) and the PGA gain. For a PGA gain = 1, one count will represent about 12 nV. Non-ratiometric offset to be calibrated by the VREF channel cannot exceed approximately ± 2.5 volts. Non-ratiometric offset to be calibrated by the AIN channel cannot exceed approximately ± 2.5 volts divided by the channel gain. With a PGA gain = 1, the maximum non-ratiometric offset which can be calibrated on the AIN channel cannot exceed approximately ± 100 mV.

When the ratiometric offset is calibrated, the 4-bit DAC coarsely trims offset from the analog

signal. The remaining ratiometric offset in the AIN channel is trimmed after the signal is converted using the digital word from the ratiometric offset register. The DAC allows the user to add or subtract offset up to 200 per cent of the nominal input signal. The AIN ratiometric offset register can be used to add or subtract offset equal to the nominal full scale input signal into the X25 amplifier. An LSB in the ratiometric offset register represents 2^{-23} proportion of the voltage input across the VREF+ and VREF- pins at the internal input to the AIN channel A/D converter. This will be scaled down by the AIN channel gain when calculated relative to the instrumentation amplifier input. For example, with a VREF = 2.5 V, and a PGA gain = 1, one count of the ratiometric offset register would represent about 12 nV at the instrumentation amplifier input. The proportion remains ratiometric even if the VREF voltage should change. The 24-bit register content is stored in 2's complement form.

All calibration registers can be read or written by the user. This allows the contents of the calibration registers to be read and stored in EEprom; or to be modified by the user. This is useful in the case of the ratiometric offset register as it allows the user to add or subtract small offsets from the transfer function after the calibration has been performed. This allows the user to shift the transfer function to allow for load cell creep or load cell zero shifting "below zero" when the converter is measuring in unipolar mode. It also allows the gain register to be modified as will be discussed in the next question.

The gain calibration is performed last. The contents of the gain register spans from 2^{-23} to 2. After gain calibration has been performed, the numeric value in the gain register should not exceed the range of 0.8 to 1.2 (decimal)[666666H to 999999H]. The gain calibration range is ± 20 % of the nominal value of 1.0. The nominal value of 1.0 is for an input span dictated by the VREF voltage, the PGA gain and the X25 instrumentation gain (see the previous discussion on setting the input span to the converter). The converter may operate, subject to internal amplifier saturation (discussed later) with gain slope factors from 0.5 to 2.0 (decimal) but when the slope exceeds 1.2 the converter output code computation may lack adequate resolution, giving results which may include missing codes.

How can the gain be calibrated if a full scale signal is not available?

Some scale manufacturers desire to calibrate gain using some weight other than full scale. For example, a truck scale may have a capacity of 100,000 lbs (45,400 Kg.). Who wants to carry around that much weight to calibrate the scale? Calibrating the scale with 10 per cent of full scale capacity isn't a simple task.

The CS5516 or CS5520 can be gain calibrated with some input signal other than full scale. Assume one wants to calibrate using an input which is 10 per cent of full scale capacity. The normal gain calibration procedure cannot be used. Instead, the user can increment or decrement the gain register until the converter arrives at the correct value, or the correction factor can be calculated. For example, when the converter is reset, the gain calibration word is 1.0. If a weight representing ten per cent of full scale reads three per cent less than it should, the value in the gain register can be scaled up by three per cent. Gain accuracy can be improved if output words are averaged while using this technique.

Caution is advised in using a calibration weight less than full scale. If the transfer function of the the load cell happens to have a major nonlinearity at the point at which calibration is being performed, this will cause the rest of the transfer function to be incorrect. Be certain you

understand the particular linearity characteristics of the load cell you are using.

The calibration word is not exactly the same each time I calibrate with the same input conditions. Why is this?

The calibration word is calculated using output words from the converter which include the thermal noise. Therefore the resulting calibration words can be affected by this peak-to-peak noise. This can be overcome by calibrating several times in succession using the same input conditions and averaging the results with an external microcontroller. The averaged answer is then written back into the calibration register. The calibration word will typically have the same magnitude of peak-to-peak noise that is seen in the output conversion data. By investigating the magnitude of this noise, one can determine how many calibration words to be averaged. Remember that Gaussian noise is reduced by the $\sqrt{N}$ when N samples are averaged.

Is a different calibration required for each PGA gain setting?

The PGA gain steps will have some tracking error, typically 1 per cent or so. The PGA actually uses different capacitor values to set the PGA gain. These capacitors have a ratio error due to processing which determines the gain error of the PGA gain steps. Calibrations of non-ratiometric offset for AIN, ratiometric offset, and gain should be performed with the PGA gain (1, 2, 4, or 8) set to the range which is going to be used in the application. If the PGA is going to be changed during measurements, calibration words should be performed and saved in EEprom for each PGA gain setting.

Therefore, to achieve good gain tracking when the PGA gain is changed, a gain calibration should be performed with each PGA gain selection. The following calibration method is preferred by some designers as it requires only one user adjustment for the input signal. Assume the converter is being gain calibrated with a 2.5 volt VREF. With the PGA gain set to 8, the full-scale input would be 12.5 mV. Input the signal intended for full scale (12.5 mV ± 20%) and calibrate the gain with the PGA set to 8. Save the gain calibration word. Then without changing the input signal, change the PGA gain to 4. Ideally the converter should output a half scale code. The actual output code may be lower or higher. Increment or decrement the gain register until the resulting conversion code is half scale. Calculate the offset required to modify the gain register when changing the PGA from a gain of 8 to a gain of 4. Save this offset word and use it to modify to gain register when PGA gain is changed from 8 to 4. Next, reload the gain register with the calibration word determined with the PGA gain of 8 and change the PGA gain to 2. The converter should output a code of one quarter of full scale. Increment or decrement the gain register to yield the correct output code. Calculate the offset required to modify the gain register when the PGA is switched from 8 to 2. Save this offset for future use. Reload the gain register with the gain word for a PGA gain of 8 and change the PGA gain to 1. This time the output code should be one eighth of full scale. Modify the gain register and save the offset as done in the previous calibration steps. While this example calls for saving the register offsets, one can choose to save the gain words themselves. This will depend upon the algorithm you choose to use in your microcontroller. The advantage of this calibration method is that it removes the error associated with the user adjusting the input signal to a new value. The method can be very accurate if some averaging of the output conversion words is performed during the calibration sequence as this removes uncertainty due to the thermal noise in the system.

Why is ac excitation better than dc excitation?

The CS5516/CS5520 converters are designed for bridge transducer signals. Bridge transducers output low level signals which can be adversely affected by amplifier offsets, amplifier bias current effects, noise (both thermal and 1/f), and parasitic thermocouples. Parasitic thermocouples exist in normal circuit wiring. Junctions such as tin-lead solder and copper PC board trace can introduce thermocouple effects of 3-4 μV/°C if thermal gradients exist across the circuit. In a dc-excited bridge circuit, there is no way to discern between the actual low level signal being generated by the bridge and the error signals introduced by amplifier offsets, amplifier bias current effects, 1/f noise, and parasitic thermocouples unless some method is used to separate the actual signal from these error sources. One method of separating the signal from the error sources is to use an ac-excited bridge system.

When the CS5516/CS5520 are configured for ac-excited bridge measurement, the converter measures the signal which is of the same phase and frequency as the excitation frequency. The CS5516/CS5520 converter actually use a polarity-switched square wave whose frequency is normally a sub-multiple of the XIN clock frequency to the converter.

Figure 6 illustrates the benefits of ac excitation versus dc excitation. In one of the plots in Figure 6, the CS5520 converter was configured to measure a bipolar signal with an input span of ± 12.5 mV with dc excitation. Conversions were performed with a zero input signal from the bridge and data was collected for a one hour time interval. One LSB (least significant bit) of the CS5520 was equivalent to about 25 nanovolts. The data collected indicates that over the one hour period the average value of the data drifted as much as 1.3 microvolt, or about 50 counts. The CDB5520 evaluation board was used for collecting the data and the drift was attributed to parasitic thermocouples in the components or the wiring of the board. The board was used in open air and the data illustrates the effects of thermal gradients introduced by the cycling of the air conditioner system. The second plot in Figure 6 illustrates the stability of the conversion system when the converter is set up for the same operating

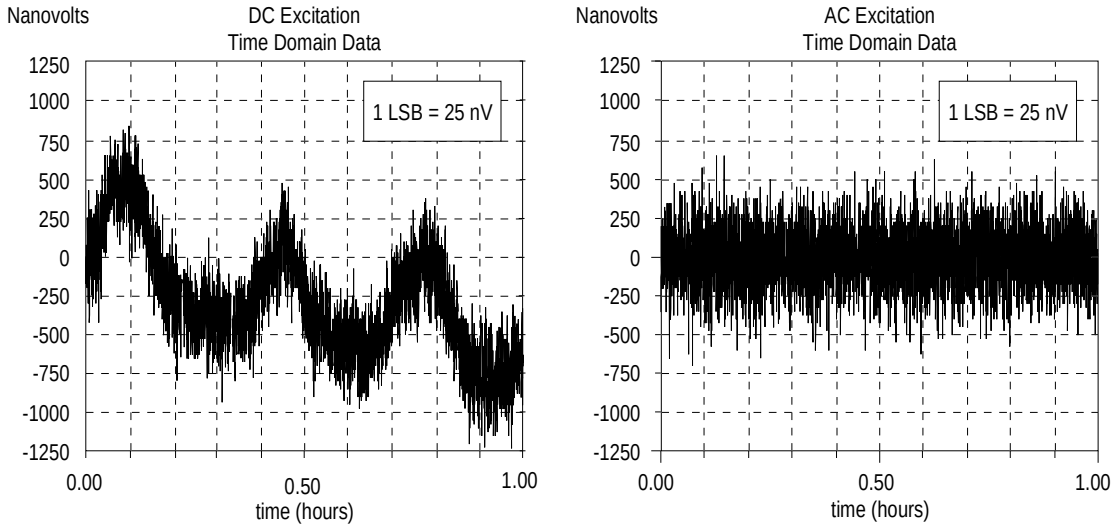

Figure 6. Stability Over One Hour using DC and AC Excitation.

conditions, but with ac bridge excitation. The plot illustrates the normal thermal noise of the circuit but the average value remains stable over time.

Are there disadvantages to ac-excitation?

The ac-excited bridge circuit must include some type of driver circuitry which can add some additional cost (The combination of a transistor and the MIC4428 is below $3.00 at 100 piece quantities (1994)). Another disadvantage is that service technicians must be educated about ac excitation; that troubleshooting with a dc meter isn't adequate; although the system can be configured for dc operation for basic troubleshooting tasks.

One must be cautious when using ac-excitation if the load cell uses a cable with a large capacitance. Since the converter uses a switched square wave to excite the bridge, the cable capacitance may adversely affect measurement accuracy if the square wave excitation signal does not settle adequately. The converter is designed to begin sampling the square wave signal at a time interval of 64 XIN clock cycles after the excitation signal changes polarity. The square wave should have settled to within ± 5% of its final value in the 64 XIN clock cycle period to ensure measurement accuracy. Note that this settling requirement must also be met by any filtering elements used in front of the converter on the AIN or the VREF signal inputs.

For very long cables, the CS5516/CS5520 can be configured for a switched bridge measurement configuration by setting the converter for dc excitation mode to measure bipolar signals and having the external microcontroller control the bridge polarity. When the polarity of the bridge excitation is changed, the external microcontroller then waits for at least six output words (the CS5516/CS5520 can take up to six filter cycles to settle whenever the input signal changes in a transient manner) from the converter before taking a final reading. By averaging a reading for one polarity of excitation with a reading with the opposite polarity of bridge excitation, the errors due to parasitic thermocouples can be averaged out. If this configuration is used, the normal calibration sequence for offset and gain would have to be modified. An algorithm to calibrate the offset and gain registers could be developed by the user.

BX1 and BX2 outputs are used for ac excitation. What logic level is output from these pins if the ac excitation is stopped? What are the logic outputs of BX1 and BX2 if the converter is put to sleep?

Internal excitation with the F1-F0 bits of the configuration register equal 0 sets BX2 = +5V, BX1 = 0V. If external excitation is used, BX1 will always control the BX2 output. In sleep BX1 = +5V and BX2 = 0V.

Explain the noise performance of the CS5516/CS5520.

The data sheet gives a typical noise specification for the CS5516/CS5520 at each gain when operating in bipolar mode with a VREF voltage of 2.5 volts. When operating in this mode one LSB of the converter is equal to (2 X 2.5)/(Gain X 2^{20}). For example, with a gain of 200 (8 X25) the noise specification is 150 nV rms. With a gain of 200, one LSB in the CS5520 converter (bipolar mode) is equivalent to about 23.8 nV, so the rms noise would be equivalent to 150 nV/23.8 nV or 6.3 counts. A rule of thumb says that peak-to-peak noise is 6 to 6.6 times greater than rms, so the peak-to-peak noise would be about 38 to 41 counts when operating in this mode. This calculation can be verified by capturing 1000 (the statistical uncertainty is reduced if a large number of samples are collected) conversion words into a file and computing the standard deviation of the data.

One standard deviation is equivalent to the rms noise if the data follows a Normal or Gaussian distribution. It is useful to plot a histogram of the data to verify that it has a Gaussian characteristic. The noise in the converter itself is Gaussian so the user can average output words to reduce the effects of noise. Averaging N samples reduces the noise in the averaged output words by the $\sqrt{N}$.

The CDB5516 and CDB5520 evaluation boards include software which allows the user to read and write all registers in the converters, collect conversion data, perform averaging, save data to a file, and compute the standard deviation of a group of output conversion words. The evaluation board and its software may be able to assist in evaluating the noise of the converter in your system.

My application circuit appears to have an excessive amount of noise. How do I determine the cause?

If the results from your circuit exceed the expected value (usually a computed estimate for the circuit based on sound engineering analysis), some steps can be taken to help determine the source of the excess noise. The first step is to remove the load cell from the circuit and ground the input signal leads as shown in figure 7. With the input grounded, collect at least 1000 samples (to remove statistical uncertainty) and perform a histogram analysis on the data. Figure 8 illustrates an example of a noise histogram which has been performed on data using Quattro which shows the "shape" of the data (Gaussian). Calculate the standard deviation of the data (one standard deviation is equivalent to the rms noise for gaussian type noise). The load cell has been disconnected so that the noise performance of the digitizer can be assessed by itself. If the converter is "quiet" with the input grounded, it suggest that noise is getting onto the cable or that the load cell is possibly sensitive to vibration. If the noise is still too high, try grounding the AIN+ and AIN- pins of the converter right at the converter itself and perform the test again. The input components to the converter may be picking up high frequency radiated noise from some digital circuitry on the board.

If the noise histogram plot does not appear to be Gaussian, suspect radiated interference from digital circuitry or from a dc-dc converter.

When testing for noise, be sure to ground the input signal leads to the signal ground; do NOT use a load cell simulator. See the next item.

Is a load cell simulator a good test tool for evaluating the CS5516 and CS5520?

It is helpful to know what limitations can exist if you are using a load cell simulator in place of an actual load cell. If you are trying to use the CS5520 to digitize a 10 to 20 mV signal to 20 bits, the output codes can drift around due to what is apparently 1/f noise in the simulator. A way to test this is to use two 348 ohm 1% metal film resistors tied from the AIN+ and AIN- inputs of the CS5520 to the signal ground. Examine to see if the drift remains when the simulator is disconnected and the signal source is signal ground.

A second problem which can be encountered when using a load cell simulator is that some simulators will not work well with AC excitation. It seems that the switch contacts in some simulators are made of materials which rectify the signal and therefore cause errors in the bridge output signal. Use a totally resistive bridge with no switches if you encounter this type of problem.

What benefit does an evaluation board offer?

The CDB5516 and CDB5520 evaluation boards save time and money over prototyping. The

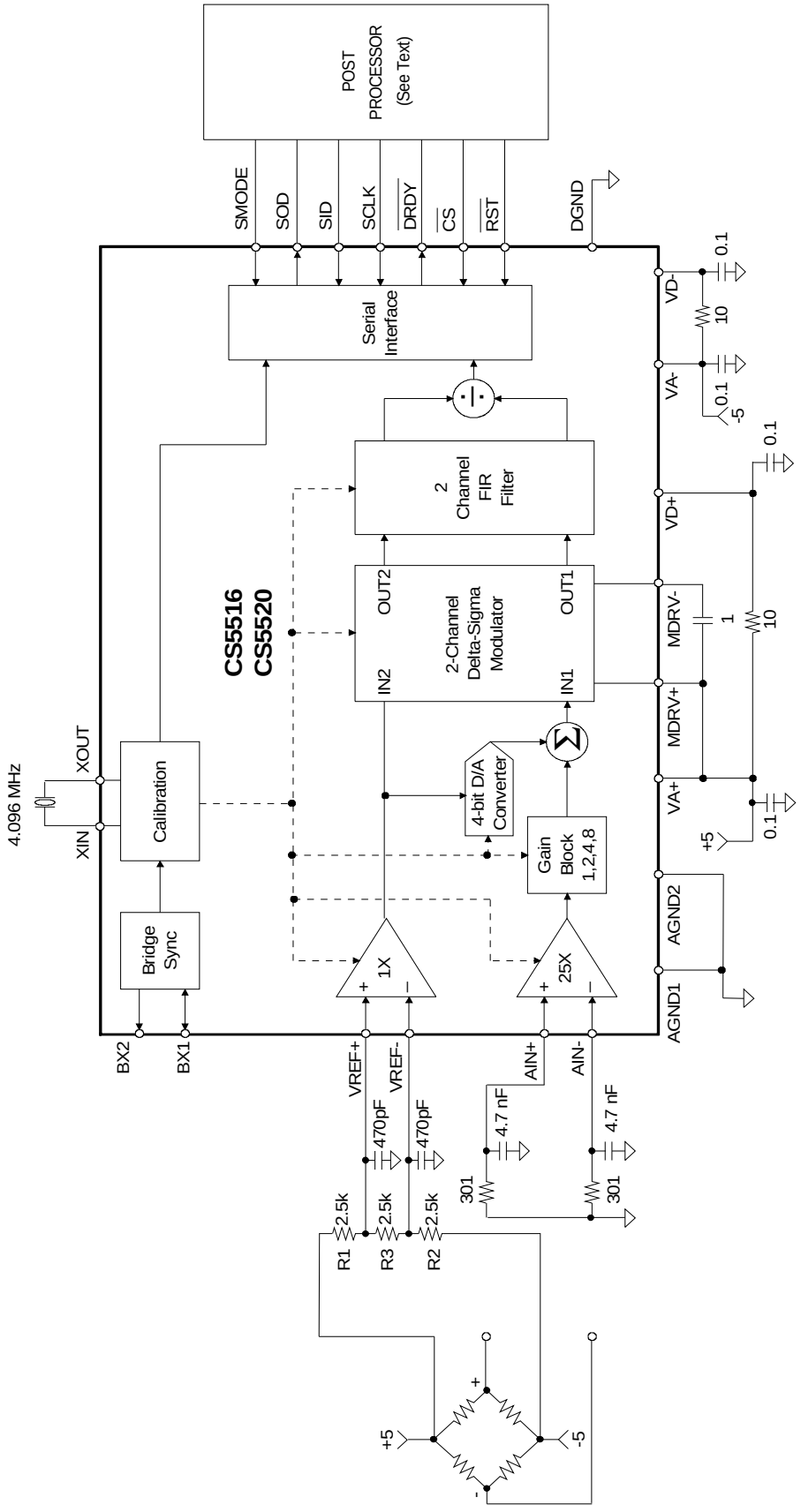

Figure 7. Ground Input Leads for Troubleshooting Noise.

preassembled and tested boards come with a serial cable to connect to a PC-compatible computer and include software which allows the user to manipulate the registers inside the CS5516 or CS5520. Calibrations can be performed and conversion data can be collected. The evaluation boards support dc or ac excitation of a bridge transducer (not supplied) which is connected to a terminal block on the circuit board.

The CDB5520 includes a CS5520; the CDB5516 includes a CS5516. Other than the converter which is socketed on the board, the evaluation boards are identical. Therefore, the board can be used to evaluate either converter chip. The software includes a menu selection for the type of converter (CS5516 or CS5520) to be tested.

The data sheet states that the converter uses about 3 mA of current. Mine draws about 30 mA. Any explanation for this?

Check your BX1 pin. One of the schematics in the first data sheet had this pin tied to +5 volts directly. It must be pulled up through a resistor as the BX1 pin has a low logic output when the converter first gets reset. If the circuit is configured for external dc excitation mode, cut the trace and use internal dc excitation; or pull up the pin with a resistor pull-up.

The MIC4428 and MIC4425 devices are used in applications with the CS5516/CS5520. What is the address of the company that makes these devices?

Micrel, Inc., 1849 Fortune Drive, San Jose, CA, 95131. (408) 944-0800, FAX (408) 944-0970.

Pin-for-pin replacements are available from Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA, 94086, phone: (408) 737-7600; and from Calogic Corporation, 237 Whitney Place, Fremont, CA 94539, phone: (510) 656-2900.

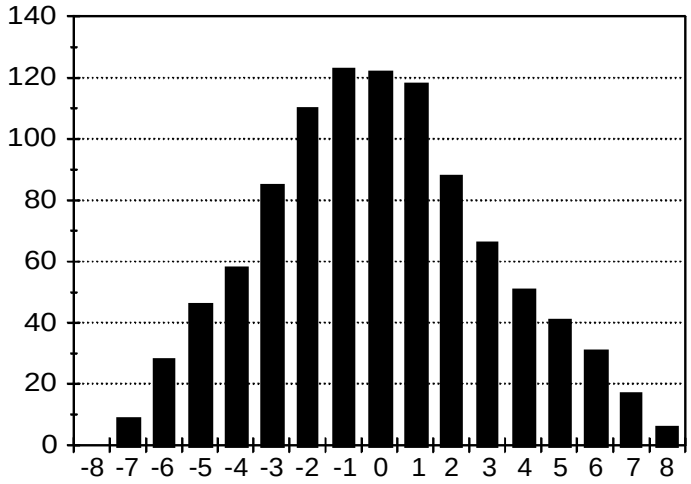

Figure 8. Example Noise Histogram for CS5520 Output Codecs VREF = 2.5V, PGA = 4, Bipolar mode.

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