AN30210A

Power supply control IC for a digital still camera

■ Overview

The AN30210A is a low voltage operative IC which has 1-ch., 5 V output sharing self-biasing voltage and PWM DC-DC converter control outputs of 6-ch. It is configured with step-up 3 channels, step-up/down 1 channel, step-down 1 channel and 2 channels for transformer drive.

Since its minimum operating voltage is as low as 1.5 V, it can be operated by two dry batteries.

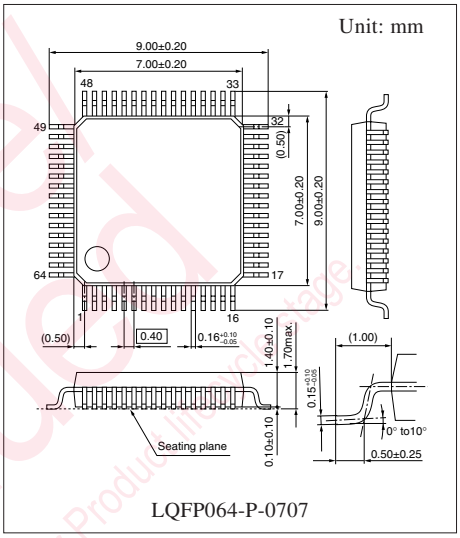
All channels operate synchronously and a synchronous rectification method is used for the low output voltage channel, thus achieving a high precision output voltage with $V_{REF} \pm 1\%$. It also is capable of driving directly the output power MOSFET of each channel.

■ Features

- Operating supply voltage range: 1.5 V to 7.2 V
- High precision reference voltage circuit built-in (±1%)
- All channels are synchronous operation in PWM control
- Synchronous rectification for the low output voltage channel (Synchronous rectification can be stopped by the external signal at the low load: STOP)
- ON/OFF (sequence control) pin attached for each and all channels. Soft-start pins for each channel (Simultaneous soft start is available with one external capacitor.)
- Timer latch circuit for short-circuit protection circuit (Selectable for each channel separately or all channels simultaneously)
- Control frequency reduction is available by an external signal at the low load.
- Maximum duty cycle 88% (Adjustment range of 0% to 100% with an external resistor)
- Low power dissipation and high speed operation thanks to 0.6 µm CMOS process

■ Applications

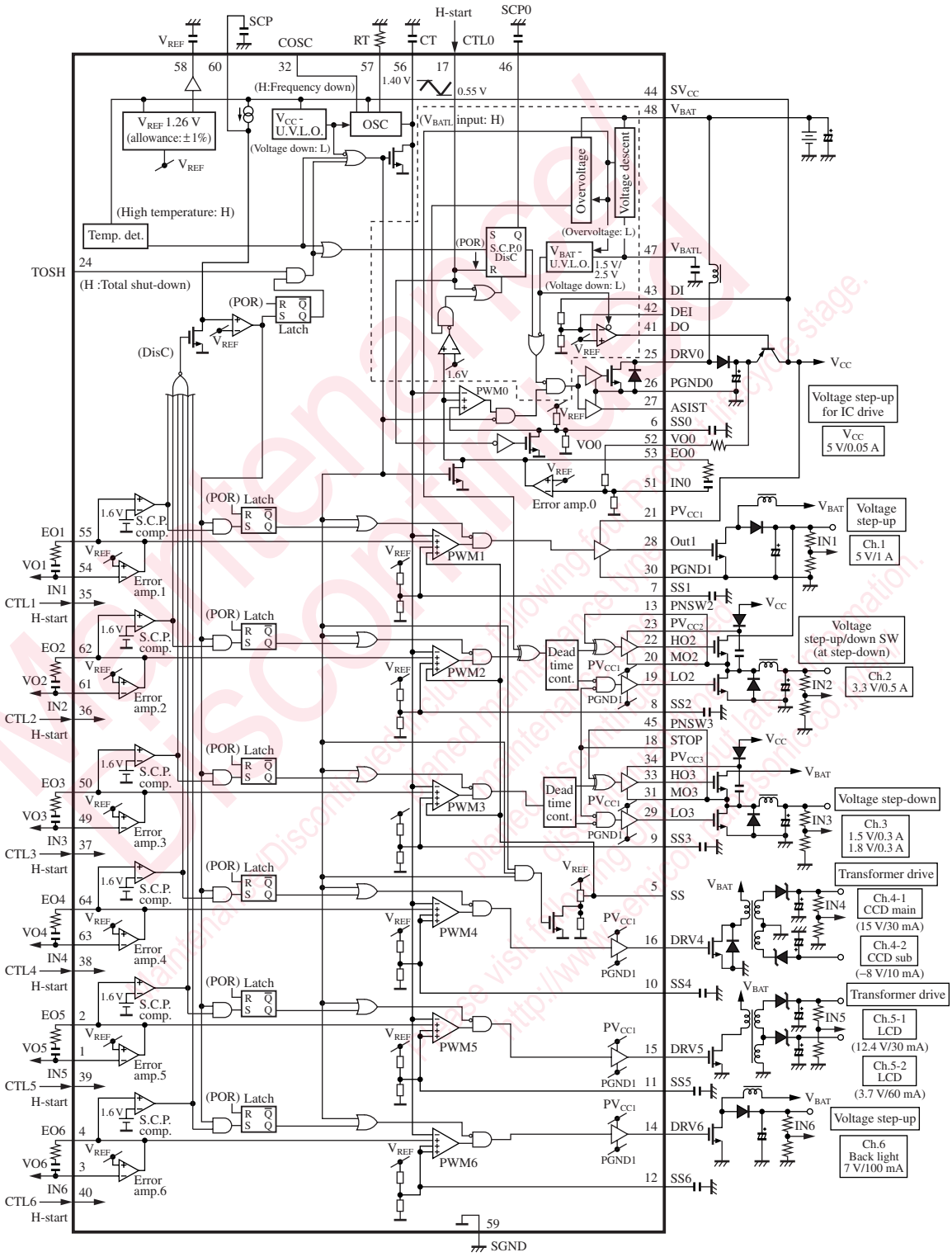
- Digital still cameras



LQFP064-P-0707

Note) The package of this product will be changed to lead-free type (LQFP064-P-0707B). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	IN5	Ch.5 error amplifier inverting input pin	33	HO3	Ch.3 high-side driver pin
2	EO5	Ch.5 error amplifier output pin	34	P_{VCC3}	Ch.3 US driver power supply pin
3	IN6	Ch.6 error amplifier inverting input pin	35	CTL1	Ch.1 on/off start-up input pin
4	EO6	Ch.6 error amplifier output pin	36	CTL2	Ch.2 on/off start-up input pin
5	SS	Ch.1 to ch.3 common soft-start setting pin	37	CTL3	Ch.3 on/off start-up input pin
			38	CTL4	Ch.4 on/off start-up input pin
6	SS0	Ch.0 soft-start setting pin	39	CTL5	Ch.5 on/off start-up input pin
7	SS1	Ch.1 soft-start setting pin	40	CTL6	Ch.6 on/off start-up input pin
8	SS2	Ch.2 soft-start setting pin	41	DO	Dropper error amplifier output pin
9	SS3	Ch.3 soft-start setting pin	42	DEI	Dropper error amplifier inverting input pin
10	SS4	Ch.4 soft-start setting pin	43	DI	Dropper output monitor pin
11	SS5	Ch.5 soft-start setting pin	44	SV_{CC}	Supply voltage application pin for signal block
12	SS6	Ch.6 soft-start setting pin			
13	PNSW2	Ch.2 high-side/P-ch., N-ch. switching pin	45	PNSW3	Ch.3 high-side/P-ch., N-ch. switching pin
14	DRV6	Ch.6 driver output pin	46	SCP0	Short-circuit protection time constant setup capacitance connection pin for ch.0
15	DRV5	Ch.5 driver output pin			
16	DRV4	Ch.4 driver output pin	47	V_{BATL}	Battery low-voltage application pin
17	CTL0	Ch.0 on/off start-up input pin	48	V_{BAT}	Battery voltage application pin
18	STOP	Synchronous rectification stop pin	49	IN3	Ch.3 error amplifier inverting input pin
19	LO2	Ch.2 low-side driver output pin	50	EO3	Ch.3 error amplifier output pin
20	MO2	Ch.2 middle-side output pin	51	IN0	Ch.0 error amplifier inverting input pin
21	PV_{CC1}	Ch.1, ch.2/L, ch.3/L, ch.4 to ch.6 driver power supply pin	52	VO0	Ch.0 output monitor pin
			53	EO0	Ch.0 error amplifier output pin
22	HO2	Ch.2 high-side driver output pin	54	IN1	Ch.1 error amplifier inverting input pin
23	PV_{CC2}	Ch.2 US driver power supply pin	55	EO1	Ch.1 error amplifier output pin
24	TOSH	Overcurrent individual/ total shutdown switching pin	56	CT	Oscillator frequency setup capacitor connection pin
25	DRV0	Ch.0 step-up output pin	57	RT	Oscillator frequency setup resistor connection pin
26	PGND0	Ch.0 step-up output GND			
27	ASIST	Assist transistor driver output pin	58	V_{REF}	Reference voltage output pin
28	Out1	Ch.1 driver output pin	59	SGND	Signal GND
29	LO3	Ch.3 low-side driver output pin	60	SCP	Short-circuit protection time constant setup capacitor connection pin for ch.1 to ch.6
30	PGND1	Ch.1, ch.2/L, ch.3/L, ch.4 to ch.6 driver GND			
			61	IN2	Ch.2 error amplifier inverting input pin
31	MO3	Ch.3 middle-side output pin	62	EO2	Ch.2 error amplifier output pin
32	COSC	Control frequency switching pin at low load	63	IN4	Ch.4 error amplifier inverting input pin
			64	EO4	Ch.4 error amplifier output pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	SV_{CC}	6.9	V
V_{BAT} / V_{BATL} voltage	V_{BAT} / V_{BATL}	7.5/6.0	V
Supply current	I_{CC}	—	mA
Power dissipation *2	P_D	QFS – 64	mW
Operating ambient temperature *1	T_{opr}	–20 to +85	°C
Storage temperature *1	T_{stg}	–55 to +125	°C
DRV0 allowable application voltage	V_{DRV0}	V_{BAT} + 0.1	V
Power V_{CC1} allowable application voltage	PV_{CC1}	SV_{CC} + 0.1	V
DRV0 allowable peak current *4	I_{DRV0P}	3.5	mA
Ch.2 high-side transistor switching input allowable application voltage *3	PNSW2	SV_{CC} + 0.1	V
Ch.3 high-side transistor switching input allowable application voltage *3	PNSW3	SV_{CC} + 0.1	V
Control input allowable application voltage 0/1/2/3/4/5/6	$V_{CTL0/1/2/3/4/5/6}$	SV_{CC} + 0.1	V
Reference supply allowable application current	I_{REF}	–5	mA
Allowable application voltage to output voltage detection input 0	V_{VO0}	SV_{CC} + 0.1	V
Allowable application voltage to output voltage detection input D1	V_{DI}	SV_{CC} + 0.1	V
Error amplifier (0 to 6) allowable application voltage to input pin	$V_{IN0/1/2/3/4/5/6}$	– 0.2 to SV_{CC}	V
Error amplifier (dropper) allowable application voltage to input pin	V_{DEI}	– 0.2 to SV_{CC}	V
Low frequency setting pin input allowable application voltage *3	COSC	SV_{CC} + 0.1	V
Synchronous rectification stop pin input application voltage *3	STOP	SV_{CC} + 0.1	V
Total shutdown pin input allowable voltage *3	TOSH	SV_{CC} + 0.1	V
Allowable application voltage between PV_{CC2} and MO2	PVMO2	SV_{CC} + 0.1	V
Allowable application voltage between PV_{CC3} and MO3	PVMO3	SV_{CC} + 0.1	V

Note) *1: Except for the power dissipation, operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

*2: T_a = 85°C. For the independent IC without a heat sink. Note that applications must observe the derating curve for the relationship between the IC power consumption and the ambient temperature.

*3: Do not apply external currents or voltages to any pins not specifically mentioned.
For the circuit currents, '+' denotes current flowing into the IC, and '–' denotes current flowing out of the IC.

*4: t < 10 ms, V_{DS} < 5 V

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	SV_{CC}	4.5 to 5.5	V
	V_{BAT}	2.8 to 7.2	
	V_{BATL}	1.5 to 4.6	

■ Electrical Characteristics (Unless otherwise specified, $T_a = 25°C \pm 2°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage						
Reference voltage	V_{REF}	$I_{REF} = -0.1$ mA	1.256	1.269	1.282	V
Line regulation	Line	$SV_{CC} = 4.5$ V to 5.5 V	—	3	15	mV
Load regulation	Load	$I_{REF} = 0$ mA to −1.0 mA	−24	−12	—	mV
SV_{CC} low voltage protection						
Circuit operation start voltage	SV_{CCON}		3.8	4.0	4.2	V
Circuit operation stop voltage	SV_{CCOFF}		3.6	3.8	4.0	V
V_{BAT} low voltage protection						
Circuit operation start voltage	V_{BATLON}	At V_{BATL} input	1.331	1.418	1.505	V
Circuit operation stop voltage	$V_{BATLOFF}$	At V_{BATL} input	1.251	1.338	1.425	V
Circuit operation start voltage	V_{BATON}	At V_{BAT} input	2.05	2.28	2.51	V
Circuit operation stop voltage	V_{BATOFF}	At V_{BAT} input	2.00	2.23	2.46	V
Dropper amp. block						
Output sink current	I_{RS}	At $V_{BATL} = 3$ V input	8	16	—	mA
Output leak current	I_{RL}	At $V_{BATL} = 3$ V input	—	—	2	µA
Output block						
Output transistor N-ch. on resistance (ch.0)	R_{ON0}	$I_{DRV0} = 30$ mA	—	0.6	1.2	Ω
Output leak current (ch.0)	I_{L0}	$V_{DRV0} = 5.0$ V	—	—	2	µA
Output high voltage (ch.1, 4, 5, 6)	$V_{H1/4/5/6}$	$I_{OH} = -1$ mA	$PV_{CC}-0.1$	—	—	V
Output low voltage (ch.1, 4, 5, 6)	$V_{L1/4/5/6}$	$I_{OL} = 1$ mA	—	—	0.1	V
N-ch. on resistance (ch.1, 4, 5, 6)	$R_{N1/4/5/6}$	$I_O = 30$ mA	—	3	10	Ω
P-ch. on resistance (ch.1, 4, 5, 6)	$R_{P1/4/5/6}$	$I_O = -30$ mA	—	3	10	Ω
Low-side high output voltage (ch.2)	V_{LOH2}	$I_{OH} = -1$ mA	$PV_{CC}-0.1$	—	—	V
Low-side low output voltage (ch.2)	V_{LOL2}	$I_{OL} = 1$ mA	—	—	0.1	V
High-side high output voltage (ch.2)	V_{HOH2}	$I_{OH} = -1$ mA	$PV_{CC}-0.1$	—	—	V
High-side low output voltage (ch.2)	V_{HOL2}	$I_{OL} = 1$ mA	—	—	MO2+0.1	V
LO2 pin N-ch. on resistance (ch.2)	R_{2LN}	$I_O = 30$ mA	—	3	10	Ω
LO2 pin P-ch. on resistance (ch.2)	R_{2LP}	$I_O = -30$ mA	—	3	10	Ω
HO2 pin N-ch. on resistance (ch.2)	R_{2HN}	$I_O = 30$ mA	—	3	10	Ω
HO2 pin P-ch. on resistance (ch.2)	R_{2HP}	$I_O = -30$ mA	—	3	10	Ω

■ Electrical Characteristics (continued) (Unless otherwise specified, T_a = 25°C ± 2°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output block (continued)						
Low-side high output voltage (ch.3)	V_{LOH3}	I_{OH} = −1 mA	PV_{CC}−0.1	—	—	V
Low-side low output voltage (ch.3)	V_{LOL3}	I_{OL} = 1 mA	—	—	0.1	V
High-side high output voltage (ch.3)	V_{HOH3}	I_{OH} = −1 mA	PV_{CC}−0.1	—	—	V
High-side low output voltage (ch.3)	V_{HOL3}	I_{OL} = 1 mA	—	—	MO3+0.1	V
LO3 pin N-ch. on resistance (ch.3)	R_{3LN}	I_O = 30 mA	—	3	10	Ω
LO3 pin P-ch. on resistance (ch.3)	R_{3LP}	I_O = −30 mA	—	3	10	Ω
HO3 pin N-ch. on resistance (ch.3)	R_{3HN}	I_O = 30 mA	—	3	10	Ω
HO3 pin P-ch. on resistance (ch.3)	R_{3HP}	I_O = −30 mA	—	3	10	Ω
Ch.0 output maximum duty ratio	Du_{max0}	At V_{BATL} = 3 V input	79	85	91	%
Ch.1 output maximum duty ratio	Du_{max1}	At V_{BATL} = 3 V input	81	87	93	%
Ch.2/3 output maximum duty ratio	$Du_{max2/3}$	At V_{BATL} = 3 V input	78	85	92	%
Ch.4/5/6 output maximum duty ratio	$Du_{max4/5/6}$	At V_{BATL} = 3 V input	82	88	94	%
Oscillator						
Ch.0 start-up oscillation frequency 1	f_{ST1}	At V_{BATL} = 3 V input	110	270	430	kHz
Ch.0 start-up oscillation frequency 2	f_{ST2}	At V_{BAT} = 3 V input	110	270	430	kHz
Ch.0 start-up output duty ratio 1	Du_{ST1}	At V_{BATL} = 3 V input	45	53	61	%
Ch.0 start-up output duty ratio 2	Du_{ST2}	At V_{BAT} = 3 V input	46	54	62	%
Ch.0 to ch.6 oscillation frequency	F_{OUT} 0/1/2/3/4/5/6	CT = 180 pF, RT = 33 kΩ COSC = 0 V, V_{BATL} = 3 V	465	515	565	kHz
Ch.0 to ch.6 low oscillation frequency	FL_{OUT} 0/1/2/3/4/5/6	CT = 180 pF, COSC = 5 V RT = 33 kΩ, V_{BATL} = 3 V	15	25	35	kHz
Error amplifier (ch.0 to ch.6)						
Input threshold voltage IN0/1/2/3/4/5/6	V_{TH} 0/1/2/3/4/5/6		1.23	1.27	1.31	V
Input bias voltage IN0/1/2/3/4/5/6	I_B 0/1/2/3/4/5/6		− 0.25	− 0.15	—	µA
High-level output voltage EO0/1/2/3/4/5/6	V_{EH} 0/1/2/3/4/5/6		1.0	—	—	V
Low-level output voltage EO0/1/2/3/4/5/6	V_{EL} 0/1/2/3/4/5/6		—	—	0.2	V
Output source current EO0/1/2/3/4/5/6	I_{SO} 0/1/2/3/4/5/6		−28	−22.5	−17	µA
Output sink current EO0/1/2/3/4/5/6	I_{SI} 0/1/2/3/4/5/6		0.5	—	—	mA
Ch.0 short-circuit protection circuit block						
Standby pin voltage	V_{SCP0}	At V_{BATL} input or V_{BAT} input	—	—	0.1	V
Latch threshold voltage 1	V_{LTH01}	At V_{BATL} input	1.12	1.24	1.36	V
Latch threshold voltage 2	V_{LTH02}	At V_{BAT} input	1.07	1.217	1.31	V

■ Electrical Characteristics (continued) (Unless otherwise specified, $T_a = 25°C \pm 2°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Ch.0 short-circuit protection circuit block (continued)						
Pin voltage after latch operation	V_{SLT0}	At V_{BATL} input or V_{BAT} input	—	—	0.1	V
Charge current 1	I_{CHG01}	At V_{BATL} input, $V_{SCP0} = 0$ V	–2.92	–2.22	–1.52	µA
Charge current 2	I_{CHG02}	At V_{BAT} input, $V_{SCP0} = 0$ V	–3.16	–2.22	–1.28	µA
Ch.1 to ch.6 short-circuit protection circuit						
Pin voltage at standby	V_{SCP}		—	—	0.1	V
Timer threshold voltage ch.1 to ch.6	V_{LTH} 1/2/3/4/5/6		1.142	1.268	1.394	V
Pin voltage at latch operation ch.1 to ch.6	V_{SLT} 1/2/3/4/5/6		—	—	0.1	V
Charge current	I_{CHG1}	$V_{SCP} = 0$ V	–1.660	–1.282	–0.904	µA
Control						
Pin current CTL0/1/2/3/4/5/6	I_{CTL} 0/1/2/3/4/5/6	$V_{CTL} = 2.7$ V	–1	—	1	µA
Input high voltage CTL0/1/2/3/4/5/6	V_{CTLH} 0/1/2/3/4/5/6		2.7	—	—	V
Input low voltage CTL0/1/2/3/4/5/6	V_{CTLL} 0/1/2/3/4/5/6		—	—	0.3	V
Current consumption						
Startup average quiscent consumption current 1	I_{BATL}	Ch.0 with no outside-transistor At V_{BATL} input, SS0 = 0 V	—	500	700	µA
Startup average quiscent consumption current 2	I_{BAT}	Ch.0 with no outside-transistor At V_{BAT} input, SS0 = 0 V	—	450	650	µA
Average quiscent current consumption	$I_{CC(AV)}$	Ch.0 to ch.6 at output off	—	3	8	mA
Standby current 1	ISBL	CTL0 to CTL6 = 0 V ($V_{BATL} = 3$ V)	—	5	10	µA
Standby current 2	ISB	CTL0 to CTL6 = 0 V ($V_{BAT} = 3$ V)	—	5	10	µA
Operation mode switching block						
ch.2 P-ch./N-ch. configuration setting voltage		Refer to "■ Usage Note, 5" (page 20)	—	PV_{CC2}/ PV_{CC3}	—	V
ch.2 N-ch./N-ch. configuration setting voltage		Refer to "■ Usage Note, 5" (page 20)	—	MO2/ MO3	—	V
Synchronous rectification stop voltage			1.5	—	—	V
Synchronous rectification stop release voltage			—	—	0.3	V
Low oscillation-frequency setting voltage			1.5	—	—	V
Low oscillation-frequency release voltage			—	—	0.3	V
Total shutdown setting voltage			1.5	—	—	V
Total shutdown release voltage			—	—	0.3	V

Note) Unless otherwise specified, V_{BAT} (V_{BATL}) = 3 V, $SV_{CC} = PV_{CC1} = PV_{CC4} = 5$ V, $C_{REF} = 0.1$ µF

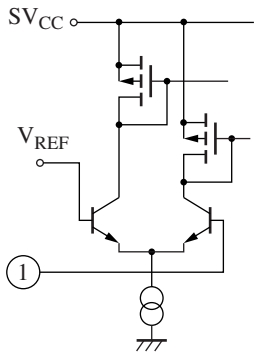
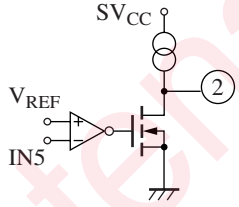
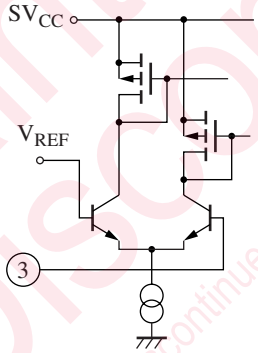
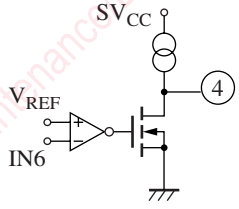
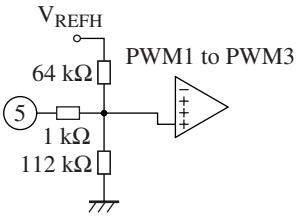
■ Electrical Characteristics (continued) (Unless otherwise specified, T_a = 25°C ± 2°C)

• Design reference data

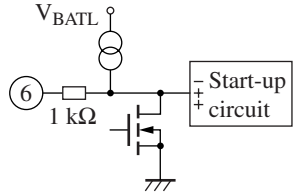
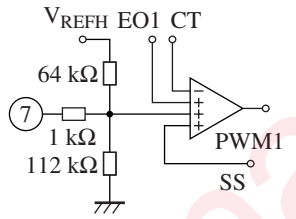
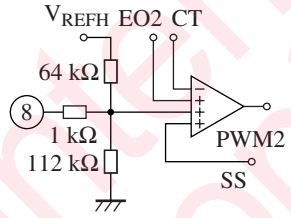
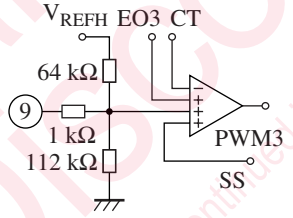
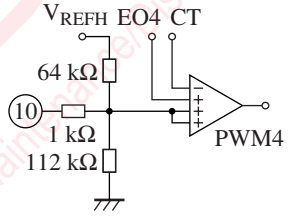
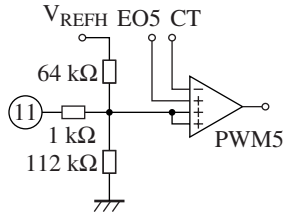
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Target value	Unit
Reference voltage				
V_{REF} temperature characteristics	V_{REFdt}	T_a = 0°C to 70°C	±1.0	%
SV_{CC} low voltage protection				
Voltage difference between operation start and stop (SV_{CC})	ΔSV_{CC}	$SV_{CCON} - SV_{CCOFF} > 0$	0.2	V
V_{BAT} low voltage protection				
Voltage difference between operation start and stop (V_{BATL})	ΔV_{BATL}	$V_{BATLON} - V_{BATLOFF} > 0$	0.07	V
Voltage difference between operation start and stop (V_{BAT})	ΔV_{BAT}	$V_{BATON} - V_{BATOFF} > 0$	0.05	V
Error amplifier (ch.0 to ch.6)				
V_{TH} temperature characteristics	V_{THdt}	T_a = 0°C to 70°C	±1.5	%
Open loop gain	A_V		60	dB
Oscillator				
Frequency supply voltage characteristics	f_{dV}	SV_{CC} = 4.5 V to 5.5 V RT = 33 kΩ, CT = 180 pF	±10	%
Frequency temperature characteristics	f_{dT}	T_a = –20°C to 85°C RT = 33 kΩ, CT = 180 pF	±3	%
Startup oscillator				
Frequency temperature characteristics output 1	f_{STT1}	T_a = 0°C to 70°C At V_{BATL} = 3 V input	±25	%
Frequency temperature characteristics output 2	f_{STT2}	T_a = 0°C to 70°C At V_{BAT} = 3 V input	±25	%
Supply voltage characteristics 1	f_{STVD1}	V_{BATL} = 1.5 V to 4.6 V	±20	%
Supply voltage characteristics 2	f_{STVD2}	V_{BAT} = 2.8 V to 7.2 V	±20	%
Short-circuit protection circuit				
Comparator threshold voltage (V_{BAT})	V_{THSB}	At V_{BATL} input	1.6	V
Comparator threshold voltage (SV_{CC})	V_{THSS}	At V_{BATL} input	1.6	V
Overvoltage protection circuit				
Overvoltage circuit operation voltage	V_{THS}	At V_{BATL} input	5.3	V
Thermal protection circuit				
Circuit operation stop temperature			125	°C
Assist driver circuit				
N-ch. on resistance	R_{OAN}		3	Ω
P-ch. on resistance	R_{OAP}		6	Ω

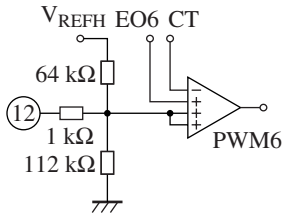
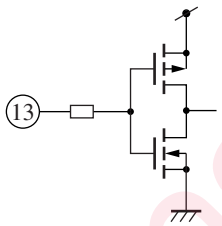
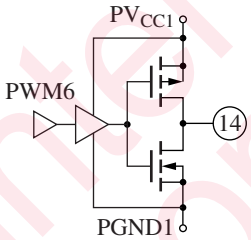
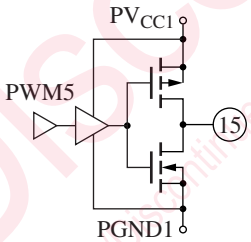
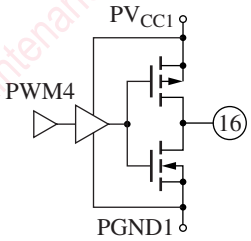
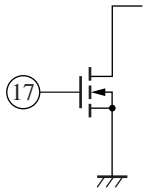
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	In/Out
1		IN5: Ch.5 error amplifier inverting input pin	In
2		EO5: Ch.5 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out
3		IN6: Ch.6 error amplifier inverting input pin	In
4		EO6: Ch.6 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out
5		SS: Ch.1 to ch.3 common soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In

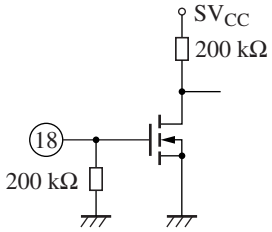
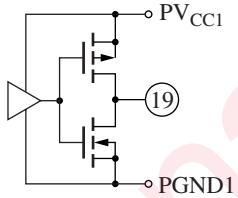
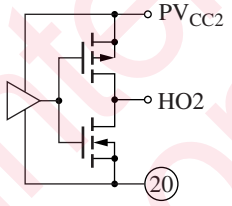
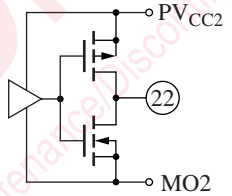
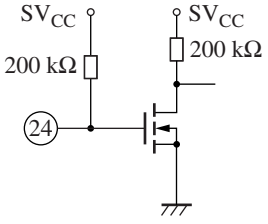
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
6		SS0: Ch.0 soft-start time setting pin V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
7		SS1: Ch.1 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
8		SS2: Ch.2 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
9		SS3: Ch.3 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
10		SS4: Ch.4 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
11		SS5: Ch.5 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In

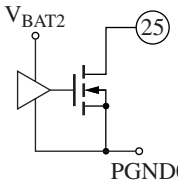
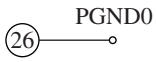
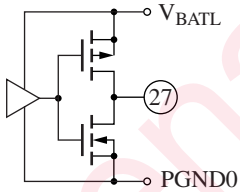
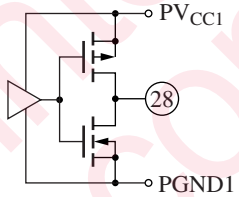
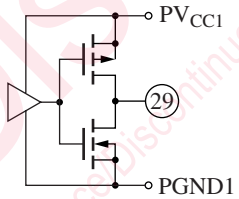
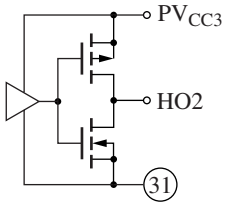
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
12		SS6: Ch.6 soft-start time setting pin Connect a capacitor between this pin and GND. • Potential dividing resistance for threshold setting 64 kΩ (typ.) 112 kΩ (typ.) V_{REFH} (typ.) = (306 kΩ/200 kΩ) × V_{REF} (typ.)	In
13		PNSW2: Ch.2; HO2 high-side output FET P-ch., N-ch. switching pin Driven by HO2, FET P-ch., N-ch. switching over • High: P-ch. (connect to PV_{CC2}) Low: N-ch. (connect to MO2)	In
14		DRV6: Ch.6 output pin CMOS type output ON resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
15		DRV5: Ch.5 output pin CMOS type output ON resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
16		DRV4: Ch.4 output pin CMOS type output ON resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
17		CTL0: Ch.0 on/off controlt pin	In

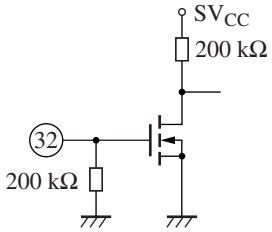
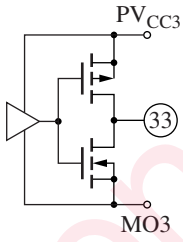
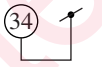
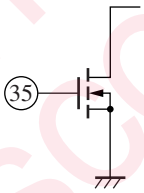
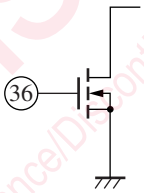
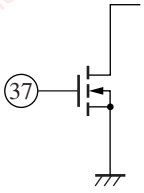
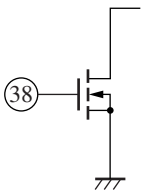
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
18		STOP: Synchronous rectification stop pin When STOP is high, ch.2 and ch.3 synchronous rectification stop.	In
19		LO2: Ch.2 output pin (low-side) Synchronous rectification system output stage CMOS type output circuit On resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
20		MO2: Ch.2 output pin (high-side) Low potential side Synchronous rectification system output stage CMOS type output circuit	Out
21		PV_{CC1}: Output system supply voltage application pin 1 Power supply pin for ch.1, ch.2/L, ch.3/L, ch.4 to ch.6 driver	—
22		HO2: Ch.2 output pin (high-side) High potential side Synchronous rectification system output stage CMOS type output circuit On resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
23		PV_{CC2}: Output system supply voltage application pin 2 Power supply pin for ch.2 US driver	—
24		TOSH: Total shutdown pin When TOSH is high, all outputs are stopped if the output is short circuited.	In

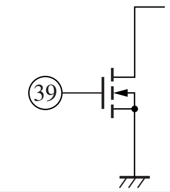
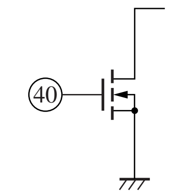
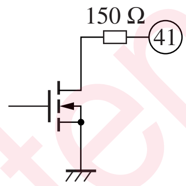
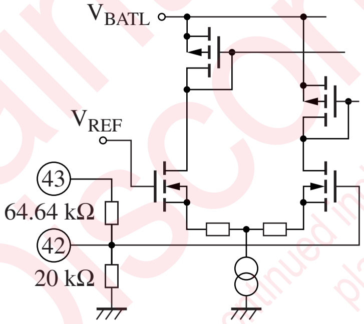
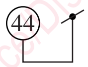
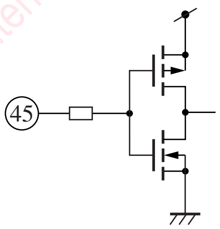
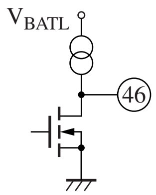
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
25		DRV0: Power supply output pin for ch.0 IC (5 V) drive For internal power supply of this IC Open drain type On resistance N-ch.: 1.2 Ω (max.)	Out
26		PGND0: Output system grounding pin 0 Ch.0 output	—
27		ASIST: Power supply auxiliary output pin for ch.0 IC drive For internal power supply of this IC Connect in parallel with DRV0 for ch.0 capacity increase On resistance (design reference data) N-ch.: 3 Ω (typ.) P-ch.: 6 Ω (typ.)	—
28		Out1: Ch.1 output pin CMOS type output circuit On resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
29		LO3: Ch.3 output pin (low-side) Synchronous rectification system output stage CMOS type output circuit On resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
30		PGND1: Output system ground pin 1 Grounding pin for ch.1, ch.2/L, ch.3/L, ch.4 to ch.6 driver	—
31		MO3: Ch.3 output pin (high-side) Low potential side Synchronous rectification system output stage CMOS type output circuit	Out

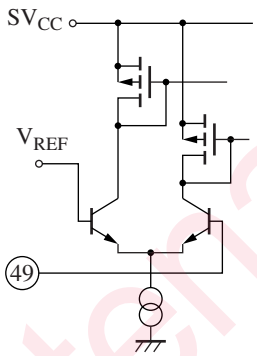
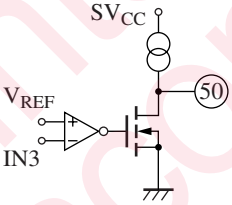
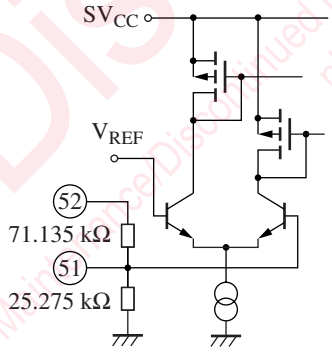
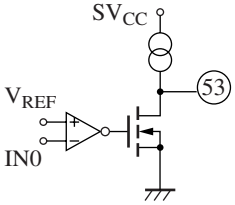
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
32		COCS: Low frequency setting pin When COCS is high, the triangular wave oscillation frequency is switched over to low frequency (20 kHz/typ.)	In
33		HO3: Ch.3 output pin (high-side) High potential side Synchronous rectification system output stage CMOS type output circuit On resistance N-ch.: 10 Ω (max.) P-ch.: 10 Ω (max.)	Out
34		PV_{CC3}: Output system supply voltage application pin 3 Power supply pin for ch.3 high-side driver	—
35		CTL1: Ch.1 on/off start-up input pin	In
36		CTL2: Ch.2 on/off control pin	In
37		CTL3: Ch.3 on/off control pin	In
38		CTL4: Ch.4 on/off control pin	In

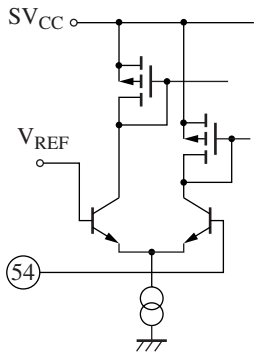
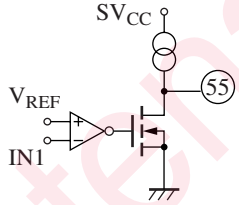
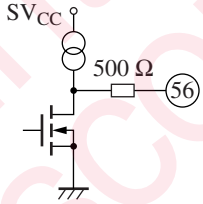
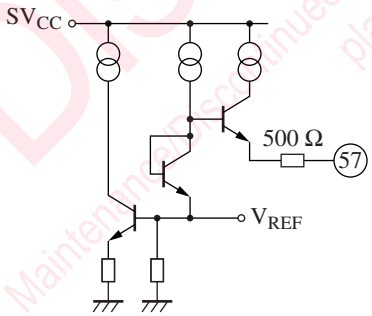
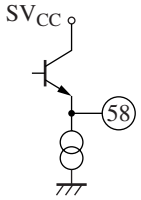
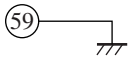
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
39		CTL5: Ch.5 on/off control pin	In
40		CTL6: Ch.6 on/off control pin	In
41		DO: Ch.0 dropper error amplifier output pin When connecting the power supply to V_{BAT} pin, connect this pin with the base of output PNP transistor of regulator amplifier which stabilizes the power supply voltage SV_{CC} for ch.0: IC drive at 5 V. Then ch.0 output voltage is controlled.	Out
42		DEI: Ch.0 dropper error amplifier inverting input pin	In
43		DI: Ch.0 dropper output monitor pin The output voltage is set by the potential dividing resistance between (DI) and SGND. • Potential dividing resistance 64.64 kΩ (typ.) 20 kΩ (typ.)	In
44		SV_{CC}: Signal system supply voltage application pin	—
45		PNSW3: Ch.3; HO3 high-side output FET P-ch., N-ch. switching pin Driven by HO3, FET P-ch., N-ch. switching over • High: P-ch. (connect to PV_{CC3}) Low: N-ch. (connect to MO3)	In
46		SCP0: Time constant setting capacitor connection pin for ch.0 output short-circuit protection	Out

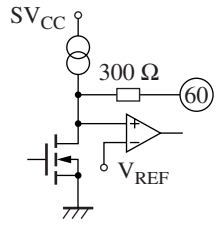
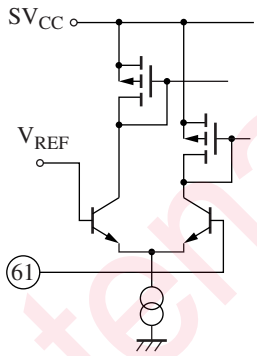
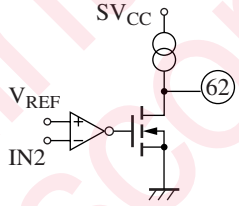
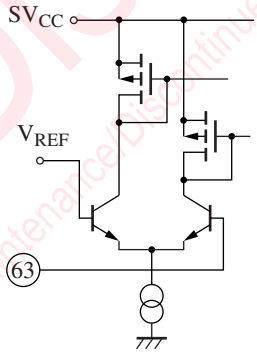
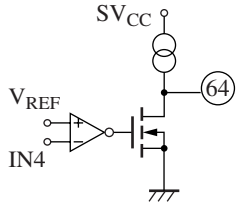
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
47		V_{BATL}: Battery voltage application pin (low voltage)	—
48		V_{BAT}: Battery voltage application pin (high voltage)	—
49		IN3: Ch.3 error amplifier inverting input pin	In
50		EO3: Ch.3 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out
51		IN0: Ch.0 error amplifier inverting input pin	In
52		VO0: Ch.0 output voltage detection pin The output voltage is set by the potential dividing resistance between VO0 and SGND • Potential dividing resistance 71.135 kΩ (typ.) 25.275 kΩ (typ.)	In
53		EO0: Ch.0 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
54		IN1: Ch.1 error amplifier inverting input pin	In
55		EO1: Ch.1 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out
56		CT: Triangular wave oscillation frequency setting capacitor connection pin	Out
57		RT: Triangular wave oscillation frequency setting resistor connection pin	Out
58		V_{REF}: Reference voltage output pin	Out
59		SGND: Signal system grounding pin	—

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	In/Out
60		SCP: Time constant setting capacitor connection pin for ch.1 to ch.6 output short-circuit protection	Out
61		IN2: Ch.2 error amplifier inverting input pin	In
62		EO2: Ch.2 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out
63		IN4: Ch.4 error amplifier inverting input pin	In
64		EO4: Ch.4 error amplifier output pin Source current: −20 µA (typ.) Sink current: 0.5 mA (min.)	Out

■ Usage Notes

1. V_{BAT} rise up speed with V_{BAT} pin (pin 48) input

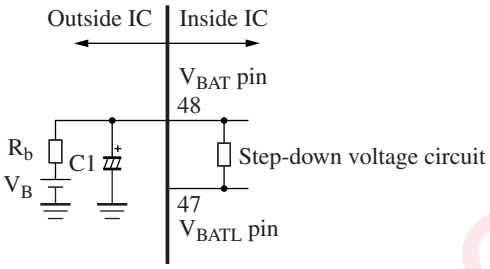


Figure 1. Peripheral circuit for V_{BAT} pin and V_{BATL} pin

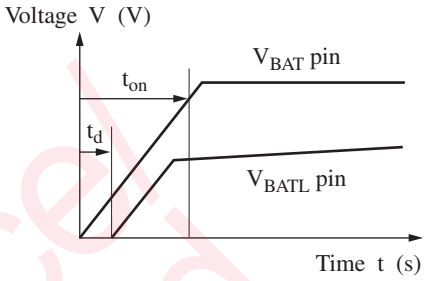


Figure 2. V_{BATL} pin voltage in the V_{BAT} pin input mode

A voltage propagation delay time (t_d) from V_{BAT} pin (pin 48) to V_{BATL} (pin 47) is made at the battery input to pin 48. If the voltage rise speed (t_{on}) of the V_{BAT} pin exceeds the specified value, the voltage also exceeds the pin's withstand voltage. Therefore, you are requested to use a bypass capacitor (C1 in fig.1) of more than 0.055 µF capacitance.

The related equation is:

From $A < 3 \times C1 \times (R_b + Z_{IC})$

$C1 > A/(3 \times (R_b + Z_{IC})) \approx A / (3 \times Z_{IC})$. Equation (1)

C1 can be calculated by substituting 500 µs for A and 3 kΩ for Z_{IC} in the equation (1)

Thus C1 > 0.055 µF

C1: Bypass capacitor

R_b: Internal impedance of the battery

Z_{IC}: Internal impedance of the IC ≈ 3 kΩ

A : Minimum time not exceeding the withstand voltage of V_{BAT} pin at V_{BAT} pin input: 500 µs

2. V_{BAT} voltage fall speed at V_{BAT} pin (pin 48) input

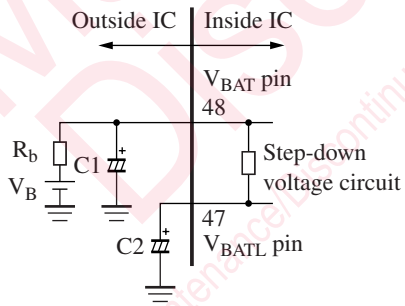
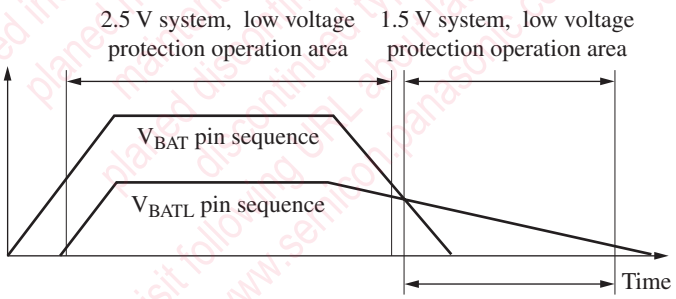


Figure 3. Peripheral circuit for V_{BAT} pin and V_{BATL} pin



*: There is a possibility that malfunction occurs depending on the capacity value of C1 and C2.

Figure 4. Example of operation error

■ Usage Notes (continued)

2. V_{BAT} voltage fall speed at V_{BAT} pin (pin 48) input (continued)

• On operation of the low voltage protection circuit when battery is applied to V_{BAT} pin.

V_{BAT} low voltage protection circuit operating voltage (V_{UOFF}) characteristic in a battery voltage fall time of pin 48 is likely to go wrong operation area depending on the capacitance of C1 and C2. (See Figure 4.) Therefore, use it based on the relation of (C1/C2) > 2 000.

The calculation equation is as follows:

V_{BAT} pin (pin 48) fall time> V_{BATL} pin (pin 47) fall time leads to:

$3 \times C1 \times Z_{HIC} > 3 \times C2 \times Z_{LIC}$

$(C1/C2) > (Z_{LIC}/Z_{HIC}) \approx (Z_{LIC}/R)$ ..... (1)

C1: V_{BAT} pin bypass capacitor
C2: V_{BATL} pin capacitor
R_b: Internal impedance of the battery
Z_{HIC}: Internal impedance of the IC measured from V_{BAT}
Z_{LIC}: Internal impedance of the IC measured from V_{BATL}
R: Load without battery (V_B) ≈ 5 Ω (worst case)

You can calculate (C1/C2) > 2 000 using the equation (1).

Example) For C2 = 0.1 µF, you can get C1 = 200 µF.

3. This control IC is designed to operate by receiving ch.0 DC-DC output voltage under a low input voltage operation.

For this reason, since its protection circuit is designed on the basis of the above operation, do not adopt any using method other than the application circuit examples. (Ex: The using method of directly applying the voltage to SV_{CC})

4. Power dissipation

The power dissipation P of this IC is proportional to the supply voltage. It also changes depending on the output load of ch.0, and the FET input capacitance and the oscillation frequency of ch.1 to ch.6. After referring to the P_D — T_a curve on its sheet No., use the IC under its allowable power dissipation on the basis of the following equation (Reference expression)

$$P = (SV_{CC} - V_{BE_{Q1}} - \frac{V_{OUT1} \times I_{OUT1} \times R_{OUT}}{h_{FE_{Q1}} \times V_{BAT}}) \times \frac{(V_{OUT1} - V_{BAT}) \times I_{OUT}}{h_{FE_{Q1}} \times V_{BAT}} + 6 \times SV_{CC} \times C_{iss} \times f + SV_{CC} \times I_{CC} + V_{BAT} \times I_{BAT} < P_D$$

V_{BEQ1}: Ch.0 NPN transistor base-emitter voltage
$h_{FE_{Q1}}$: Ch.0 NPN transistor current amplification ratio
R_{OUT} : Ch.0 NPN transistor bias current limiting resistance
C_{iss} : Ch.1 to ch.6 output connection FET input capacitance
f : Oscillation frequency
I_{CC} : SV_{CC} , PV_{CC1} , PV_{CC2} and PV_{CC3} pin current
I_{BAT} : V_{BAT} or V_{BATL} pin current

5. PNSW2: Ch.2 high-side P-ch., N-ch. switching pin

- In the case of P-ch., connect to PV_{CC2}
- In the case of N-ch., connect to MO2

PNSW3: Ch.2 high-side P-ch., N-ch. switching pin

- In the case of P-ch., connect to PV_{CC3}
- In the case of N-ch., connect to MO3

■ Application Notes

[1] Functional outline descriptions

1. Functional outline description figure

<Start>

1) After power supply connection, turn on the control pin CTL0.
2) PWM control operates to step-up the supply voltage and this voltage is applied to SV_{CC} pin.
3) When SV_{CC} becomes higher than 4.2 V, the oscillation changes over from the internal oscillator to the triangular wave oscillator and SV_{CC} is at 5 V. This becomes the power supply for the entire IC and the whole IC starts its operations.

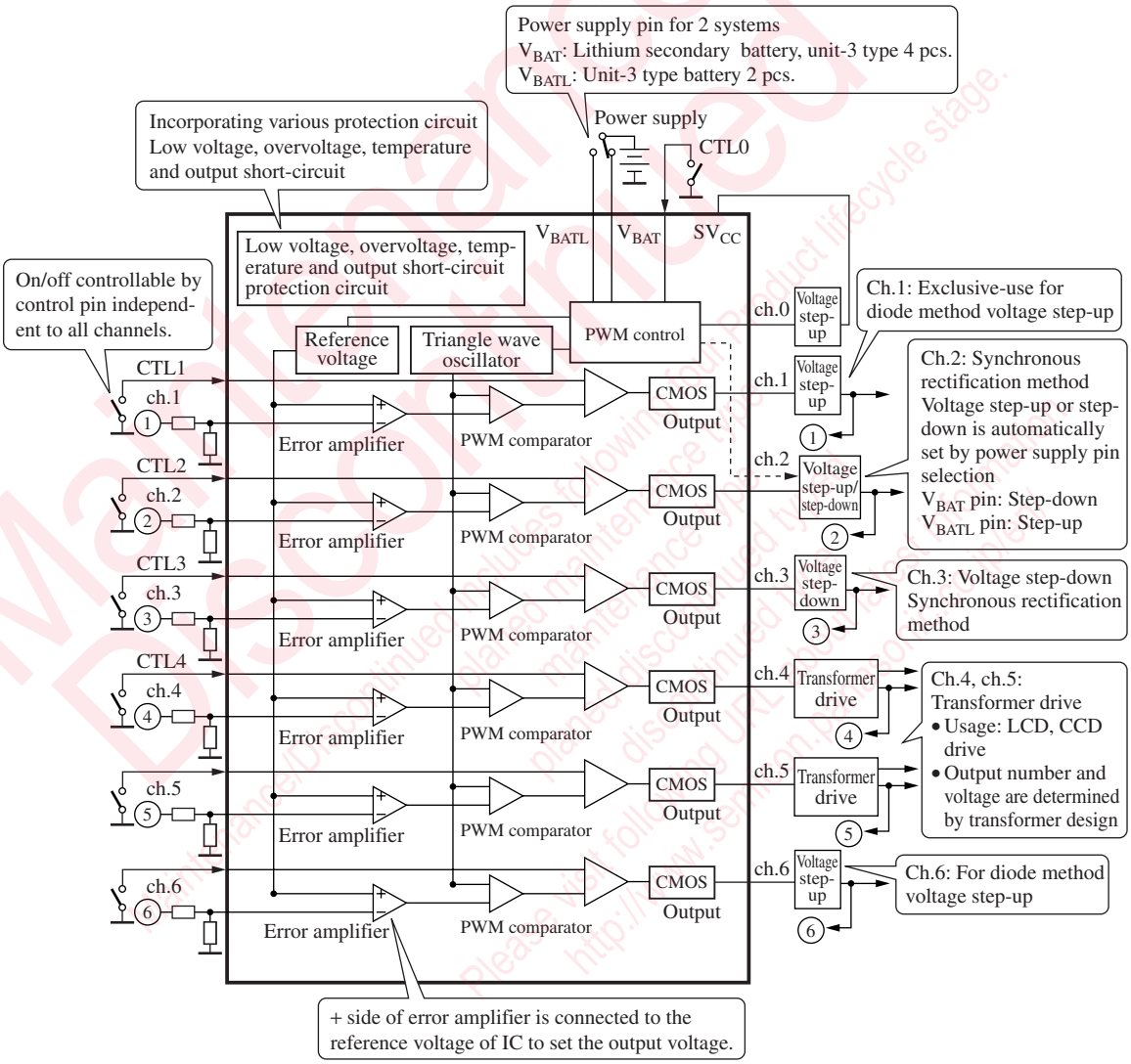


Figure 1. Configuration example

Note) Voltage set-up: Transform to a voltage higher than supply voltage
Voltage step-down: Transform to a voltage lower than supply voltage

■ Application Notes (continued)

[1] Functional outline descriptions (continued)

2. Outline of rise time operation (Refer to the rise time timing chart on the next page)

1) Connect the power supply to V_{BATL} pin (pin 47) (1.5 V to 4.6 V) or V_{BAT} pin (pin 48) (2.8 V to 7.2 V).

2) When ch.0 (power supply for IC drive) control pin (CTL0: Pin17) is turned on, the pulse voltage output is given to DRV0 pin (pin 25) by the PWM control circuit and the voltage of IC power supply pin SV_{CC} (pin 44) rises.

- Since the timer of the short-circuit protection circuit for ch.0 operates for the period until ch.0 error amplifier output voltage (EO0: pin 53) stabilizes, consideration should be given to the rise setting of each part. (SCP0 pin voltage increases due to the charging of timer setting capacitor connected to SCP0 pin (pin 46)). (Refer to "[2] Functional Descriptions of Each Block 6. Timer latch type short-circuit protection circuit block for ch.0")
- IC output pin voltage of each channel is not generated until each CTL pin is turned on.

3) After turning on the control pin of each channel, the PWM output pulse voltage is given from IC output pin of each channel and the power supply circuit output voltage of each channel is generated.

- Since the timer of the short-circuit protection circuit for ch.1 to ch.6 operates (SCP pin: pin 60 voltage increase) for the period until the error amplifier output voltage of each channel (EO1 to EO6) stabilizes, consideration should be given to the rise setting of each part.
  (Refer to "[2] Functional descriptions of each block 7. Timer latch type short-circuit protection circuit block for ch.1 to ch.6")

4) If any one of the power supply circuit output pin voltages of ch.1 to ch.6 drops in the steady-state due to overloading or short circuiting, the error amplifier output voltage of relevant channel increases and the timer of the short-circuit protection circuit for ch.1 to ch.6 operates.

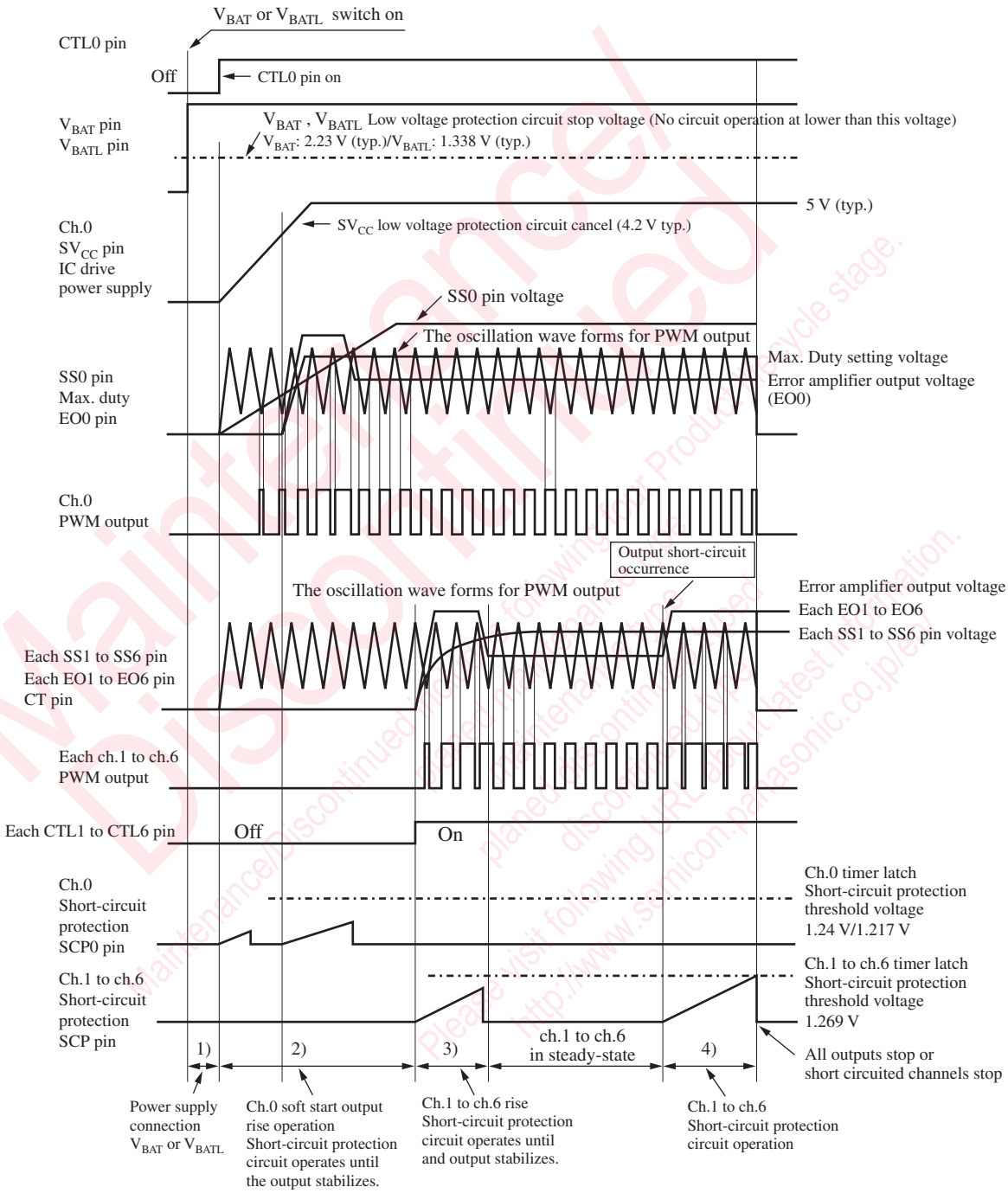
- If SCP pin voltage becomes a value higher than the threshold, ch.1 to ch.6 PWM output pulse stops so as to turn off the power supply circuit.
  (1) When TOSH pin (pin 24) is high: All channels stop simultaneously.
  (2) When TOSH pin (pin 24) is low: Only the short circuited channel stops.
  (Refer to "[2] Functional descriptions of each block 7. Timer latch type short-circuit protection circuit block for ch.1 to ch.6")

5) If SV_{CC} voltage drops to a point under 4.0 V due to overloading or short circuiting, the PWM pulse of ch.1 to ch.6 stops. Moreover the timer of the short-circuit protection circuit for ch.0 starts, and the voltage of the terminal SCP0 rises when the output of EO0 becomes more than the threshold voltage. The PWM pulse of ch.0 stops when the voltage of the terminal SCP0 becomes more than the threshold voltage. Ch.0 PWM pulse stops so as to turn off the power supply circuit.
(Refer to "[2] Functional descriptions of each block 6. Timer latch type short-circuit protection circuit block for ch.0")

■ Application Notes (continued)

[1] Functional outline descriptions (continued)

3. Rising timing chart (typical chart) 1

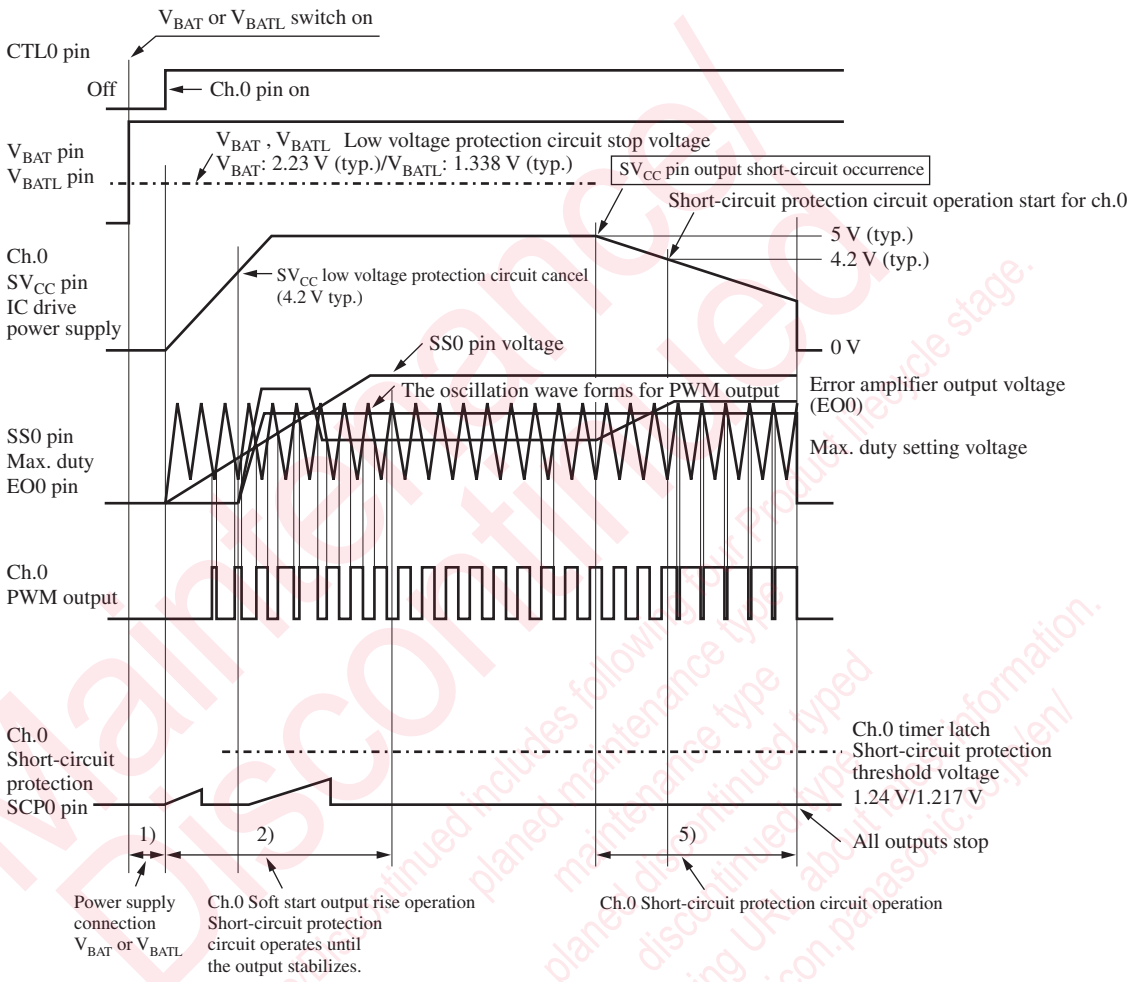


Note) For 1) to 4), refer to the description on the previous page.

■ Application Notes (continued)

[1] Functional outline descriptions (continued)

4. Rising timing chart (typical chart) 2: Short-circuit protection circuit operation for ch.0



[2] Function descriptions of each block

1. Reference voltage block

This block consists of band gap circuit and provides 1.26 V (typ.) reference voltage output with a temperature compensation accuracy of ±1%.

The reference voltage is stabilized at a supply voltage (SV_{CC}) over 4.2 V (typ.). This voltage is used as the reference voltage for error amplifier 0 to 6, the regulator amplifier and the short-circuit protection circuit, etc.

2. Triangular wave oscillation block

1) PWM operation

After ch.0 (Built-in IC power supply) start up, the triangular wave with high wave value of approx. 1.40 V and low wave value of approx. 0.55 V by the timing capacitor on CT pin (pin 56) and RT pin (pin 57) connection resistor is generated, and the connection is made inside the IC to the non-reverse input of PWM comparator of each channel.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

2. Triangular wave oscillation block (continued)

2) PWM operation (continued)

$$f_{OSC} = \frac{1}{t_1 + t_2} = \frac{I_O}{2 \times C_T \times (V_{CTH} - V_{CTL})}$$

$$I_O = 4 \times \frac{V_{RT}}{R_T} = 4 \times \frac{V_{REF}}{R_T}$$

$$V_{CTH} - V_{CTL} = 0.85 \text{ V}$$

$$f_{OSC} \approx \frac{1}{0.34 \times C_T \times R_T} \quad [\text{Hz}]$$

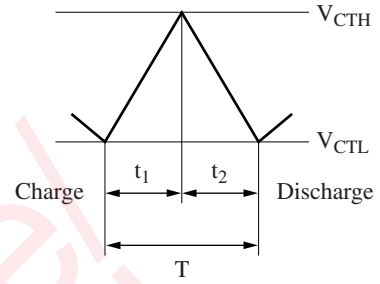


Figure 2. Triangular oscillation waveform

However, since the above equations are for the calculation when the oscillation frequency of the product specifications is at 515 kHz, the time for loosting charge if the frequency is variable, the amount of overshoot and under shoot are not taken into consideration.

When the frequency is variable, the calculation value obtained from the above equations is just a standard. Confirm the final result with the actual equipment.

Notes) When setting the oscillation frequency, the recommended value for the timing capacitor connected to CT pin (pin 56) is 180 pF and the resistor to RT pin (pin 57) is 33 kΩ.

3) Frequency change-over

It is possible to change over the triangular oscillation frequency by COCS pin (Pin32) setting.

(1) COCS pin is high: Oscillation frequency decreases (25 kHz typ.)

(2) COCS pin is low: Oscillation frequency normal (515 kHz typ.)

3. V_{BAT} , V_{BATL} low voltage protection circuit block

This part protects the system from breakdown or degradation due to a malfunction control in the transition state of V_{BAT} or V_{BATL} start and stop.

1) V_{BAT} input time

For the period until V_{BAT} pin (pin 48) voltage reaches 2.28 V (typ.) in its rise time, and when it goes below 2.23 V in its fall time, ch.0 (internal power supply of IC) output is completely stopped by cutting off the bias to the startup oscillation circuit.

2) V_{BATL} input time

For the period until V_{BATL} pin (pin 47) voltage reaches 1.418 V (typ.) in its rise time, and when it goes below 1.338 V in its fall time, ch.0 (internal power supply of IC) output is completely stopped by cutting off the bias to the startup oscillation circuit.

4. SV_{CC} low voltage protection circuit block

This part protects the system from breakdown or degradation due to a malfunction control in the generation transition state of the internal power supply of IC (SV_{CC}) by the ch.0 (Built-in IC power supply) start and stop.

For the period until SV_{CC} pin voltage (ch.0 output voltage) (pin 44) reaches 4.2 V (typ.) in its rise time, the output drive transistor is cut off (100% quiescent period) by setting SCP0 pin (pin 46), each SS pin (pin 7 to pin 12) and each EO pin (pin 55, pin 62, pin 50, pin 64, pin 2 and pin 4) at 0 V.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

4. SV_{CC} low voltage protection circuit block (continued)

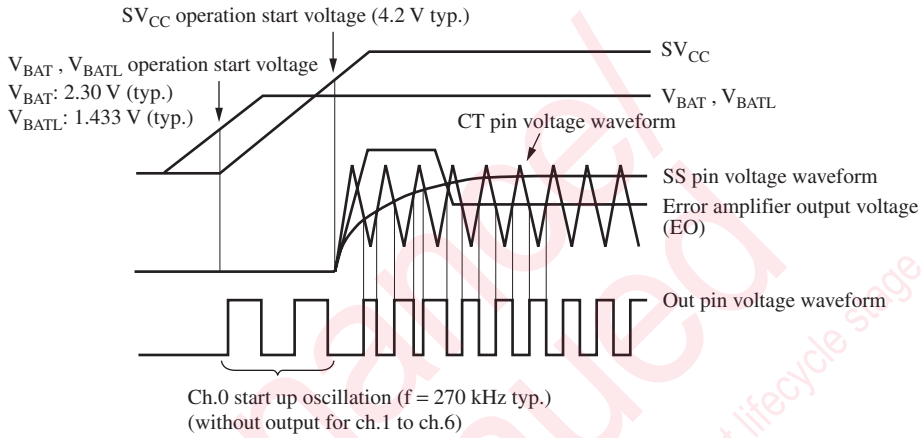


Figure 3. Low voltage protection circuit operation timing chart at V_{BAT} , V_{BATL} and SV_{CC} start time (Typical chart)

5. Error amplifier block

This part is the error amplifier for NPN transistor input. It detects the output voltage from the DC-DC converter and inputs the amplified signal to PWM comparator.

The non-reverse input of each channel (reference side) is set at 1.26 V (typ.) of the internal reference voltage. It is possible to carry out an arbitrary gain setting and phase compensation by the connection of a resistor and capacitor between EO pin and IN pin of each channel.

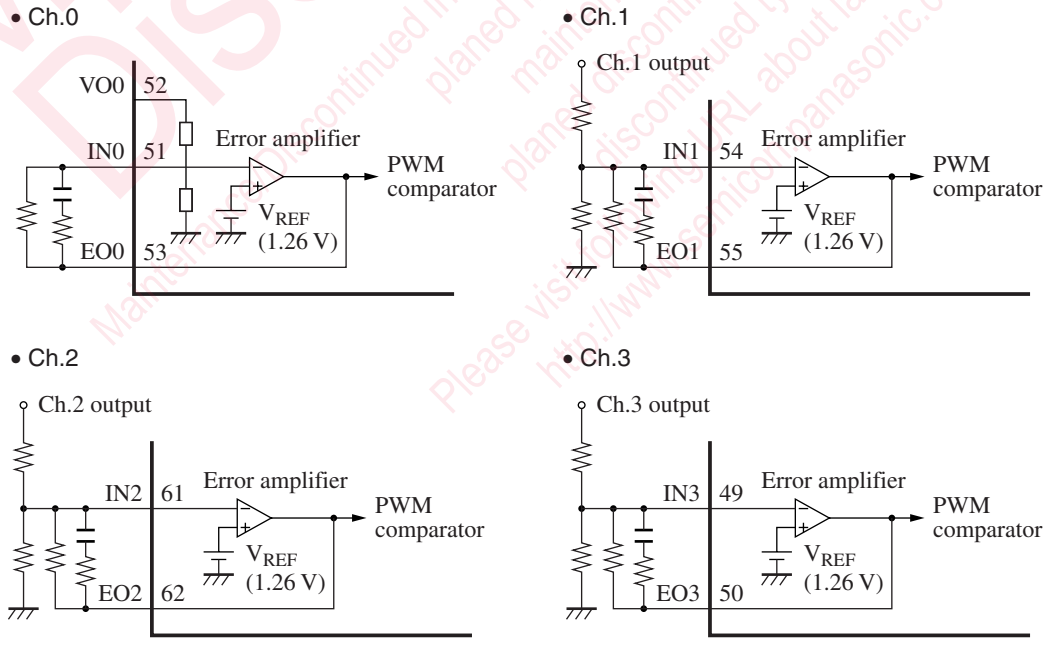


Figure 4. Connection of each channel error amplifier

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

5. Error amplifier block (continued)

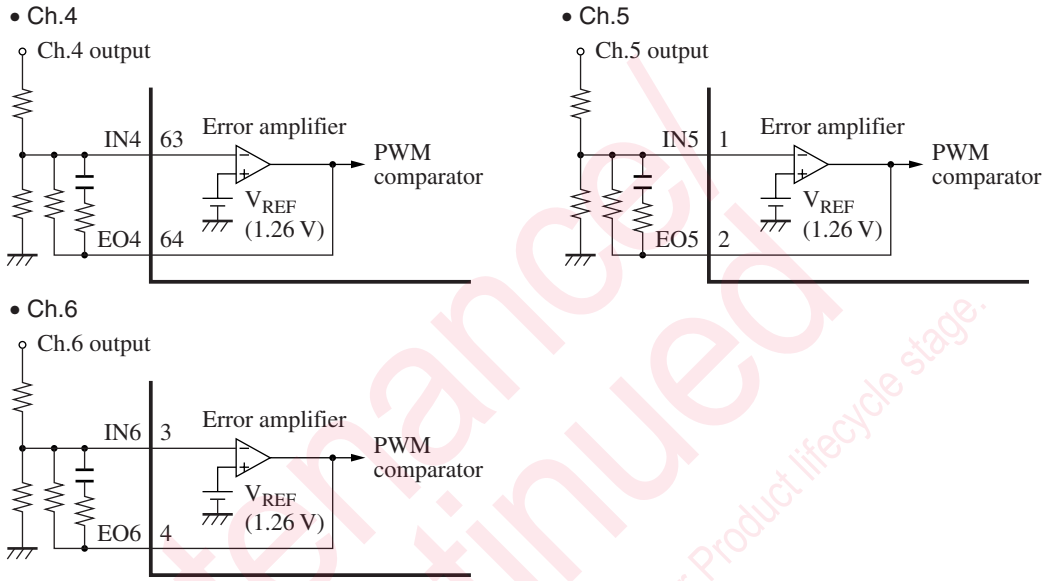


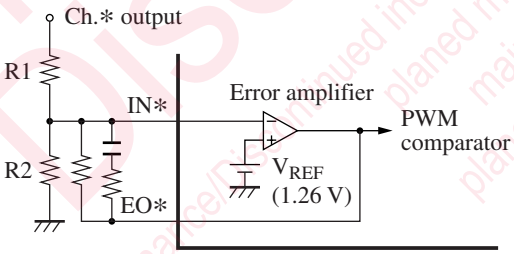
Figure 4. Connection of each channel error amplifier (continued)

1) Ch.0 part output voltage setting

Ch.0 has a built-in voltage setting resistor so that the output voltage is set at 5.0 V (typ.).

2) Ch.1 to ch.6 part output voltage setting

The voltage for ch.1 to ch.6 can be set by the connection of external voltage setting resistors as shown in the following diagram.



$$V_{OUT} = V_{REF} \times \frac{R1 + R2}{R2} \quad [V]$$

$$= 1.26\ V \times \frac{R1 + R2}{R2} \quad [V]\ (typ.)$$

Figure 5. Output voltage setting

6. Timer latch type short-circuit protection circuit block for ch.0

This block protects an external main switching device, flywheel diode and choke coil from breakdown or degradation if ch.0 output is maintained in an overloading or short circuiting condition for a certain period of time.

This protection circuit recognizes a drop of ch.0 output, which is the IC's SV_{CC} power supply, as short circuiting and operates the protection circuit.

If ch.0 output voltage (SV_{CC}) drops and goes below the latch threshold voltage described later, the timer circuit is operated by the output reversing of the short-circuit detection comparator (S.C.P. comp.), and the protection enable capacitor externally attached to SCP0 pin (Pin46) starts charging.

Unless ch.0 output voltage (SV_{CC}) returns to the normal voltage range ($SV_{CC} > 4.2$ V) until the voltage of this capacitor reaches;

with V_{BATL} input: 1.24 V (typ.)

with V_{BAT} input: 1.217 V (typ.),

the latch circuit is set, and the output drive transistor is cut off, and the quiescent period becomes 100%.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

6. Timer latch type short-circuit protection circuit block for ch.0 (continued)

Also, this short-circuit protection circuit stops all of them from ch.1 to ch.6 because of ch.0 output, that is SV_{CC} , is short-circuit. The short-circuit protection can be canceled by either the following 1) or 2) method.

1) Once reduce V_{BATL} (pin 47) or V_{BAT} (pin 48) potential to a voltage below the lower threshold voltage limit of V_{BAT} , V_{BATL} low voltage protection circuit, and restart .
2) Bringing down CTL0 pin (pin 17) to low-level, and restart.

Note) When the power supply is started up, it is recognized as short-circuit state so that SCP0 pin voltage (pin 46) starts charging. For this reason, it is necessary to set SCP0 pin capacitance so as to start up DC-DC converter output voltage before the IC sets the short-circuit detection and latch circuit

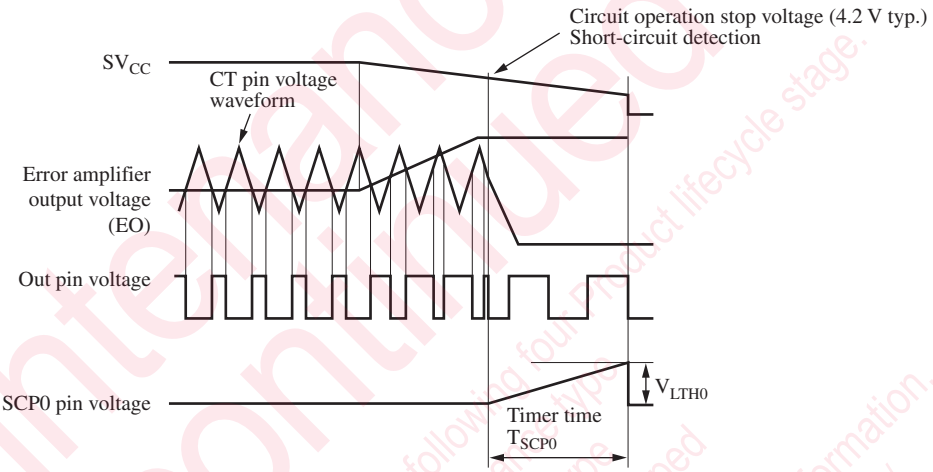


Figure 6. Ch.0 output short-circuit protective operation timing chart (Typical chart)

<V_{BATL} input time>

$$T_{SCP0} = \frac{C_{SCP0} \times V_{LTH0}}{I_{CHG0}} = \frac{C_{SCP0} \times 1.24}{2.22\ \mu A} = \frac{C_{SCP0} \times 10^6}{1.79}\ [s]\ (typ.)$$

<V_{BAT} input time>

$$T_{SCP0} = \frac{C_{SCP0} \times V_{LTH0}}{I_{CHG0}} = \frac{C_{SCP0} \times 1.217}{2.22\ \mu A} = \frac{C_{SCP0} \times 10^6}{1.82}\ [s]\ (typ.)$$

∗C_{SCP0}: SCP0 pin connection capacitance
I_{CHG0}: SCP0 pin charge current

7. Timer latch type short-circuit protection circuit block for ch.1 to ch.6

1) This block protects an external main switching device, flywheel diode and choke coil from breakdown or degradation if each output is maintained in an overloading or short circuiting condition for a certain period of time. This protection circuit detects short-circuit by the output signal of each error amplifier.

If the output voltage of DC-DC converter drops and any one of the pin voltages of EO1 to EO6 (pin 55, pin 62, pin 50, pin 64, pin 2 and pin 4) exceeds 1.6 V (typ.), the timer circuit is operated by the output reversing of the short-circuit detection comparator (S.C.P. comp.), and the protection enable capacitor externally attached to SCP pin (pin 60) starts charging. Unless the error amplifier output voltage returns to the normal voltage range until the voltage of this capacitor reaches 1.268 V (typ.), the latch circuit is set, the output drive transistor is cut off and the quiescent period becomes 100%.

The short-circuit protection can be canceled by either the following 1) or 2) method.

(1) Once reduce V_{BATL} (pin 47) or V_{BAT} (pin 48) potential to a voltage below the lower threshold voltage limit of V_{BAT} , V_{BATL} low voltage protection circuit, and restart .
(2) Bring down CTL0 pin (pin 17) to low-level, and restart.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

7. Timer latch type short-circuit protection circuit block for ch.1 to ch.6 (continued)

   2) Total shutdown setting

      TOSH pin (pin 24) setting allows the selection of channels whose operation is stopped by the short-circuit protection circuit, either only short-circuit channel or all ch.0 to ch.6 channels.

      (1) TOSH pin (pin 24) is high: All channels shutdown

      (2) TOSH pin (pin 24) is low: Only short-circuit channel shutdown

      Note) When the power supply is started up, it is recognized as short-circuit state so that SCP pin voltage (pin 60) starts charging. For this reason, it is necessary to set SCP pin capacitance so as to start up DC-DC converter output voltage before the IC sets the short-circuit detection and latch circuit. A care must be taken especially when applying the softstart because the startup time extends.

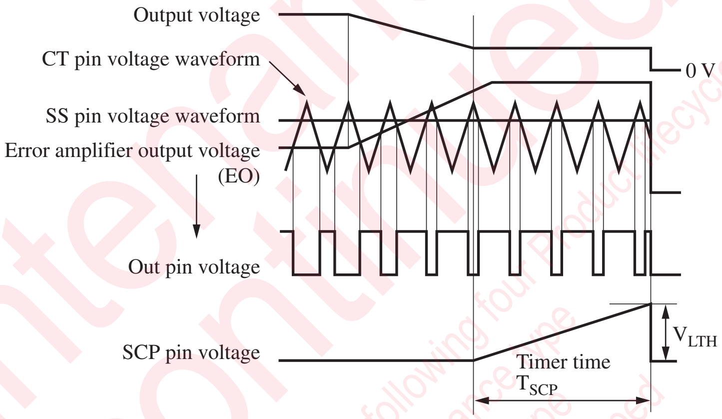


Figure 7. Ch.1 to ch.6 output short-circuit protective operation timing chart (Typical chart)

$$T_{SCP} = \frac{C_{SCP} \times V_{LTH}}{I_{CHG}} = \frac{C_{SCP} \times 1.268}{1.282\ \mu A} = \frac{C_{SCP} \times 10^6}{0.989}\ [s]\ (typ.)$$

$*C_{SCP}$: SCP pin connection capacitance

I_{CHG}: SCP pin charge current

8. PWM comparator block

   PWM comparator controls the output pulse On period according to the input voltage.

   It puts the output pin of each channel in high-level and turns on the output transistor during the period when the triangular wave voltage of CT pin (pin 56) is lower than each SS∗ pin voltage and each EO∗ pin voltage.

   The maximum duty ratio is internally set by the triangular wave voltage and each SS∗ pin setting voltage.

   The maximum duty ratio is internally set at 88% (typ.) for all channels. However, it can be set at any value from 0% to 100% by the connection of a resistor between each SS pin and SGND (pin 59) or V_{REF} pin (pin 58).

   Also, the softstart which gradually expands the On period of the output pulse at the startup time operates by a capacitor connection between each SS pin and GND.

   • Max-Du setting equation

$$MaxDu = \frac{V_{SS} - V_{CTL}}{V_{CTH} - V_{CTL}} \times 100\ [\%]$$

where,

$$V_{SS} = V_{REF}' \times \frac{RO2}{RO1 + RO2}\ [V]$$

$V_{CTH} = 1.40$ V (typ.)

$V_{CTL} = 0.55$ V (typ.)

$V_{REF}' = 1.94$ V (typ.)

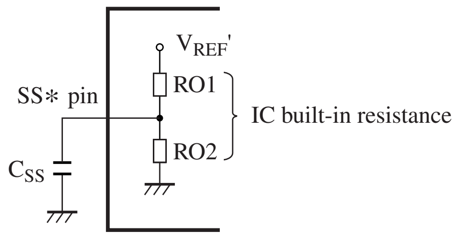


Figure 8. Output Du and softstart setting diagram

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

8. PWM comparator block (continued)

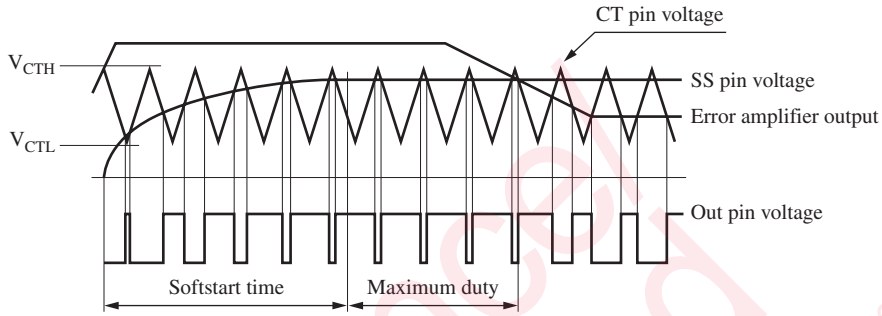


Figure 9. PWM comparator operation and softstart operation timing chart (Typical chart)

Actually measured value and calculated value may not agree due to the delay of PWM comparator operation and the shift of V_{CTH} , V_{XTL} value of triangular wave oscillation. Adjust with actually mounted circuit board.

9. Ch.0 output part

1) Operational explanation

(1) Output circuit is open drain configuration.

(2) Exclusive-use for voltage step-up circuit

(3) Output stage has built-in power MOSFET (N-ch.) and on-state resistance is 1.2 Ω (max.).

(4) Exclusive-use for IC's internal power supply and the setting voltage is 5 V.

- The circuit block of ch.0 output part and the peripheral circuit example are shown in figure 10.

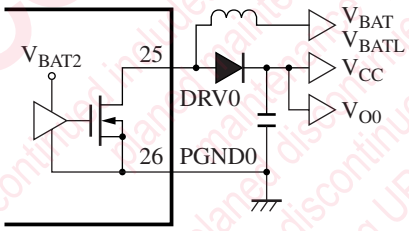


Figure 10

10. Ch.1 output part

1) Operational explanation

(1) Output circuit is CMOS configuration.

- The circuit block of ch.1 output part and the peripheral circuit example are shown in figure 11.

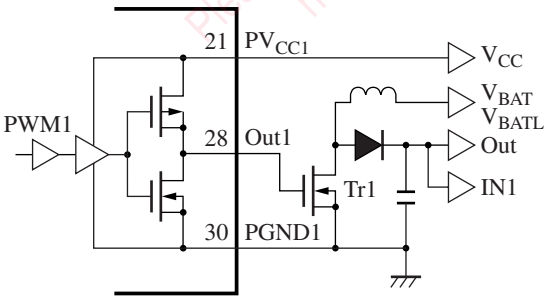


Figure 11

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

11. Ch.2 output block

1) Operational explanation

(1) The output circuit is synchronous rectification method.

(2) The output stage for both HO2 (pin 22) and LO2 (pin 19) is CMOS configuration.

(3) It is set up at either the voltage step-up or step-down by the selection of the the supply voltage connection pin.

i) If the power supply is connected to V_{BATL} pin (pin 47), it is set at the voltage step-up.

ii) If the power supply is connected to V_{BAT} pin (pin 48), it is set at the voltage step-down.

(4) The setting of PNSW2 pin (pin 13) allows the selection of either N-ch. or P-ch. for the HO2 output driven external SW device.

i) PNS pin is high: P-ch. FET drive (connect to PV_{CC2})

ii) PNS pin is low: N-ch. FET drive (connect to MO2)

(5) The synchronous rectification is stopped by STOP pin (pin 18) setting.

i) STOP pin is high: Synchronous rectification stops

a) Voltage step-up time: HO2 output stops

b) Voltage step-down time: LO2 output stops

At that time, a rectification diode is required in place of the stopped FET.

ii) STOP pin is low: Synchronous rectification operates

The synchronous rectification stop is performed at the same time with ch.3.

2) Voltage step-up time

• Ch.2 output part circuit block and the voltage step-up time peripheral circuit example are shown in figure 12.

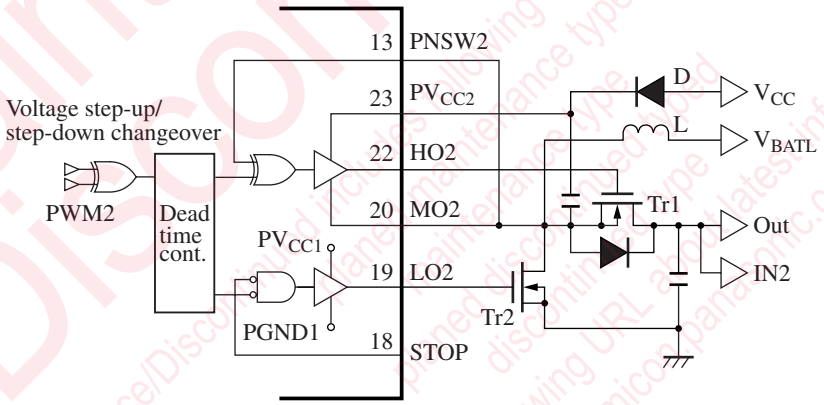


Figure 12

(1) PWM output voltage

• The PWM output voltage is supplied from HO2 pin (pin 22) and LO2 pin (pin 19) to drive FET Tr1 and Tr2 respectively. Both pin voltages are as shown in figure 13.

• When Tr2 is On, the current flows through the path from the power supply (V_{BATL}) → coil → Tr2 → GND and the electric power is supplied to the coil. At this time, Tr1 is Off.

• Next when Tr2 is Off, Tr1 goes On, and the electric power accumulated in the coil is supplied to the output through Tr1.

(2) Quiescent period

• The PMW output voltages given from HO2 pin (pin 22) and LO2 (pin 19) are provided with the quiescent period t_d in which both become off state as shown in figure 13. This is provided for the prevention of simultaneous turning On of Tr1 and Tr2.

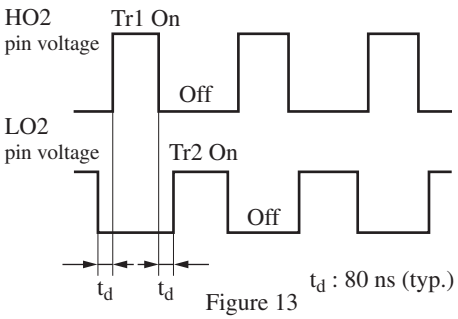


Figure 13

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

11. Ch.2 output block (continued)

3) Voltage step-down time

- Ch.2 output part circuit block and the voltage step-down time peripheral circuit example are shown in figure 14.

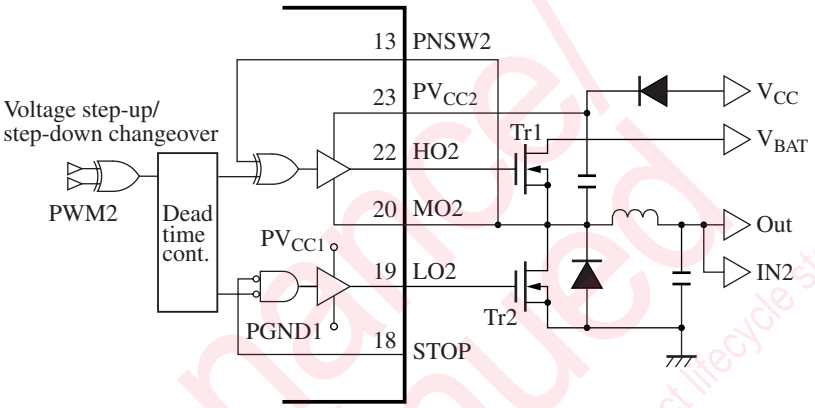


Figure 14

(1) PWM output voltage

- The PWM output voltage is supplied from HO2 pin (pin 22) and LO2 pin (pin 19) to drive FET Tr1 and Tr2 respectively. Both pin voltages are as shown in figure 15.
- When Tr1 is On, the current flows through the path from the power supply (V_{BAT}) → Tr1 → coil → output and the electric power is supplied to the coil. At this time, Tr2 is off.
- Next when Tr1 is Off, Tr2 goes On, and the electric power accumulated in the coil is supplied to the output through Tr2.

(2) Quiescent period

- As same as the case of voltage step-up, the PMW output voltages given from HO2 pin (pin 22) and LO2 (pin 19) are provided with the quiescent period td in which both become Off state as shown in figure 15. This is provided for the prevention of simultaneous turning on of Tr1 and Tr2.

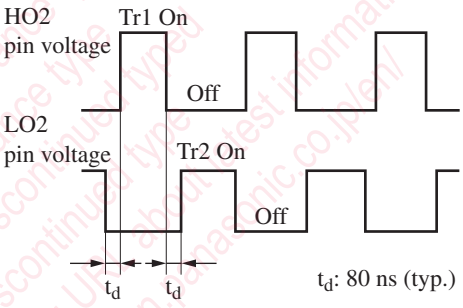


Figure 15

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

11. Ch.2 output block (continued)

4) Bootstrap circuit

A bootstrap circuit is provided for driving N-ch. MOSFET: Tr1. This bootstrap circuit is provided for keeping the gate-source voltage of N-ch. MOSFET: Tr1 over the gate threshold voltage by increasing high-level of HO2 pin (pin 22) to a voltage higher than Vcc when N-ch. MOSFET: Tr1 is On.

(1) Operational explanation of bootstrap circuit

i) Voltage step-up case

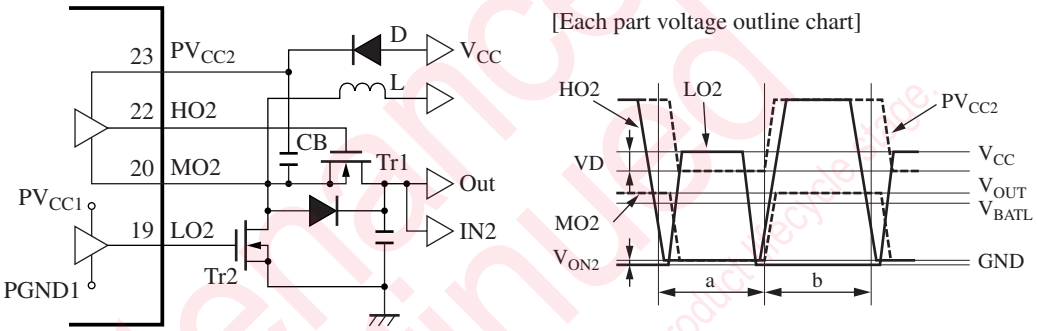


Figure 16

a) Off period of N-ch MOSFET (Tr1)

- N-ch MOSFET (Tr2) is On (LO2: High) in the period when Tr1 is Off, and the source voltage (V_{MO2}) of Tr1 corresponds to a portion of Tr2 (V_{ON2}) voltage drop which is approximately equal to GND voltage. (∗1)
- When the forward voltage of diode D is V_D, the potential VPV_{CC2} of IC's internal output circuit power supply PV_{CC2} becomes;

  $VPV_{CC2} = V_{CC} - V_D$

  and the charge voltage V_{CB} of capacitor CB for bootstrap becomes;

  $V_{CB} = (VPV_{CC2}) - V_{ON2} \approx V_{CC} - V_D$

b) On-period of N-ch MOSFET (Tr1)

- Tr2 is Off in the period when Tr1 is On, and the current is being supplied from the power supply V_{BATL} to the output through coil L and Tr1. When the voltage drop of Tr1 is V_{ON1}, the source voltage (V_{MO2}) of Tr1 becomes;

  $V_{MO2} = V_{OUT} + V_{ON1}$

  and it approximately equal to the output voltage (V_{OUT}). (∗1)
- The potential VPV_{CC2} of IC's internal output circuit power supply PV_{CC2} is maintained because the capacitor for bootstrap CB is being charged for the period t1 so that it becomes;

  $VPV_{CC2} = V_{MO2} + V_{CB}$
- The voltage (V_{HO2}) of the output pin HO2 of IC is at the voltage approximately equal to the power supply voltage PV_{CC2} since the output circuit inside the IC is high. Therefore, V_{GS1} which is the gate-source voltage of Tr1 is;

  $V_{GS1} = V_{HO2} - V_{MO2} \approx VPV_{CC2} - V_{MO2} = V_{CB}$

  here, V_{CB} is charged at $V_{CC} - V_D$ during the Off period of Tr1 so that the voltage sufficient to turn On Tr1 can be maintained.

Note) ∗1 : It is desirable to use MOSFET with low On resistance for Tr1/Tr2.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

11. Ch.2 output block (continued)

4) Bootstrap circuit (continued)

(1) Operational explanation of bootstrap circuit (continued)

ii) Voltage step-down case

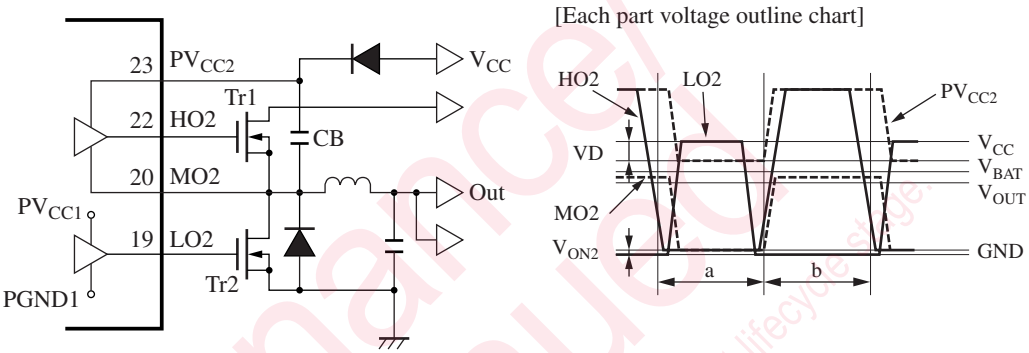


Figure 17

a) Off period of N-ch MOSFET (Tr1)

- N-ch MOSFET (Tr2) is On (LO2: High) in the period when Tr1 is Off, and the source voltage (V_{MO2}) of Tr1 corresponds to a portion of Tr2 (V_{ON2}) voltage drop which is approximately equal to GND voltage. (*2)
- When the forward voltage of diode D is V_D , the potential VPV_{CC2} of IC's internal output circuit power supply PV_{CC2} becomes;

  $VPV_{CC2} = V_{CC} - V_D$

  and the charge voltage V_{CB} of capacitor CB for bootstrap becomes;

  $V_{CB} = (VPV_{CC2}) - V_{ON2} \approx V_{CC} - V_D$

b) On-period of N-ch MOSFET (Tr1)

- Tr2 is Off in the period when Tr1 is On, and the current is being supplied from the power supply V_{BAT} to the output through coil L and Tr1. When the voltage drop of Tr1 is V_{ON1} , the source voltage (V_{MO2}) of Tr1 becomes;

  $V_{MO2} = V_{BAT} - V_{ON1}$

  and it approximately equal to the output voltage (V_{BAT}). (*2)
- The potential VPV_{CC2} of IC's internal output circuit power supply PV_{CC2} is maintained because the capacitor for bootstrap CB is being charged for the period t1 so that it becomes;

  $VPV_{CC2} = V_{MO2} + V_{CB}$
- The voltage (V_{HO2}) of the output pin HO2 of IC is at the voltage approximately equal to the power supply voltage PV_{CC2} since the output circuit inside the IC is high. Therefore, V_{GS1} which is the gate-source voltage of Tr1 is;

  $V_{GS1} = V_{HO2} - V_{MO2} \approx VPV_{CC2} - V_{MO2} = V_{CB}$

  here, V_{CB} is charged at $V_{CC} - V_D$ during the Off period of Tr1 so that the voltage sufficient to turn On Tr1 can be maintained.

Note) *2 : It is desirable to use MOSFET with low On resistance for Tr1/Tr2.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

11. Ch.2 output block (continued)

4) Bootstrap circuit (continued)

(2) Bootstrap circuit usage notes

i) Operating power supply voltage range

Use an operating power supply voltage with a sufficient margin since PV_{CC2} pin voltage (pin 23) exceeds V_{CC} as shown below when N-ch. MOSFET (Tr1), being a switching device, is turned on.

$VPV_{CC2} \approx V_{MO2} + V_{CC} - V_D \approx V_{CC} + V_{OUT} + V_{ON1} - V_D$: Voltage step-up time

$VPV_{CC2} \approx V_{MO2} + V_{CC} - V_D \approx V_{CC} + V_{BAT} - V_{ON1} - V_D$: Voltage stap-down time

ii) Bootstrap capacitor constant setting

The bootstrap capacitor pulls up PV_{CC2} pin voltage to a point over V_{CC} by capacitance coupling with the source side of N-ch. MOSFET when it is turn-on. At this time, the bootstrap capacitor is discharged by the gate drive current of N-ch. MOSFET. A too small capacitance value setting for the bootstrap capacitor may cause the efficiency drop due to switching loss increase.

Therefore, a sufficiently large capacitance setting value should be taken as compared with the gate input capacitance.

12. Ch.3 output block

1) Operational explanation

(1) The output circuit is synchronous rectification method.

(2) The output stage is CMOS configuration for both HO3 (pin 33) and LO3 (pin 29).

(3) Exclusive-use for voltage step-down circuit.

(4) The setting of PNSW3 pin (pin 45) allows the selection of either N-ch. or P-ch. for the HO3 output driven external SW device.

i) PNSW pin is high: P-ch. FET drive (connect to PV_{CC3})

ii) PNSW pin is low: N-ch. FET drive (connect to MO3)

(5) LO3 (pin 29) output is turned off and the synchronous rectification is stopped by setting of STOP pin (pin 18).

i) STOP pin is high: Synchronous rectification stops

At that time, a rectification diode is required in place of the stopped FET.

ii) STOP pin is low: Synchronous rectification operates

The synchronous rectification stop is carried out simultaneously with ch.2.

(6) The circuit operation is similar to ch.2 voltage step-down circuit.

(7) The quiescent period is also similar to ch.2 voltage step-down circuit.

(8) The bootstrap circuit is also similar to ch.2 voltage step-down circuit.

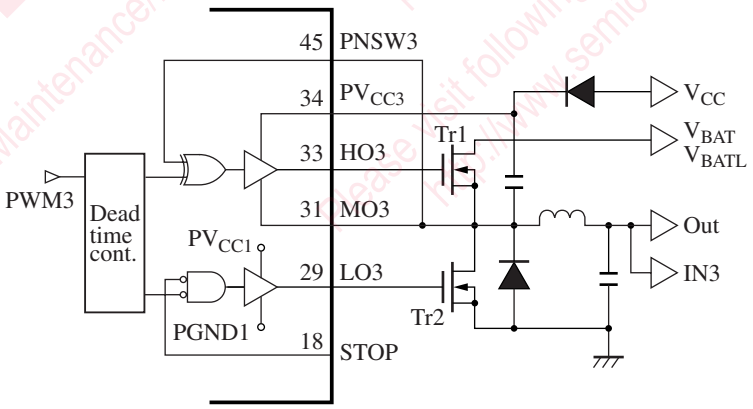


Figure 18

Refer to the items for ch.2 for the concrete circuit operations.

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

13. Ch.4 output block

1) Operational explanation

(1) Output circuit is CMOS configuration.

The circuit block of ch.4 to ch.6 output part and the peripheral circuit example are shown in figure 19.

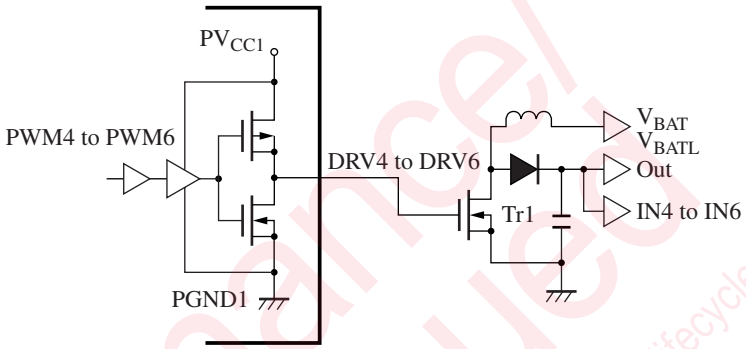


Figure 19

14. CTL block

Each ch.0 to ch.6 channel turns On each time by bringing CTL∗ pin (CTL0 to CTL6) for each ch.0 to ch.6 to high-level. Each channel turns Off if CTL∗ pin is brought to low-level (< 0.3 V).

1) The maximum applied voltage for each CTL∗ pin: Bring it under SV_{CC} (pin 44) + 0.1 V
2) This IC's ch.0 output is IC's power supply (SV_{CC}) so that On/Off operation of other channels can not be performed unless ch.0 is started up.

15. Regulator amplifier block

1) Operational explanation

(1) A regulator amplifier is built in this IC which makes up a three terminal voltage regulator by the connection of an external PNP transistor to DI pin (pin 43) and DO pin (pin 41).
Ch.0 output is exclusive-use for voltage step-up circuit control. Therefore, if the power supply input is from V_{BAT} pin, it is possible to maintain ch.0 output in stabile state by using the regulator amplifier as shown below.

(2) Output circuit is open drain configuration.

(3) Output sink current is 20 mA (typ.).

The circuit block of the regulator output part and the peripheral circuit example are shown in figure 20.

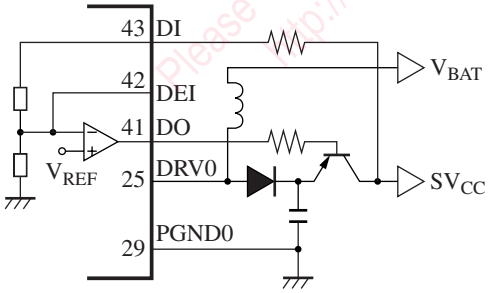


Figure 20

■ Application Notes (continued)

[2] Functional descriptions of each block (continued)

16. Overvoltage protection circuit block

The protection circuit stops ch.0 output completely by cutting off the bias to the startup oscillation circuit if V_{BATL} pin (pin 47) voltage exceeds 4.2 V (typ.).

17. Thermal protection circuit block

This IC is incorporating the built-in temperature detection circuit. The protection circuit stops all channel outputs completely by cutting off the bias to the startup oscillation circuit if the temperature inside the IC exceeds 125°C (typ.).

18. Assist driver circuit block

1) Operational explanation

(1) The output circuit is CMOS configuration.

(2) As the supplement to ch.0, an external power transistor is connected and used in parallel with ch.0. The output part circuit block is shown in figure 21.

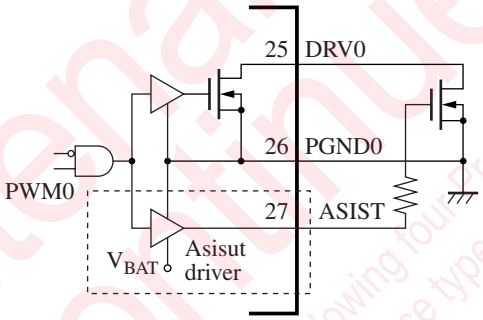
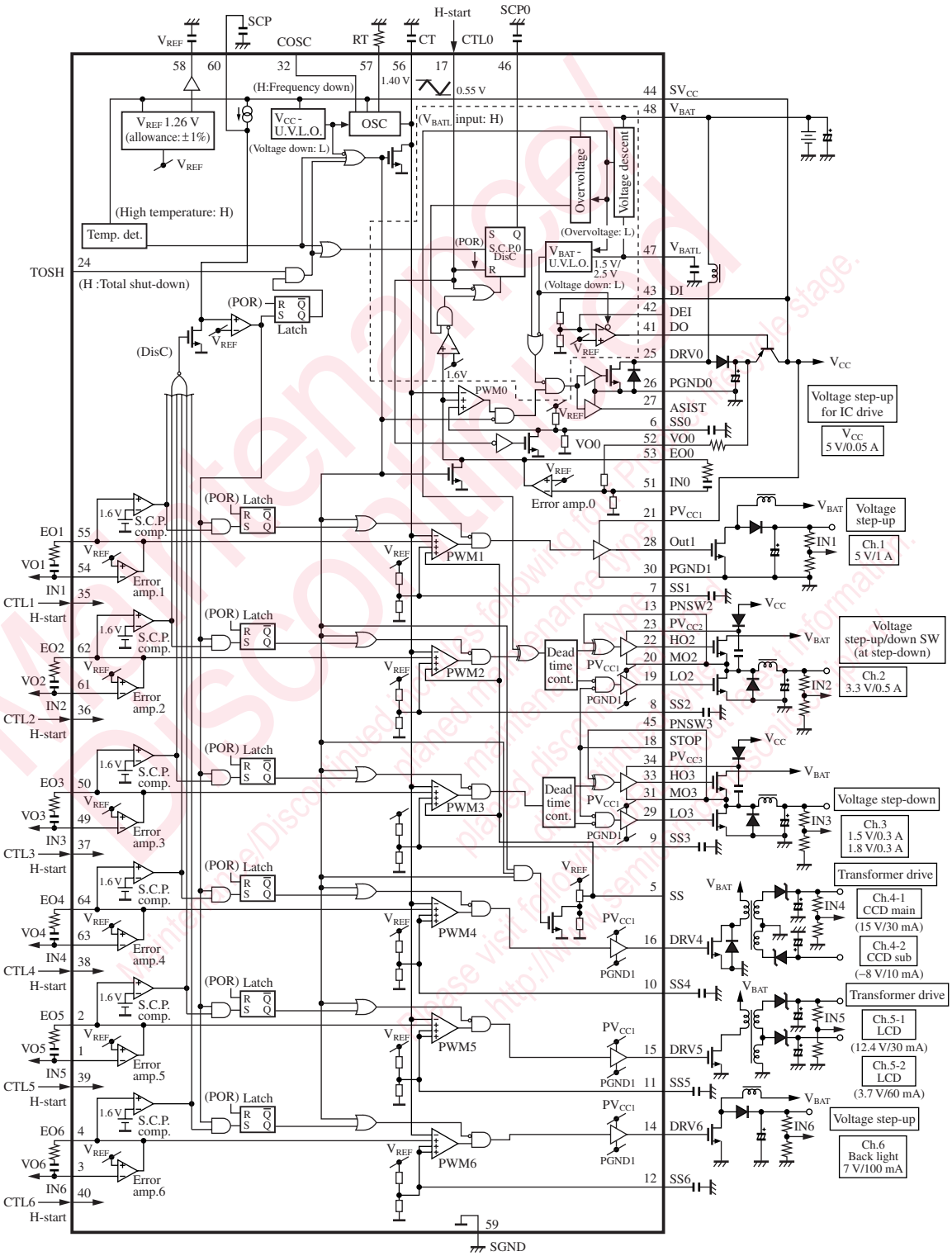


Figure 21

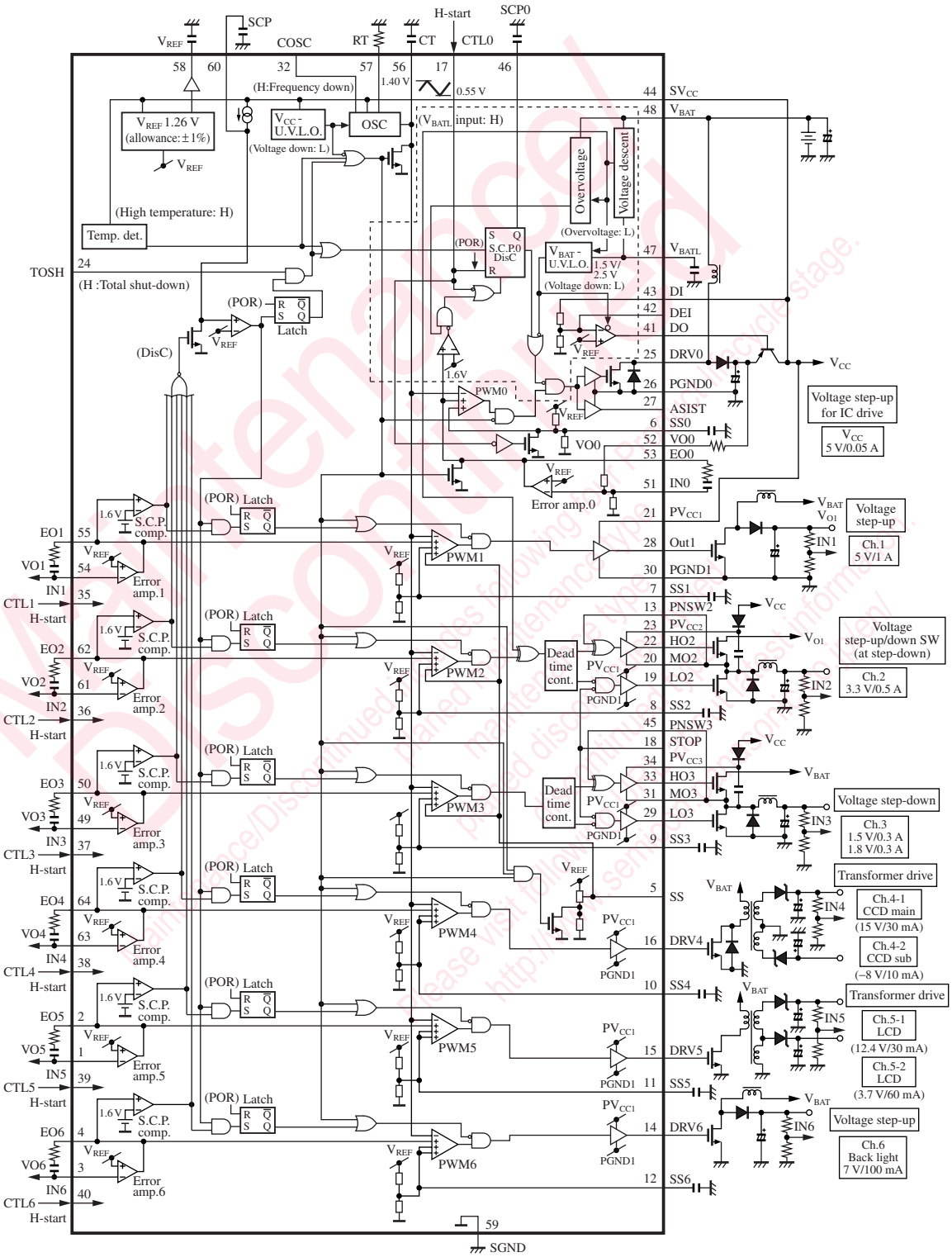
■ Application Circuit Example

• Application circuit example 1 (4 pcs of unit-3 battery: 3.6 V to 7.2 V)



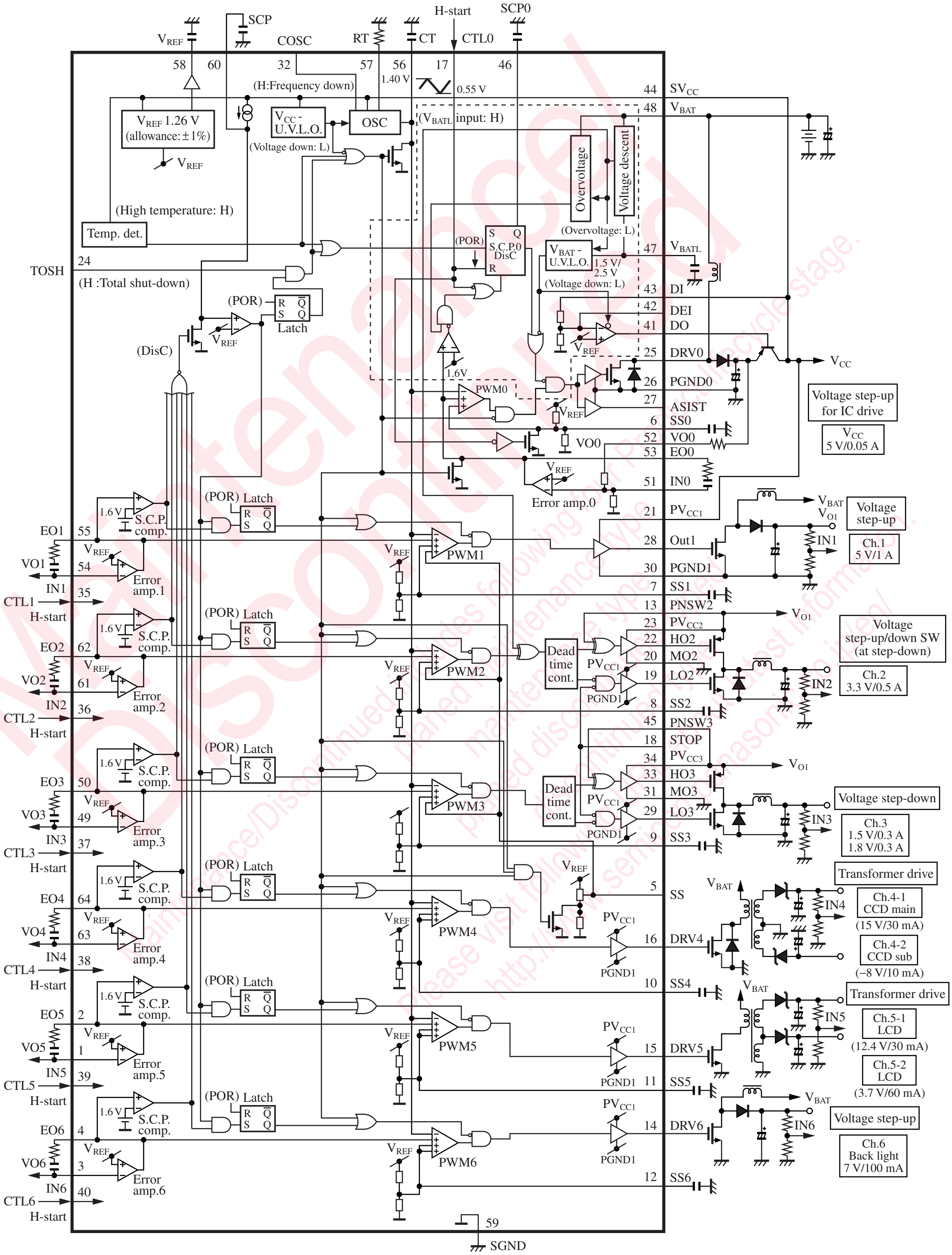
■ Application Circuit Example (continued)

- Application circuit example 2 (Li secondary battery –1: 2.8 V to 4.2 V)
  - Ch.2, ch.3 output FET (High-side): Using N-ch. FET



■ Application Circuit Example (continued)

- Application circuit example 3 (Li secondary battery –2: 2.8 V to 4.2 V)
  - Ch.2, ch.3 output FET (High-side): Using P-ch. FET

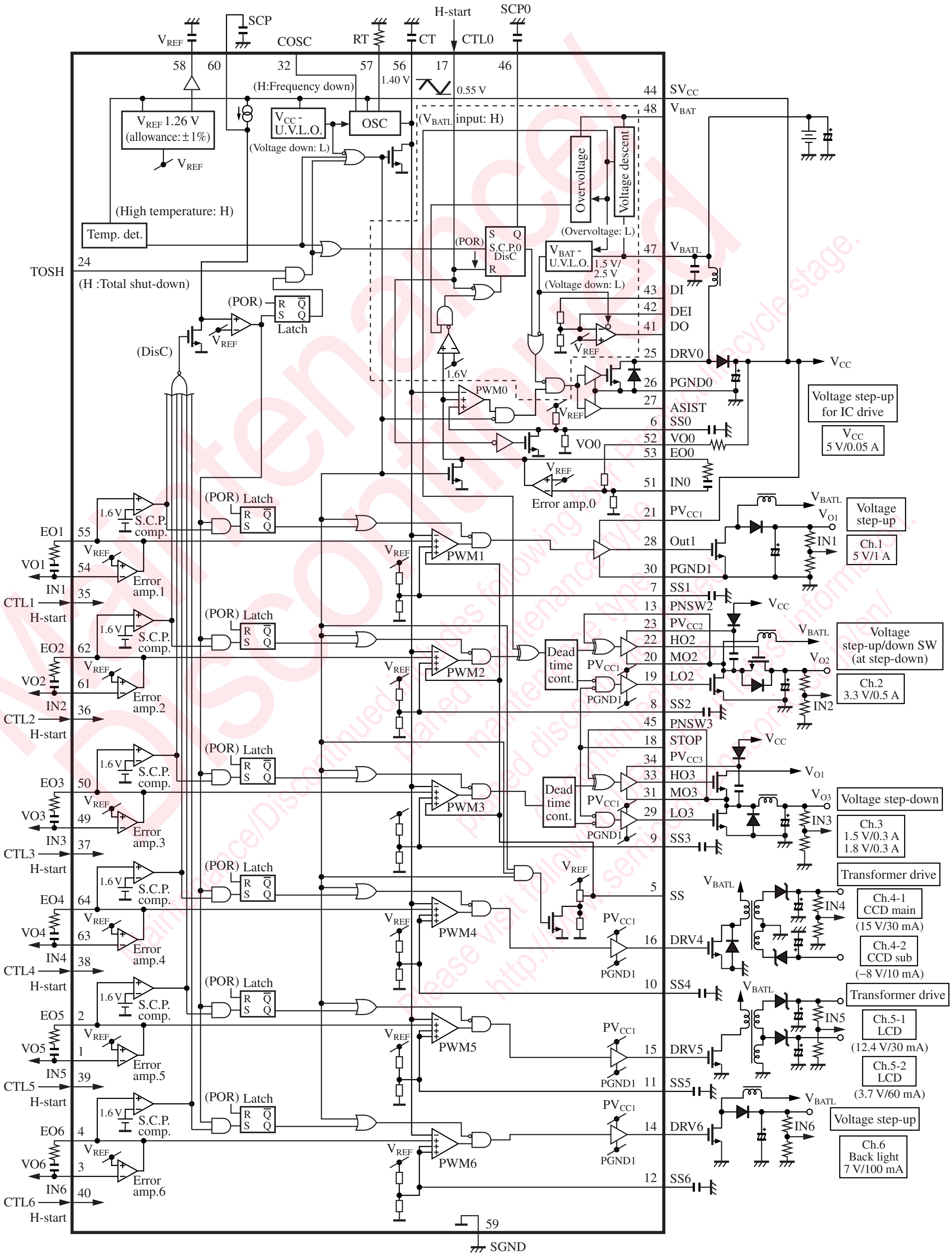


VREF
SCP
COSC
RT
CT
H-start
CTL0
SCP0
58
60
32
57
56
17
46
(H:Frequency down)
1.40 V
0.55 V
44 SVCC
48 VBAT
VREF 1.26 V (allowance: ±1%)
VCC - U.V.L.O.
(Voltage down: L)
OSC
(VBATL input: H)
Overvoltage
Voltage descent
(High temperature: H)
Temp. det.
(Overvoltage: L)
(POR)
S.C.P.0 DisC
VBAT - U.V.L.O.
1.5 V/ 2.5 V
(Voltage down: L)
47 VBATL
TOSH
24
(H :Total shut-down)
43 DI
42 DEI
41 DO
(POR)
Latch
(DisC)
1.6V
25 DRV0
VCC
PWM0
26 PGND0
27 ASIST
6 SS0
52 VO0
53 EO0
51 IN0
Voltage step-up for IC drive
VCC 5 V/0.05 A
Error amp.0
21 PVCC1
VBAT
VO1
Voltage step-up
EO1 55
VO1 54
IN1 35
CTL1
H-start
S.C.P. comp.
Error amp.1
PWM1
28 Out1
IN1
Ch.1 5 V/1 A
30 PGND1
7 SS1
13 PNSW2
23 PVCC2
VO1
EO2 62
VO2 61
IN2 36
CTL2
H-start
Error amp.2
PWM2
Dead time cont.
22 HO2
20 MO2
19 LO2
PGND1
Voltage step-up/down SW (at step-down)
IN2
Ch.2 3.3 V/0.5 A
8 SS2
45 PNSW3
18 STOP
34 PVCC3
EO3 50
VO3 49
IN3 37
CTL3
H-start
Error amp.3
PWM3
33 HO3
31 MO3
29 LO3
Voltage step-down
IN3
Ch.3 1.5 V/0.3 A 1.8 V/0.3 A
9 SS3
EO4 64
VO4 63
IN4 38
CTL4
H-start
Error amp.4
PWM4
5 SS
Transformer drive
IN4
Ch.4-1 CCD main (15 V/30 mA)
16 DRV4
Ch.4-2 CCD sub (–8 V/10 mA)
10 SS4
EO5 2
VO5 1
IN5 39
CTL5
H-start
Error amp.5
PWM5
Transformer drive
IN5
Ch.5-1 LCD (12.4 V/30 mA)
15 DRV5
Ch.5-2 LCD (3.7 V/60 mA)
11 SS5
EO6 4
VO6 3
IN6 40
CTL6
H-start
Error amp.6
PWM6
14 DRV6
Voltage step-up
IN6
Ch.6 Back light 7 V/100 mA
12 SS6
59
SGND

■ Application Circuit Example (continued)

• Application circuit example 4 (2 pcs of unit-3 battery –1 : 1.5 V to 3.6 V)

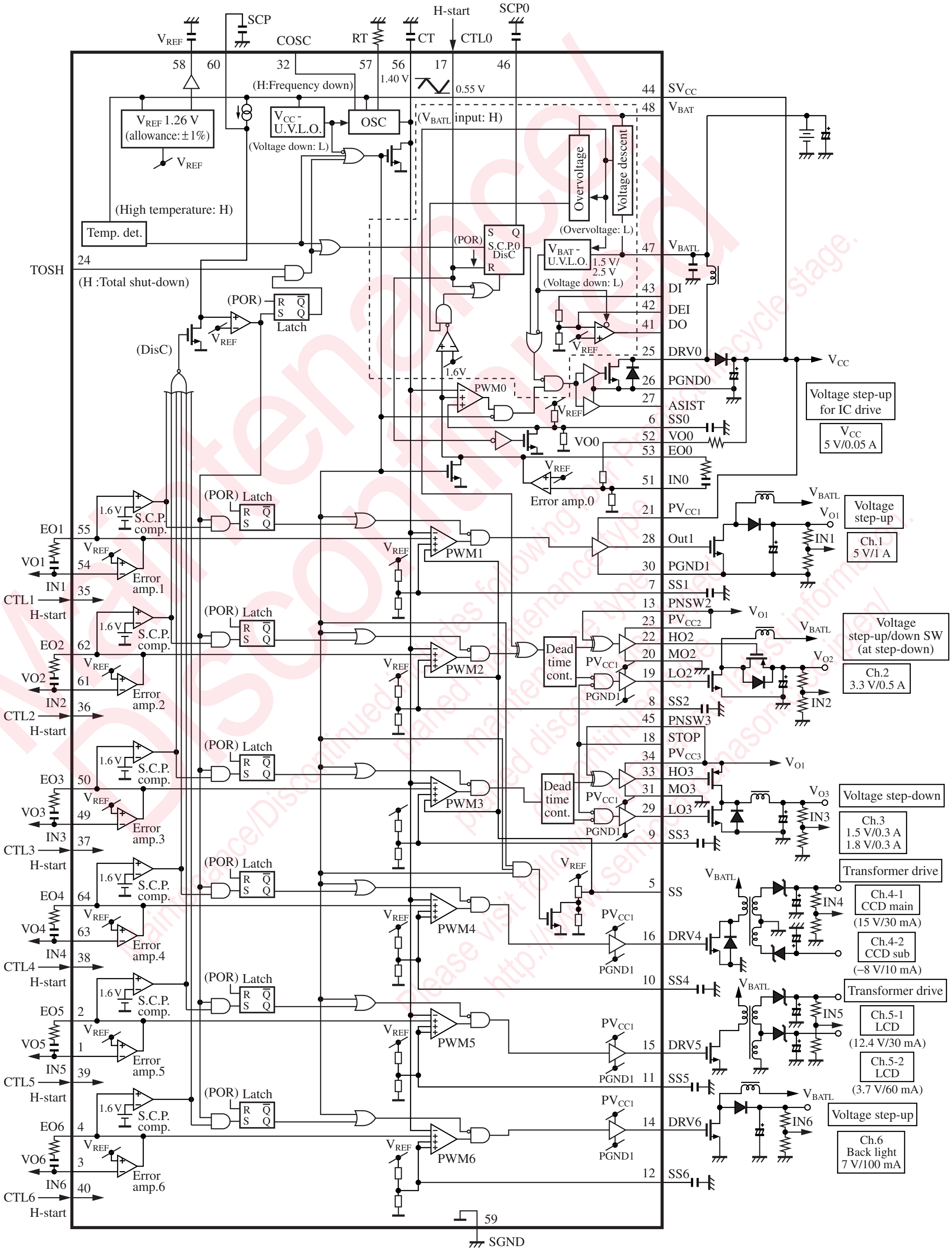
• Ch.2, ch.3 output FET (High-side): Using N-ch. FET



VREF
SCP
COSC
RT
CT
H-start
CTL0
SCP0
(H:Frequency down)
1.40 V
0.55 V
VREF 1.26 V (allowance: ±1%)
VCC - U.V.L.O.
(Voltage down: L)
OSC
(VBATL input: H)
Overvoltage
Voltage descent
(High temperature: H)
Temp. det.
TOSH
(H :Total shut-down)
(POR)
S.C.P.0 DisC
(Overvoltage: L)
VBAT - U.V.L.O.
1.5 V/ 2.5 V
(Voltage down: L)
Latch
(DisC)
1.6V
PWM0
VO0
Error amp.0
SVCC
VBAT
VBATL
DI
DEI
DO
DRV0
PGND0
ASIST
SS0
VO0
EO0
IN0
VCC
Voltage step-up for IC drive
VCC 5 V/0.05 A
(POR) Latch
S.C.P. comp.
Error amp.1
Error amp.2
Error amp.3
Error amp.4
Error amp.5
Error amp.6
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
Dead time cont.
PVCC1
PGND1
EO1
VO1
IN1
CTL1
EO2
VO2
IN2
CTL2
EO3
VO3
IN3
CTL3
EO4
VO4
IN4
CTL4
EO5
VO5
IN5
CTL5
EO6
VO6
IN6
CTL6
H-start
PVCC1
Out1
PGND1
SS1
PNSW2
PVCC2
HO2
MO2
LO2
SS2
PNSW3
STOP
PVCC3
HO3
MO3
LO3
SS3
SS
DRV4
SS4
DRV5
SS5
DRV6
SS6
SGND
Voltage step-up
Ch.1 5 V/1 A
Voltage step-up/down SW (at step-down)
Ch.2 3.3 V/0.5 A
Voltage step-down
Ch.3 1.5 V/0.3 A 1.8 V/0.3 A
Transformer drive
Ch.4-1 CCD main
(15 V/30 mA)
Ch.4-2 CCD sub
(–8 V/10 mA)
Ch.5-1 LCD
(12.4 V/30 mA)
Ch.5-2 LCD
(3.7 V/60 mA)
Ch.6 Back light 7 V/100 mA

■ Application Circuit Example (continued)

- Application circuit example 5 (2 pcs of unit-3 battery –2 : 1.5 V to 3.6 V)
  - Ch.2, ch.3 output FET (High-side): Using P-ch. FET

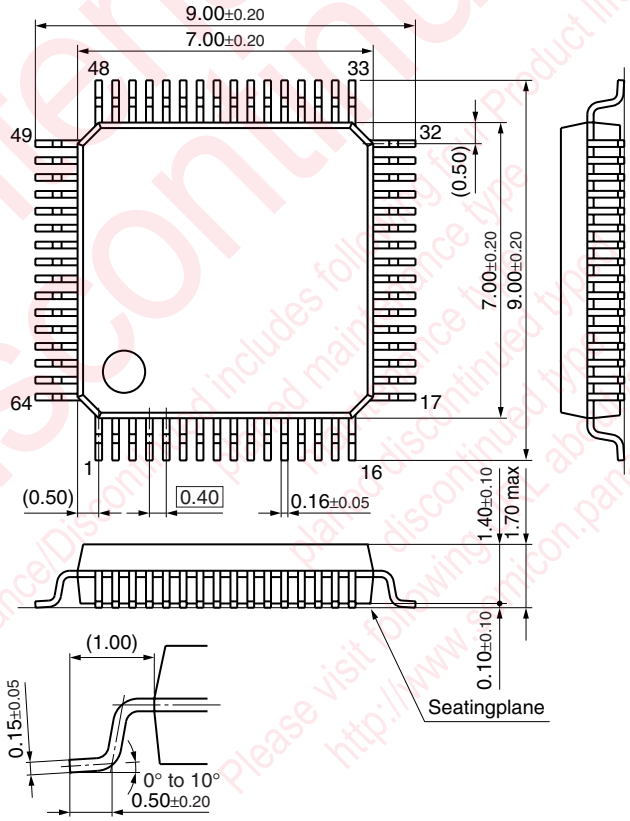

H-start
SCP0
SCP
VREF
COSC
RT
CT
CTL0
58
60
32
57
56
17
46
1.40 V
0.55 V
(H:Frequency down)
VREF 1.26 V
(allowance: ±1%)
VCC - U.V.L.O.
(Voltage down: L)
OSC
(VBATL input: H)
Overvoltage
Voltage descent
(High temperature: H)
Temp. det.
TOSH
24
(H :Total shut-down)
(POR)
Latch
(DisC)
S.C.P.0
DisC
(Overvoltage: L)
VBAT - U.V.L.O.
1.5 V/ 2.5 V
(Voltage down: L)
1.6V
PWM0
Error amp.0
VO0
S.C.P. comp.
Error amp.1
Error amp.2
Error amp.3
Error amp.4
Error amp.5
Error amp.6
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
Dead time cont.
PVCC1
PGND1
EO1
VO1
IN1
CTL1
EO2
VO2
IN2
CTL2
EO3
VO3
IN3
CTL3
EO4
VO4
IN4
CTL4
EO5
VO5
IN5
CTL5
EO6
VO6
IN6
CTL6
44 SVCC
48 VBAT
47 VBATL
43 DI
42 DEI
41 DO
25 DRV0
26 PGND0
27 ASIST
6 SS0
52 VO0
53 EO0
51 IN0
21 PVCC1
28 Out1
30 PGND1
7 SS1
13 PNSW2
23 PVCC2
22 HO2
20 MO2
19 LO2
8 SS2
45 PNSW3
18 STOP
34 PVCC3
33 HO3
31 MO3
29 LO3
9 SS3
5 SS
16 DRV4
10 SS4
15 DRV5
11 SS5
14 DRV6
12 SS6
59
SGND
VCC
Voltage step-up for IC drive
VCC 5 V/0.05 A
Voltage step-up
Ch.1 5 V/1 A
Voltage step-up/down SW (at step-down)
Ch.2 3.3 V/0.5 A
Voltage step-down
Ch.3 1.5 V/0.3 A 1.8 V/0.3 A
Transformer drive
Ch.4-1 CCD main
(15 V/30 mA)
Ch.4-2 CCD sub
(–8 V/10 mA)
Ch.5-1 LCD
(12.4 V/30 mA)
Ch.5-2 LCD
(3.7 V/60 mA)
Ch.6 Back light 7 V/100 mA

■ Recommended Operating Conditions

Parameter	Symbol	Recommended value	Unit
Timing resister	R_T	33	kΩ
Timing capacitor	C_T	180	pF
Oscillator frequency	f_{OUT}	550	kHz
Constant setting capacitance at ch.0 short-circuit and V_{BATL} over-voltage protection operating	C_{SCP0}	0.15	µF
Constant setting capacitance at ch.1 to ch.6 short-circuit and thermal protection operating	C_{SCP}	0.1	µF
Constant setting capacitance at soft start	C_{SS}	20	nF

■ New Package Dimensions (Unit: mm)

• LQFP064-P-0707B (Lead-free package)



Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products, and no license is granted under any intellectual property right or other right owned by our company or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
 Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

littlediode
COMPONENTS FOR ALL

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.