

AN2800K

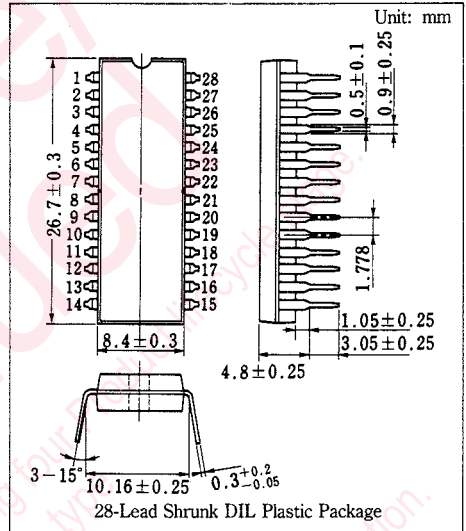
VHD Video Disc Player Sound Signal Demodulator Circuit

Outline

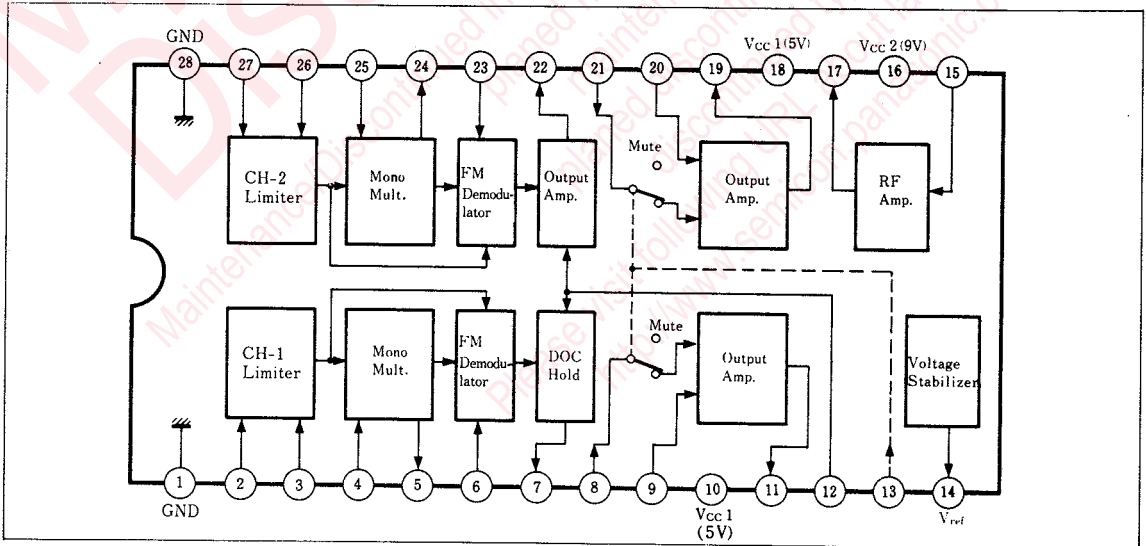
The AN2800K is an integrated circuit designed for sound signal demodulation of VHD-system video disk player.

Features

- The functions consist of :
 - RF Amplifier
 - FM limiters, demodulators (dual channel)
 - Dropout compensators (dual channel)
 - Muting circuits (dual channel)



Block Diagram



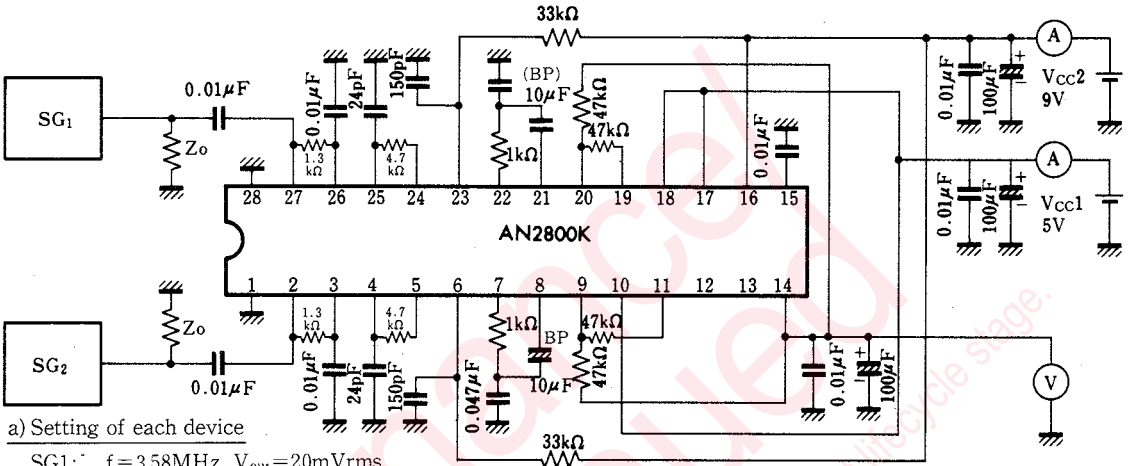
■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC1}	6.0	V
	V _{CC2}	10.8	V
Supply current	I _{CC1}	20	mA
	I _{CC2}	3.3	mA
Power dissipation	P _D	160	mW
Operating ambient temperature	T _{opr}	-20~+70	°C
Storage temperature	T _{stg}	-55~+150	°C

■ Electrical Characteristics (V_{CC1} = 5V, V_{CC2} = 9V, Ta = 25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current 1	I _{CC1}	1	V _{CC1} =5V, V _{CC2} =9V	9	13	17	mA
Circuit current 2	I _{CC2}	1	V _{CC1} =5V, V _{CC2} =9V	1.48	2.10	2.75	mA
Terminal voltage	V ₁₄₋₁	1	V _{CC1} =5V, V _{CC2} =9V	2.30	2.50	2.70	V
Squelch ON/OFF(CH-1) output offset voltage	V _(offset)	2	V _{CC1} =5V, V _{CC2} =9V, Pin ⑬ GND ON/OFF	-100	0	+100	mV
Squelch ON/OFF(CH-2) output offset voltage	V _(offset)	2	V _{CC1} =5V, V _{CC2} =9V, Pin ⑬ GND ON/OFF	-100	0	+100	mV
RF amp. voltage gain	G _v	3	f _c =3.58MHz, V _i =20mVrms	21.8	25.8	28.9	dB
FM demodulation min. input voltage(CH-1)	V _{i(min.)}	4	f _c =3.73MHz, THD≤5% f _m =1kHz, Δf=±37.5kHz		1.0	2.5	mVrms
FM demodulation min. input voltage(CH-2)	V _{i(min.)}	4	f _c =3.73MHz, THD≤5% f _m =1kHz, Δf=±37.5kHz		1.0	2.5	mVrms
FM demodulation output harmonic distortion(CH-1)	THD	5	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		0.07	0.30	%
FM demodulation output harmonic distortion(CH-2)	THD	5	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		0.07	0.30	%
FM demodulation output signal voltage(CH-1)	V _o	6	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz	150	200	250	mVrms
FM demodulation output signal voltage(CH-2)	V _o	6	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz	150	200	250	mVrms
Cross talk output signal voltage(CH-1)	CT	7	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		150	300	μVrms
Cross talk output signal voltage(CH-2)	CT	7	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		150	300	μVrms
Squelch ON output signal voltage(CH-1)	SV _o	8	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		50	140	μVrms
Squelch ON output signal voltage(CH-2)	SV _o	8	f _c =3.73MHz, V _i =35mVrms f _m =1kHz, Δf=±37.5kHz		50	140	μVrms
Dropout pulse extension(CH-1)	t _d	9	f _c =3.58MHz, V _i =20mVrms f _{doc} =20kHz rectangular wave	4	8	16	μs
Dropout pulse extension(CH-2)	t _d	9	f _c =3.58MHz, V _i =20mVrms f _{doc} =20kHz Rectangular wave	4	8	16	μs

Test Circuit 1 (I_{CC1} , I_{CC2} , V_{14-1})



a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$

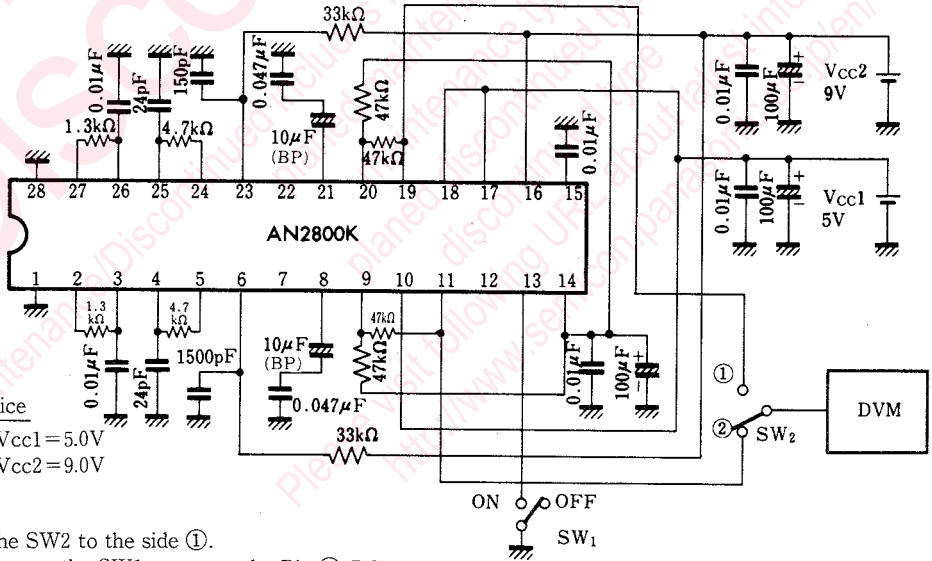
Adjust Z_o to the output impedance ($50\Omega/75\Omega$) of each SG.

DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

I_{CC1} : Measure a value of the ammeter 1.
 I_{CC2} : Measure a value of the ammeter 2.
 V_{REF} : Measure a value of the voltmeter 1.

Test Circuit 2 (V_{offset})



a) Setting of each device

DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

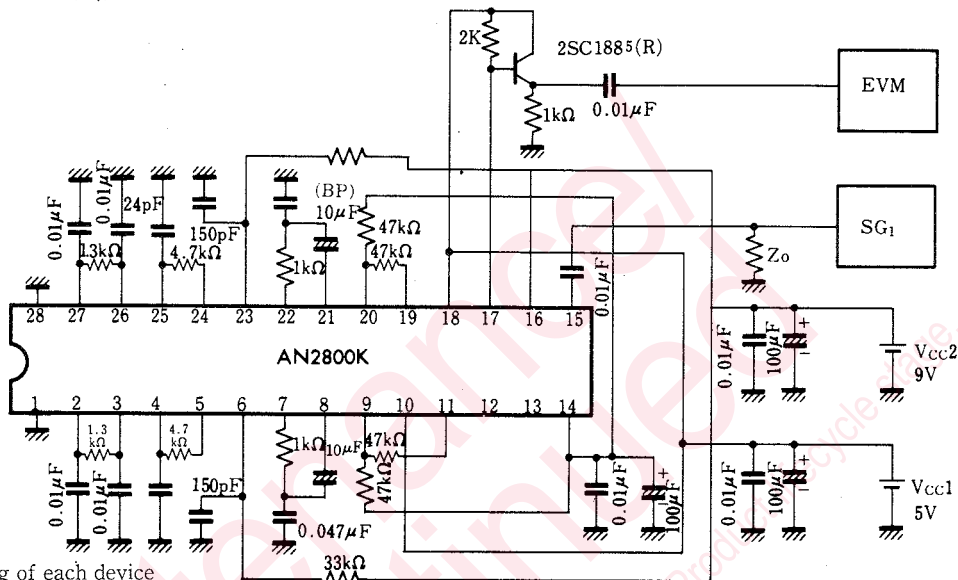
Voffset: The shift the SW2 to the side ①.

When turning on the SW1, measure the Pin ① DC voltage.
 Next, measure the DC voltage when the SW1 is turned off.
 Then, calculate a differential voltage value between both DC voltages.

Voffset: The shift the SW2 to the side ②.

When turning on the SW1, measure the Pin ② DC voltage.
 Next, measure the DC voltage when turning off the SW1.
 Then, calculate a differential voltage value between both DC voltages.

Test Circuit 3 (G_v)



a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 Adjust Z_o to the output impedance ($50\Omega / 75\Omega$)
 of SG.

Electronic voltmeter (EVM) EVM: Set to a 1 Vrms full scale range.

DC power supply: $V_{cc1} = 5.0\text{V}$

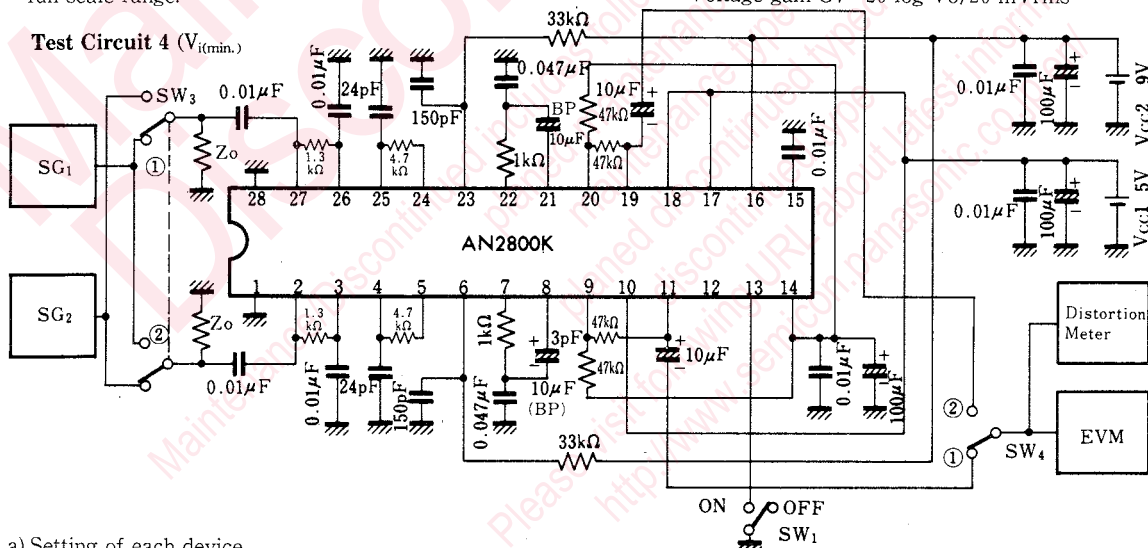
DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

G_v: Measure the value (V_o) of the electronic voltmeter

$$\text{Voltage gain } G_v = 20 \log V_o / 20 \text{ mVrms}$$

Test Circuit 4 ($V_{i(\text{min})}$)



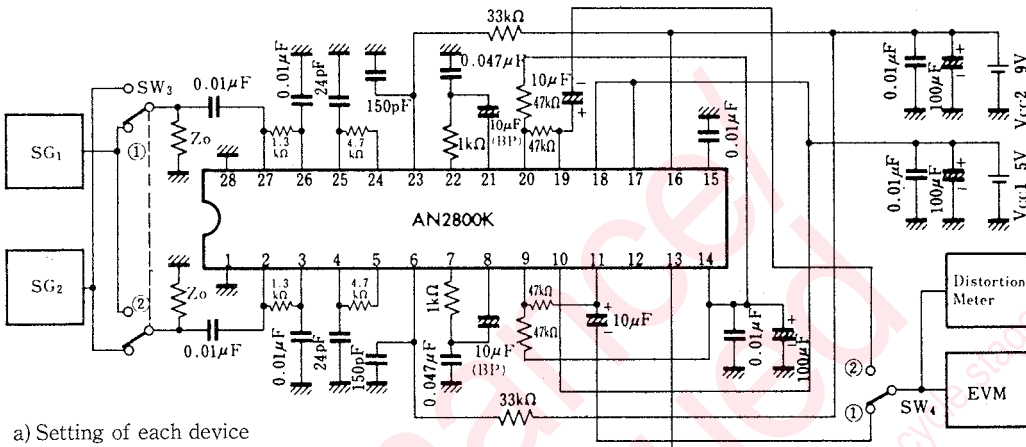
a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 2.5\text{mVrms}$, FM modulation $f_m = 1\text{kHz}$, $f_{dev} = \pm 37.5\text{KHz}$
 Adjust Z_o to the output impedance ($50\Omega / 75\Omega$) of each SG.
 Harmonic distortion gauge: 10% range (LPF 100 kHz ON, HPF 400 Hz ON)
 DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

$V_{i(\text{min})}$: Turn off the SW1, and shift the SW3 and SW4 to the side ①. Obtain a value indicated by the harmonic distortion gauge. ($\leq 5\%$)
 $V_{i(\text{min})}$: Turn off the SW1, and shift the SW3 and SW4 to the side ②. Obtain a value indicated by the harmonic distortion gauge. ($\leq 5\%$)
 Note) Input an FM signal voltage of a max. specified value and determine with a harmonic distortion factor of a demodulated output waveform.

Test Circuit 5 (THD)



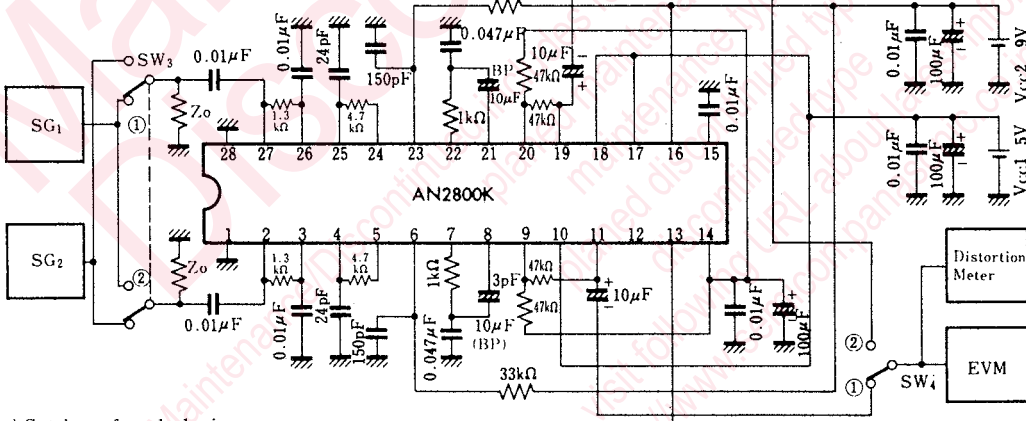
a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$, FM modulation $f_m = 1\text{kHz}$, $f_{dev} = \pm 37.5\text{kHz}$
 Adjust Z_o to the output impedance of each SG.
 Harmonic distortion gauge: 1.0% range (LPF 100 kHz ON, HPF 400 Hz ON)
 DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

THD: Turn off the SW1, and shift the SW3 and SW4 to the side ①, and obtain a value indicated by the harmonic distortion gauge.
 THD: Turn off the SW1, and shift the SW3 and SW4 to the side ②, and obtain a value indicated by the harmonic distortion gauge.

Test Circuit 6 (V_o)



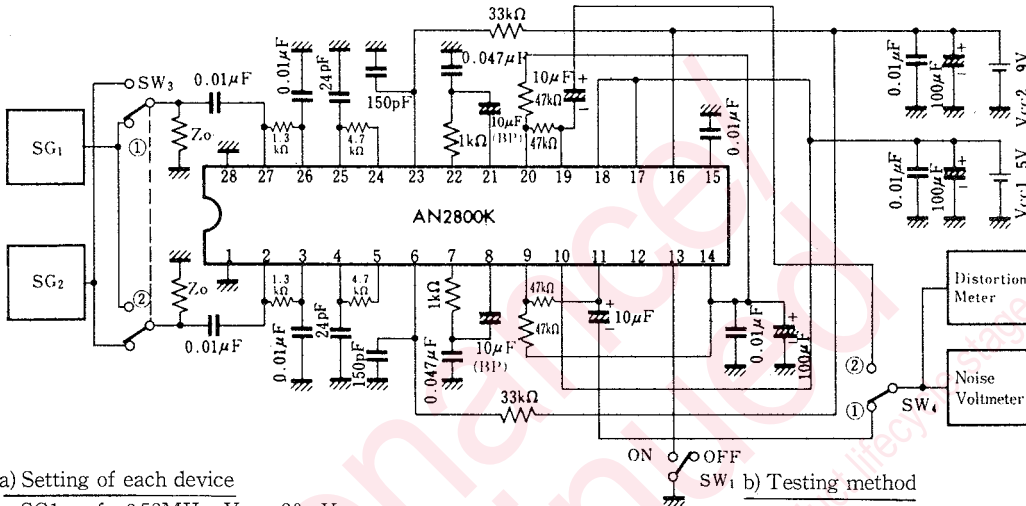
a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$, FM modulation $f_m = 1\text{kHz}$, $f_{dev} = \pm 37.5\text{kHz}$
 Adjust Z_o to the output impedance ($50\Omega / 75\Omega$) of each SG.
 Electronic voltmeter: 0.3 Vrms range
 DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

V_o : FM demodulated output signal voltage (CH-1)
 Turn off the SW1, and shift the SW3 and SW4 to the side ①, and obtain a value indicated by the electronic voltmeter.
 V_o : FM demodulated output signal voltage (CH-2).
 Turn off the SW1, and shift the SW3 and SW4 to the side ②, and obtain a value indicated by the electronic voltmeter.

Test Circuit 7 (CT)



a) Setting of each device

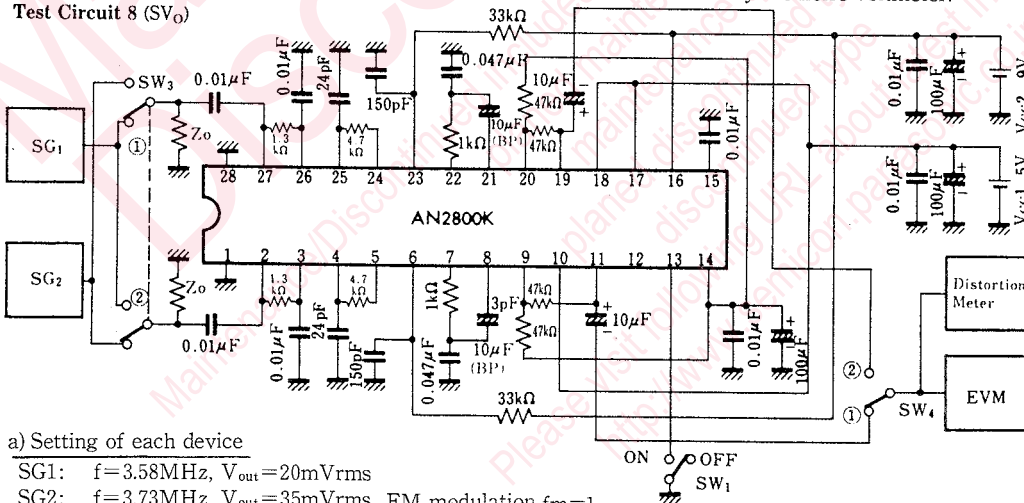
SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$, FM modulation $f_m = 1\text{kHz}$, $f_{dey} = \pm 37.5\text{kHz}$
 Adjust Z_o to the output impedance ($50\Omega / 75\Omega$) of each SG.

Noise voltmeter: $300\mu\text{Vrms}$ range, IHF-A filter
 DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

CT: Cross talk output signal voltage (CH-1 → CH-2).
 Turn off the SW1, and shift the SW3 to the side ① and the SW4 to the side ②, and obtain a value indicated by the noise voltmeter.
 CT: Cross talk output signal voltage (CH-2 → CH-1).
 Turn off the SW1, and shift the SW3 to the side ② and SW4 to the side ①, and obtain a value indicated by the noise voltmeter.

Test Circuit 8 (SV_o)



a) Setting of each device

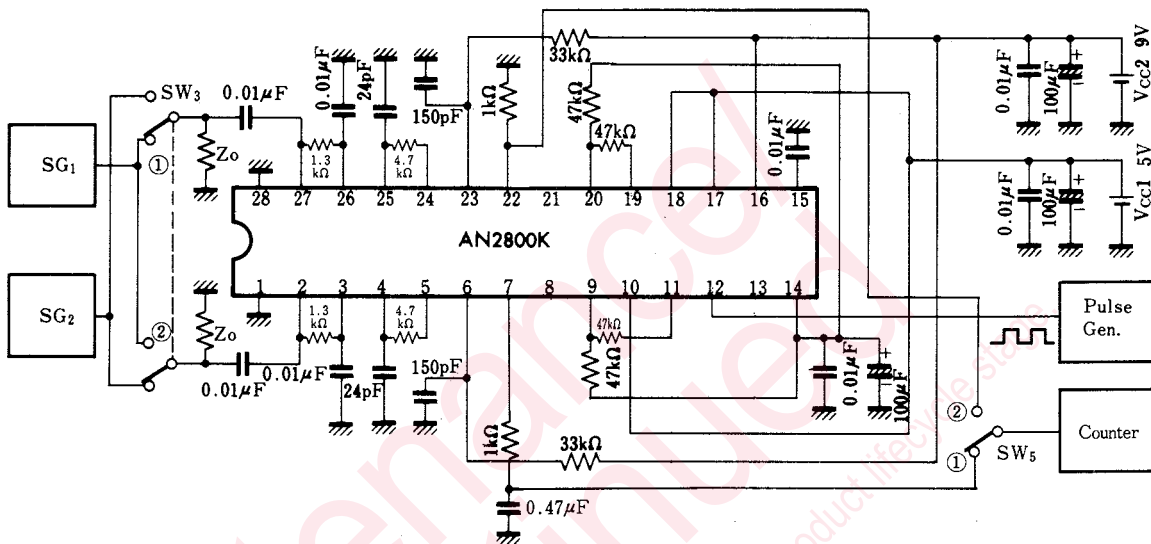
SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$
 SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$, FM modulation $f_m = 1\text{kHz}$, $f_{dey} = \pm 37.5\text{kHz}$
 Adjust Z_o to the output impedance ($50\Omega / 75\Omega$) of each SG.

Noise voltmeter: $300\mu\text{Vrms}$ range, IHF-A filter ON
 DC power supply: $V_{cc1} = 5.0\text{V}$
 DC power supply: $V_{cc2} = 9.0\text{V}$

b) Testing method

SV_o: Output signal voltage (CH-1) at squelch ON time. Turn on the SW1, and shift the SW3 and SW4 to the side ①. Obtain a value indicated by the noise voltmeter.
 SV_o: Output signal voltage (CH-2) at squelch ON time. Turn on the SW1, and shift the SW3 and SW4 to the side ②. Obtain a value indicated by the noise voltmeter.

Test Circuit 9 (td)



a) Setting of each device

SG1: $f = 3.58\text{MHz}$, $V_{out} = 20\text{mVrms}$

SG2: $f = 3.73\text{MHz}$, $V_{out} = 35\text{mVrms}$. FM modulation $f_m = 1\text{kHz}$, $f_{dey} = \pm 37.5\text{kHz}$

Adjust Z_o to the output impedance ($50\Omega/75\Omega$) of each SG.

Pulse generator: $f = 20\text{kHz}$ rectangular wave

(duty ratio 1:1)

$V_H = 3.75\text{V}$, $V_L = 2.75\text{V}$, DC offset voltage

Universal counter: Negative pulse width measurement mode

DC power supply : $V_{cc1} = 5.0\text{V}$

DC power supply : $V_{cc2} = 9.0\text{V}$

b) Testing method

td: Shift the SW3 to the side ② and SW5 to the side

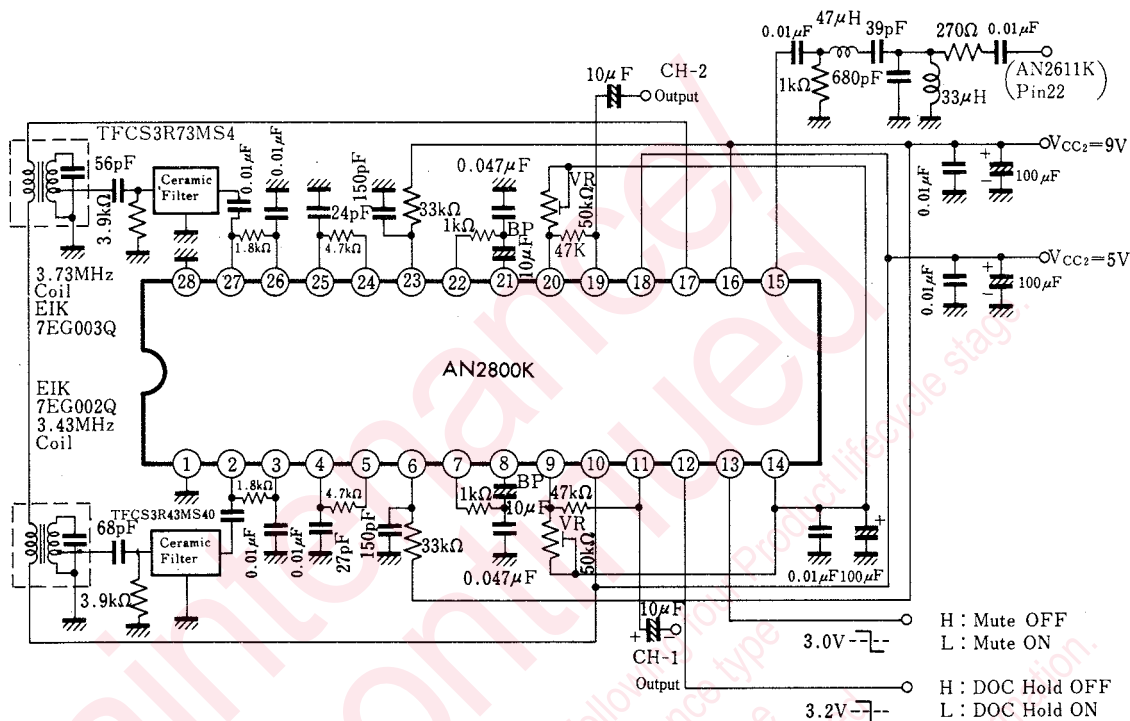
①, and measure an output pulse Low section with the universal counter. (T_{VLOW})

td: Shift the SW3 to the side ① and SW5 to the side

②, and measure an output pulse Low section with the universal counter. (T_{VLOW})

Obtain a pulse extension td of $T_{VLOW} - 25\eta\text{sec}$.

■ Application Circuit



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	GND	15	RF Amp. Input
2	CH-1 Limiter Input	16	V _{CC2} (typ 9V)
3	CH-1 Limiter Bias	17	RF Amp. Output
4	CH-1 Mono Multi (CR)	18	V _{CC1} (typ 5V)
5	CH-1 Mono Multi Bias	19	CH-2 Output Amp. Output
6	CH-1 FM Demodulator Output	20	CH-2 Output Amp. Input 2
7	CH-1 DOC Hold	21	CH-2 Output Amp. Input 1
8	CH-1 Output Amp. Input 1	22	CH-2 DOC Hold
9	CH-1 Output Amp. Input 2	23	CH-2 FM Demodulator Output
10	V _{CC1} (typ 5V)	24	CH-2 Mono Multi Bias
11	CH-1 Output Amp. Output	25	CH-2 Mono Multi (CR)
12	DOC Control Signal Input	26	CH-2 Limiter Bias
13	Mute Control Signal Input	27	CH-2 Limiter Input
14	Voltage Stabilizer Output	28	GND

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