AN2450S

CCD Video Camera Signal Processing Circuit

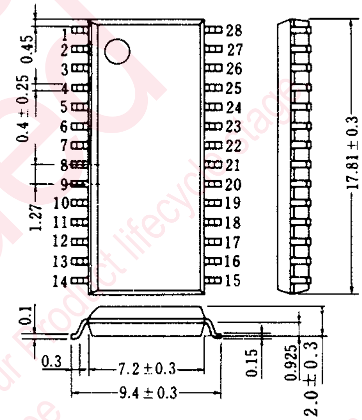
■ Outline

The AN2450S is an integrated circuit for CCD video camera signal processing. After putting a synchronized color difference signal through a color difference matrix, it outputs the signal as a chroma signal.

■ Features

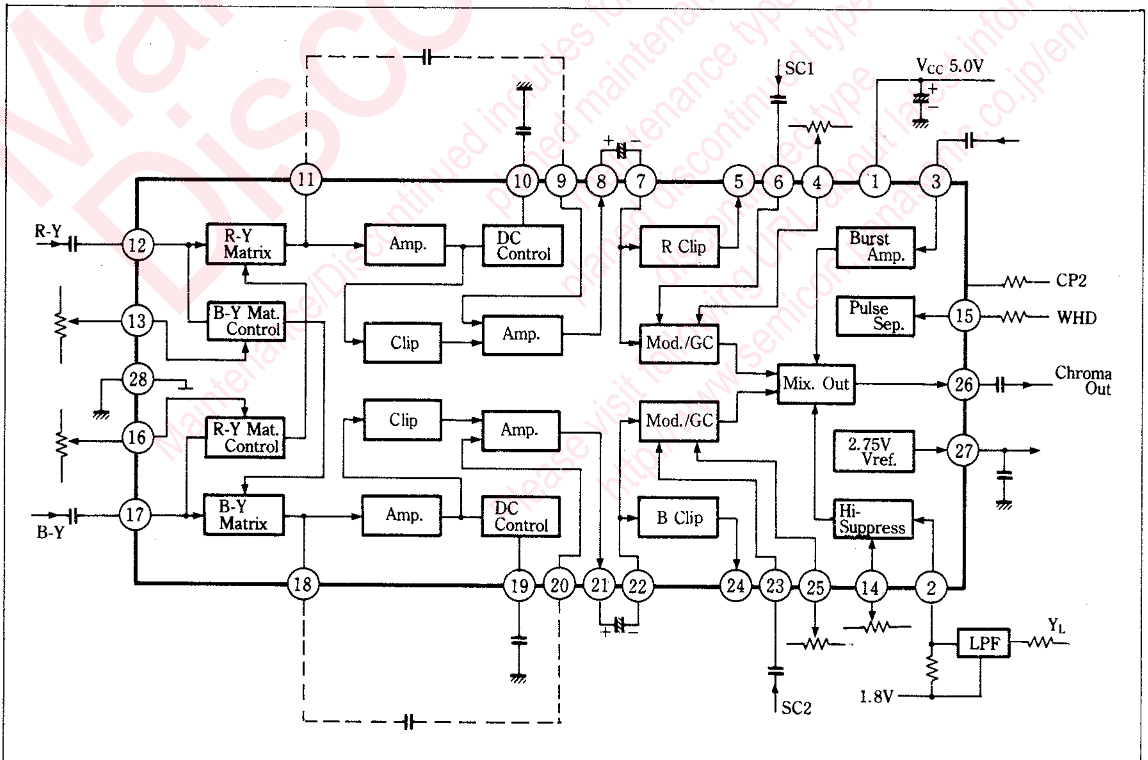
- Low operating voltage and current : $V_{CC}=5V$, $I_{CC}=12mA$ (typ.)
- Built-in matrix, 3.58MHz modulation and burst signal mix.

Unit : mm



28-Lead PANAFLAT Package (SO-28D)

■ Block Diagram



■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	V_{CC} (typ. 5.0V)	15	Pulse Input
2	Hi-Lumi Suppress	16	R-Y Matrix Control
3	Burst Input	17	B-Y Input (AN2350S)
4	R-Y Gain Control	18	B-Y Matrix Output
5	R-Y Clip Output	19	DC Control
6	CW1 Input	20	B-Y Input (Amp.)
7	R-Y Clamp Input	21	B-Y Output
8	R-Y Output	22	B-Y Clamp Input
9	R-Y Input (Amp.)	23	CW2 Input
10	DC Control	24	B-Y Clip Output
11	R-Y Matrix Output	25	B-Y Gain Control
12	R-Y Input (AN2350S)	26	Chroma Burst Output
13	B-Y Matrix Control	27	Vref (typ. 2.75V) Output
14	Hi-Lumi. Sup. Control	28	GND

■ Absolute Maximum Ratings (Ta=25℃)

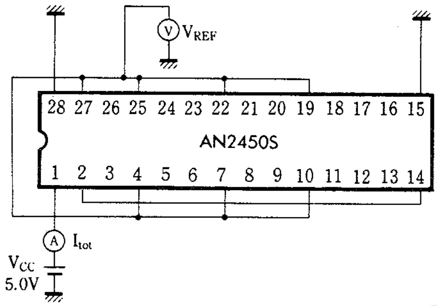
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	6.0	V
Supply current	I_{CC}	20	mA
Power dissipation	P_D	130	mW
Operating ambient temperature	T_{opr}	−20~+75	℃
Storage temperature	T_{stg}	−55~+125	℃

■ Electrical Characteristics (Ta=25℃)

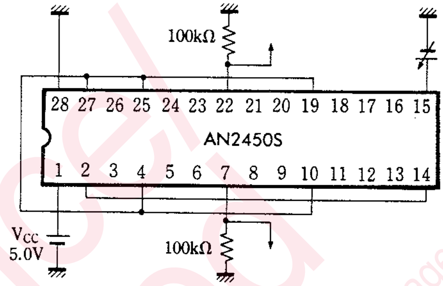
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Total circuit current	I_{tot}	1	I_{CC}=5.0V	6	12	18	mA
2.75 V power supply	V_{REF}	1	V_{CC}=5.0V	2.6	2.75	2.9	V
CP2 pulse separation level 1	$V_{t(CP1)}$	2	V_{CC}=5.0V	1.6	2.05	2.5	V
CP2 pulse separation level 2	$V_{t(CP2)}$	2	V_{CC}=5.0V	1.6	2.05	2.5	V
WHD pulse separation level 1	$V_{t(WHD1)}$	3	V_{CC}=5.0V	0.6	1.05	1.5	V
WHD pulse separation level 2	$V_{t(WHD2)}$	3	V_{CC}=5.0V	0.6	1.05	1.5	V
R-Y color difference gain 1	G_{V1}	4	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	1400	1650	1900	mV_{P-P}
R-Y color difference gain 2	G_{V2}	4	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	600	850	110	mV_{P-P}
R-Y matrix gain 1	G_{V3}	4	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	140	230	320	mV_{P-P}
R-Y matrix gain 2	G_{V4}	4	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}		20	50	mV_{P-P}
B-Y color difference gain 1	G_{V5}	5	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	1400	1650	1900	mV_{P-P}
B-Y color difference gain 2	G_{V6}	5	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	600	850	1100	mV_{P-P}
B-Y matrix gain 1	G_{V7}	5	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}	120	180	240	mV_{P-P}
B-Y matrix gain 2	G_{V8}	5	V_{CC}=5.0V, f_i=650kHz, V_i=200mV_{P-P}		20	50	mV_{P-P}
R-Y SC gain 1	G_{V9}	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	320	400	480	mV_{P-P}
R-Y SC gain 2	G_{V10}	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	630	725	820	mV_{P-P}
B-Y SC gain 1	G_{V11}	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	400	480	560	mV_{P-P}
B-Y SC gain 2	G_{V12}	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	730	855	980	mV_{P-P}
Carrier leak	C_L	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}		10	20	mV_{P-P}
Burst AMP gain	G_{V14}	6	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	40	85	130	mV_{P-P}
High-luminance suppresion 1	G_{V15}	7	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}		10	20	mV_{P-P}
High-luminance suppresion 2	G_{V16}	7	V_{CC}=5.0V, f_i=3.58MHz, V_i=400mV_{P-P}	300	400	500	mV_{P-P}
Y_L signal leak	G_{V17}	7	V_{CC}=5.0V, APL 50%, 400mV_{P-P}		40	85	mV_{P-P}

Note) Operating supply voltage range : $V_{CC(opr)}$=4.8~5.2V

Test Circuit 1 (I_{tot}, V_{REF})

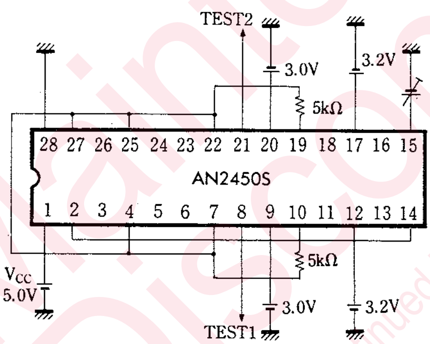


Test Circuit 2 ($V_{t(CP1)}$, $V_{t(CP2)}$)



- $V_{t(CP1)}$: Pin ⑮ DC voltage value when the Pin ⑦ has the Pin ㉗ voltage by changing the Pin ⑮ DC voltage from 1.6V
- $V_{t(CP2)}$: Pin ⑮ DC voltage value when the Pin ㉒ has the Pin ㉗ voltage by changing the Pin ⑮ DC voltage from 1.6V

Test Circuit 3 ($V_{t(WHD1)}$, $V_{t(WHD2)}$)



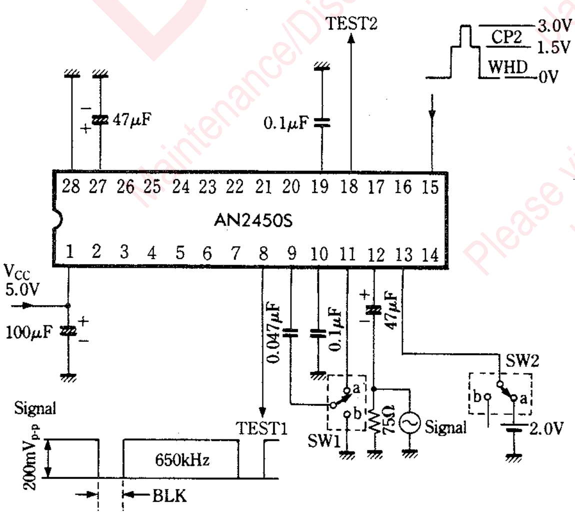
- WHD pulse separation level 1 $V_{t(WHD1)}$ [V]

  Pin ⑮ DC voltage value when the Pin ⑧ changes by changing that voltage from O V

- WHD pulse separation level 2

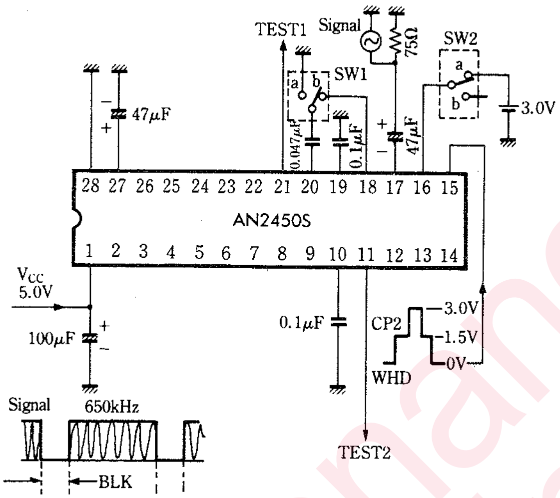
  Pin ⑮ DC voltage value when the Pin ㉑ changes by changing that voltage form O V

Test Circuit 4 (G_{V1}, G_{V2}, G_{V3}, G_{V4})



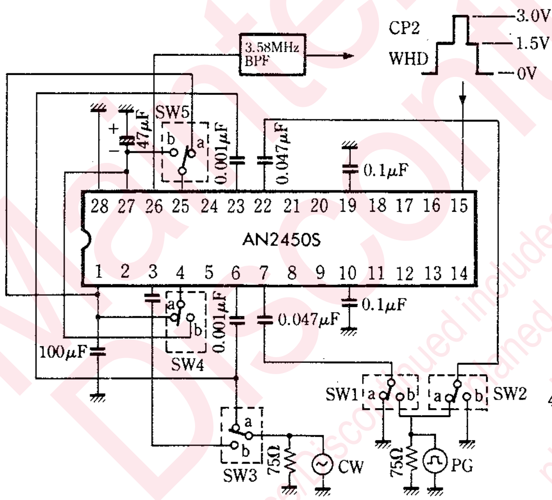
Item	SW1	SW2	Measuring Pin
G_{V1}	a	–	Pin ⑧ (output amplitude measured)
G_{V2}	b	–	Pin ⑧ (output amplitude measured)
G_{V3}	–	a	Pin ⑱ (output amplitude measured)
G_{V4}	–	b	Pin ⑱ (output amplitude measured)

Test Circuit 5 (G_{V5}, G_{V6}, G_{V7}, G_{V8})

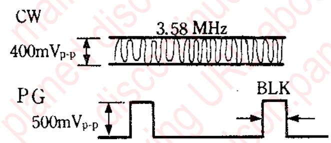


Item	SW1	SW2	Measuring Pin
G_{V5}	a	–	Pin ㉑ (output amplitude measured)
G_{V6}	b	–	Pin ㉑ (output amplitude measured)
G_{V7}	–	a	Pin ⑪ (output amplitude measured)
G_{V8}	–	b	Pin ⑪ (output amplitude measured)

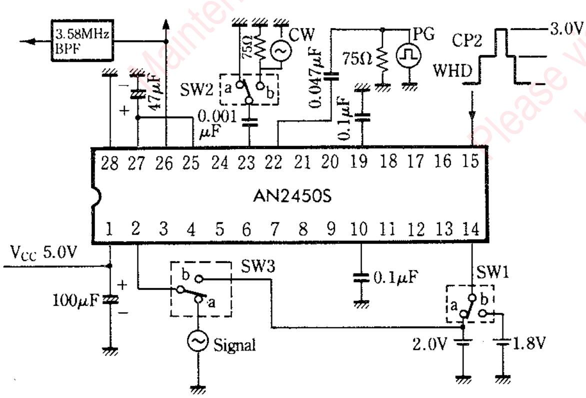
Test Circuit 6 (G_{V9}, G_{V10}, G_{V11}, G_{V12}, C_L, G_{V14})



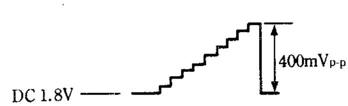
Item	SW 1	SW 2	SW 3	SW 4	SW 5	Measuring Pin
G_{V9}	a	a	a	–	b	Pin ㉖ (BPF output measured)
G_{V10}	a	a	a	–	a	Pin ㉖ (BPF output measured)
G_{V11}	b	b	a	b	–	Pin ㉖ (BPF output measured)
G_{V12}	b	b	a	a	–	Pin ㉖ (BPF output measured)
CL	a	b	a	b	b	Pin ㉖ (BPF output measured)
G_{V14}	a	b	b	b	b	Pin ㉖ (BPF output measured)



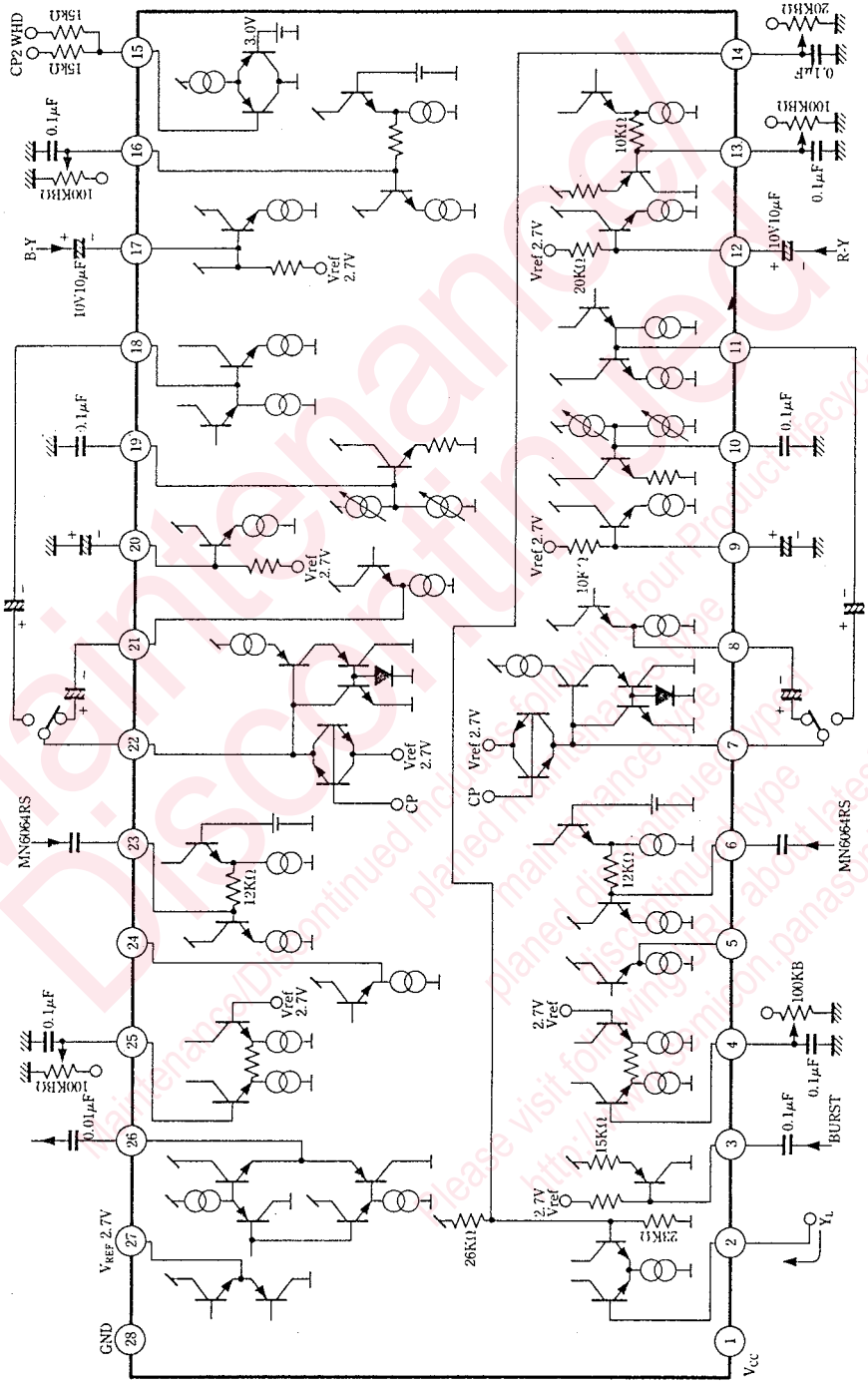
Test Circuit 7 (G_{V15}, G_{V16}, G_{V17})



Item	SW 1	SW 2	SW 3	Measuring Pin
G_{V15}	b	b	b	Pin ㉖ (BPF output measured)
G_{V16}	a	b	b	Pin ㉖ (BPF output measured)
G_{V17}	a	a	a	Pin ㉖ (BPF output measured)



■ Input-Output Schematic Diagram



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