AN1538
APPLICATION NOTE

Reducing Analog-Digital Conversion Error Using ST10F269/ST10F280

By André ROGER

INTRODUCTION

The ST10F269/ST10F280 contains an Analog / Digital Converter with 10-bit resolution, 4.85µs conversion time, a sample & hold circuit on-chip, ESD protected analog inputs and a “Total Unadjusted Error” of ± 2LSB across the whole automotive temperature range.

This application note identifies the causes of ADC error and gives solutions to optimize ADC performance. An appendix reviews the meaning of the terms: resolution, accuracy and intrinsic error.

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1 - SOURCES OF ADC ERROR

Sources of ADC accuracy error are classified into 3 categories:

– Analog input signal error

– Input overload error

– Reference voltage error

Each of these categories is described in the following sections.

1.1 - Analog Input Signal Error

1.1.1 - Source Internal Resistance Matching with ADC Input Parameters

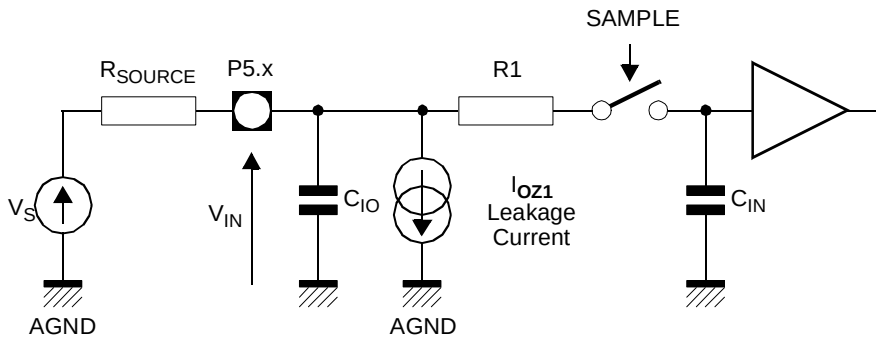
Analog input signal error can be created by poor matching of the source internal resistance with the ADC input parameters, either caused by,

– Voltage drop in the voltage source resistance due to input leakage current,

– Or by poor charging of the ADC internal capacitance (Cin).

Analog input error can also be caused by noise from the analog input signal. This section described each of these causes.

Figure 1 : Source Internal Resistance Errors



I_{OZ1} (Input leakage current Port5): maximum ± 200 nA (test Condition: 0.45V<V_{IN}<VDD)
C_{IO} (Pin capacitance Port5): maximum 10 pF (test Condition: f = 1 MHz, TA = 25°C, guaranteed by design characterization)
C_{IN} (ADC Internal capacitance): maximum 5 pF (guaranteed by design characterization)
R1 (series input resistance): maximum 1.5kΩ (guaranteed by design characterization)

Refer to Figure 1 for a schematic of source internal resistance errors.

Static voltage drop in the source resistance: The error generated by the voltage source internal resistance is:

$$error_{(LSB)} = \frac{R_{SOURCE} \times I_{0Z1}}{V_{AREF} - V_{AGND}} \times 1024$$

For example : A source resistance of 15KΩ and a specified leakage current (I_{OZ1}) of ±500nA will cause a static voltage error of ±7.5mV or ±1.5LSB.

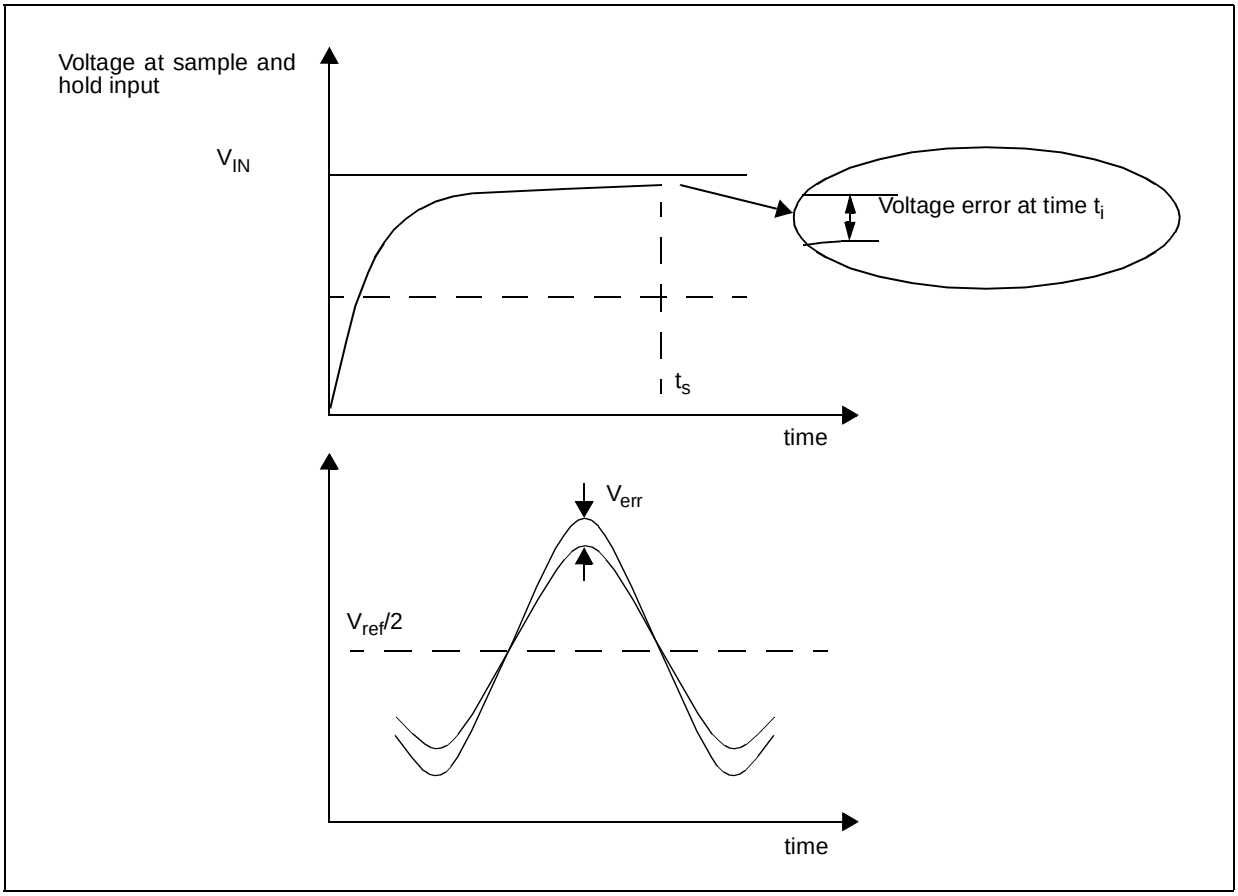
Refer the latest product datasheet for the value of I_{OZ1}.

Notes: 1. Input leakage current is caused by parasitic current at input pin protection; this protection is necessary to protect the device against ESD (Electrical Static Discharge) and against overload.

2. Adding a filtering capacitor at the analog input pin does not change the static voltage drop; it only improves the charging time of the internal capacitors (see after).

Poor charging of the ADC internal capacitance: During the sample time, the input capacitance (C_{IO} and C_{IN}) must be charged/discharged by the external source. The internal resistance of the source must allow the capacitance to reach its final value before the end of sample time:

Figure 2 : Possible Error Due to Input Capacitance Charging



If this does not happen, i.e. if the source resistance is mis-matched to the sample time, a voltage loss will occur at the sample and hold stage. This voltage loss causes an accuracy loss when increasing or decreasing the input voltage from Vref/2 (hold capacitor is pre-charged to Vref/2 before sampling to reduce charge/discharge time).

The error is be calcuated by the formula:

$$Max.error_{(LSB)} = \frac{1}{2} \times 1024 \times e^{\left(-\frac{t_S}{RC}\right)}$$

Where: t_S = sample time in µs, R = R_{SOURCE} + R1 in Ω, C = C_{IN} + C_{IO} in µF. For example:

Since the error is proportional to the difference between V_{IN} and Vref/2, the effect produces a non-linearity in the conversion of large-amplitude signals. In practice, if t_S>7RC, the maximum error is reduced to <1/2 LSB (<0.05%).

Errors due to noise from the input signal : The sample and hold circuitry is not designed to filter the input analog signal. Noise at the input signal will cause input voltage variation and, therefore, accuracy loss.

1.1.2 - Errors Due to High Frequencies from Input Signal

Small but high frequency signal variations can result in big conversion errors : During sampling time, the analog signal is fed to an internal auto-zero circuitry. Signal variations (2 opposite transitions at least) during this time can generate auto-zero error.

Signal variations during sampling time generate excessively high or low conversion results; big variations (ex : 150mV peak to peak variations at 1.5MHz, with a 2.5V offset for 1µs sampling time) can generates clamped results (0x000h or 0x3FFh).

=> Allthough the sample and hold internal circuitry is integrating signal variations, other internal analog circuitry can be affected by signal transitions during sampling time,

=> **The input analog signal shall always be low pass filtered to ensure that high frequencies are rejected**.

1.2 - Input Overload Errors

These errors are caused by input overload. During overload, internal protection-diodes sink current to reduce the overload voltage. Because of the close proximity of the internal protection-diodes and the ADC circuitry, the ADC performance is affected.

The ST10F269/ST10F280 accepts up to 10mA of input overload current while guaranteeing a Total Unadusjted Error (TUE) of ± 2LSB (refer to the product Data sheet for values).

Overload above the specified limit causes ADC accuracy loss and may damage the circuit.

1.3 - Reference Voltage Errors

The accuracy of the conversion is obviously linked to the accuracy of the reference voltage.

1.3.1 - Reference Voltage Accuracy and Absolute Tolerance on a Conversion Result

To compute the accuracy on conversion result, the accuracy on the reference voltage must be taken into account.

1.3.2 - Reference Voltage Accuracy and Differential Tolerance on Conversion Results

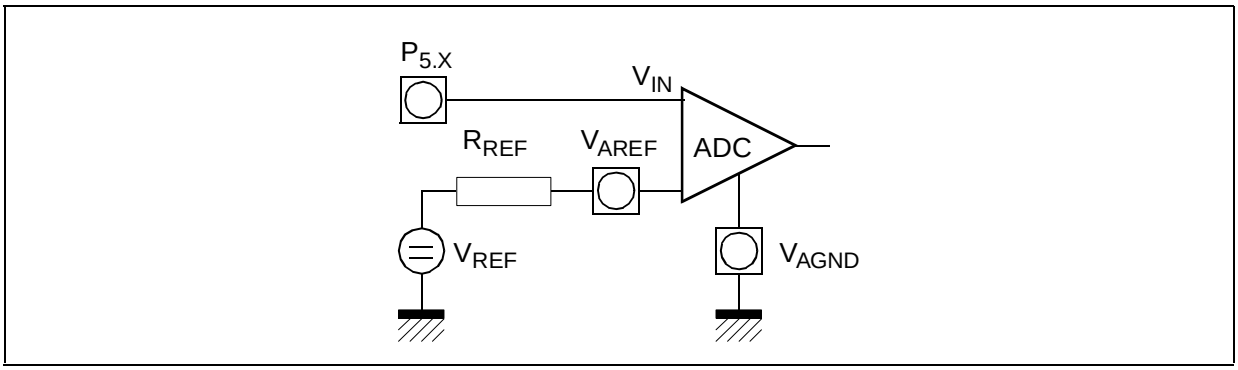
For differential computing (ie : difference between conversions), only the stability of the reference voltage is to take into account. When the analog voltage is derived from a voltage regulator, the accuracy on voltage reference is given by the rejection factor of the regulator and the maximum voltage variation that is possible between the 2 conversions.

Temperature : Temperature coupling effect may be neglected if the time between the 2 samples is short compared to the thermal constant.

While noise and/or voltage variations are a well known source of error, internal resistance is another source of error from the reference voltage.

During the conversion, the ADC internal capacitance must be repeatedly charged or discharged. The internal resistance of the reference voltage must allow the capacitance to reach its correct voltage within the conversion time (see figure below). A mis-match between the conversion time and reference voltage internal resistance will cause accuracy errors.

Figure 3 : Simplified Circuit for Analog Reference Voltage



2 - HOW TO MINIMIZE ERROR

2.1 - Optimise the Input Signal

There are four possible optimisations :

Minimise the total source impedance seen by the ST10: This means choosing sensors with low output impedance (not always easy for some types of sensor), and minimising the serial resistance of any protection devices between the analog source and the input pin (while still providing a voltage protection level compatible with the circuit specification).

Match the sample time to the analog source impedance: Use the formula that relates sample time to source internal resistance (given in the ST10 datasheet) to match the source resistance to one of the available sample times.

For example: With a source impedance of 10kΩ, and given

$$R_{ASRC} = (t_S / 330) - 0.25$$

then the minimum sample time is:

$$t_S = 330 \times (R_{ASRC} + 0.25)$$

$$t_S = 3380ns(min)$$

Note: This formula includes a safety factor of 10, therefore, dynamic errors are ≈0.02LSB.
Also, R_{ASRC} is the total source impedance seen by the device and, therefore, includes any protection components.

Match the sample time to the analog filter cut-off frequency to remove high frequencies : the ST10F269/ST10F280 sampling time (ADC silicon configuration) shall be 5 to 10 times shorter than the period of the cut-off frequency of the low-pass filter on ADC input signal.

Reduce noise at the input pin: Add an external RC filter (with attention to the source internal resistance). Comput the average value of different samples in the software routine.

2.2 - Reduce Input Overload Error

Because errors are induced from overload current going into/out of the integrated protection diodes, optimisations minimize this current in 3 ways:

Minimize the overvoltage at the analog source: The possible optimisations depend on the user application, typically, they involve the addition of zener diodes or transils. For component selection, please refer to ST-On-Line Discrete Devices / Protection Circuit Data Books.

Minimize the overvoltage at the ST10 analog input pins: Either, add protection diode(s) or transil(s), or add a serial resistor. CAUTION: the addition of a serial resistor increases the source internal resistance and, therefore, may impact maximum conversion speed.

Synchronise ADC conversion with analog transitions: Where possible, avoid carrying out conversions when analog inputs are scheduled to go into overload conditions (at least, during the transition phase).

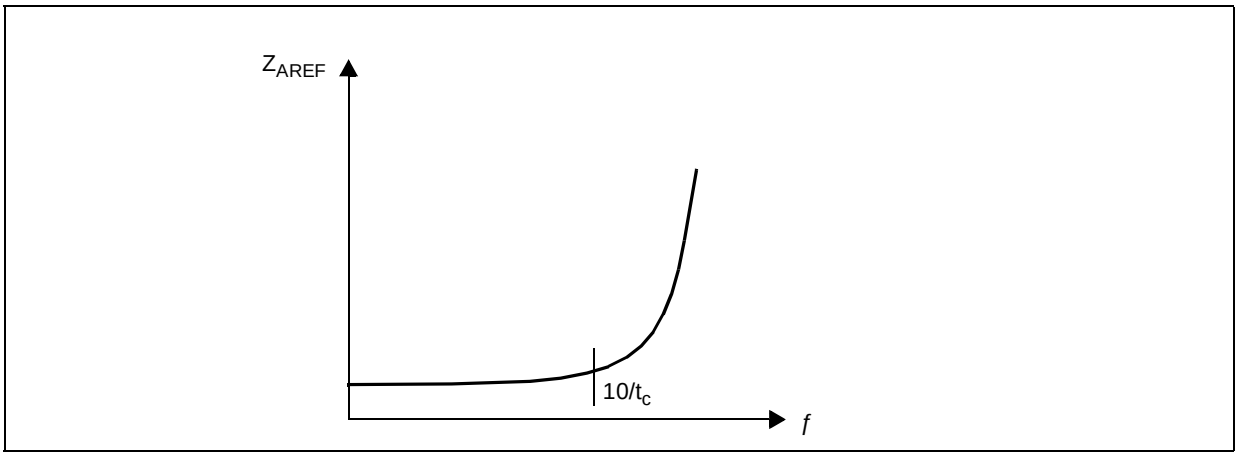
2.3 - Reference Voltage Error Reduction

The possible optimisations are :

Reference voltage noise: Noise can be reduced by carefull design, PCB routing and decoupling of the reference voltage:

- Place the analog-reference source as close as possible to the V_{AREF} pin.
- Avoid routing any high frequency/high amplitude signals near to the analog source.
- Make sure that the Voltage Reference source presents a low impedance from DC to well above the max. sampling frequency ($1/t_c$):

Figure 4 : Analog Reference Source - Impedance Characteristics



Match the reference voltage internal resistance to conversion time: Use the formula that relates conversion time to source internal resistance (given in the ST10 datasheet) to match the reference voltage to one of the 3 available conversion times.

For example: given

$$R_{AREF} = \frac{t_{CC}}{165} - 0.25$$

then the maximum source impedance for t_{cc} of 1200ns is:

$$R_{AREF} = \frac{1200}{165} - 0.25$$
$$= 7k\Omega(max)$$

Note: This should hold up to $f=10/t_C$, so if $t_C \approx 20\mu s$, $Z_{AREF} < 7k\Omega$, up to 500k

Figure 5 : Typical Analog Reference Circuit

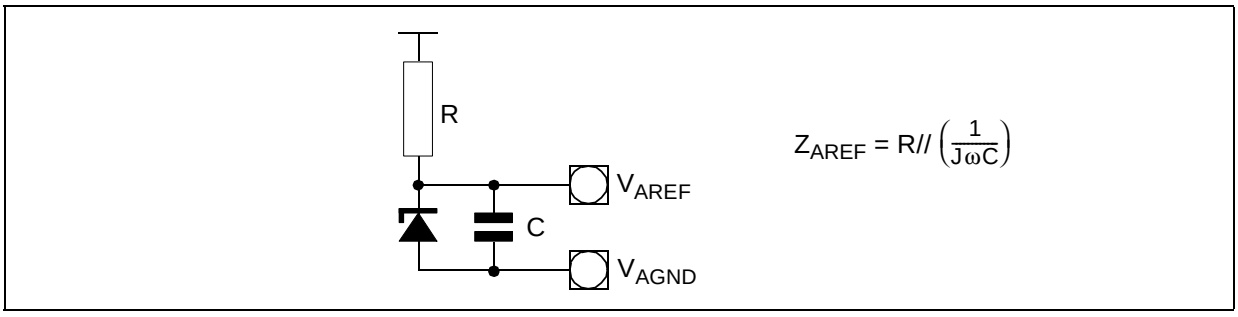


Figure 5 shows a commonly used circuit for the analog reference voltage.

3 - APPENDIX - DEFINITIONS

LSB : Least Significant Bit.

Resolution : defines the smallest input voltage change required to increment the output of the ADC between one code and the next adjacent code. Resolution is a design parameter rather than a performance specification; it says nothing about accuracy. Resolution is either expressed in percent of the full-scale, or in binary bits.

Accuracy : defines the worst case difference between the actual input voltage and the full-scale weighted equivalent of the binary output code. For ST10 devices, the Total Unadjusted Error describes the maximum sum of all errors intrisic to the ADC.

Intrisic errors : are errors intrisic to the ADC itself, such as: quantizing error, scale error, offset error, hysteresis error, linearity error. For simplicity and ease of use, the ST10 ADC specification gives the sum of all intrisic errors (Total Unadjusted Errors).

4 - REVISION HISTORY

4.1 - Creation of the AN1538 on the 14th of March 2002

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