AN1511
APPLICATION NOTE

Ensuring Compatibility Between M25P10 to M25P10-A and M25P05 to M25P05-A in Your Application

STMicroelectronics is constantly improving its technology. The 1 Mbit M25P10, and 512 Kbit M25P05, Serial Flash memory devices are being upgraded from our 0.35 µm T6X fabrication process to our new 0.18 µm T7X process.

This upgrade is in line with our declared commitment to support the growth of our customers on a long-term basis. The move to the new process helps to increase the performance of the product, to increase our customer's production throughput, to reduce our customer's delivery lead time, and to improve the service that we provide to our customers and that our customers provide to the end user.

The devices in the new T7X technology, the M25P10-A and M25P05-A, are an upgrade of the original T6X devices, the M25P10 and M25P05.

The new devices offer a more compact layout, and improved features such as:

- reduced Read time (using the new Fast_Read instruction)
- a double sized page
- reduced Page_Program time

The process change is described in PCEE0039 (PCN MPG/EE/0039), obtainable from your nearest ST sales office, but this application note gives a fuller description. Please see the data sheets, though, for the definitive specification of each of the products described here.

These changes can be transparent to the end user who seeks backward compatibility with the previous T6X devices, *provided that the conditions listed, later in this document, are met*.

HOW CAN THE CHANGE BE SEEN ?

The package remains unchanged, excepted for the top-side marking.

A letter 'U' is used as the process identification letter of the new T7X process, instead of the letter 'T' for the T6X process.

Table 1. Change of Top-Side Marking to Indicate the New Process

Top-Side Marking on the New T7X Devices	Top-Side Marking on the Previous T6X Devices
25P10AV AYWW**U**	25P10V6 AYWW**T**
25P05AV AYWW**U**	25P05V6 AYWW**T**

CHANGES

The adoption of the new T7X technology allows us to improve the most important AC parameters, and other key performance features, including a reduction of the die size. However, it should be noted that, in the process, the values of a few minor parameters have had to be relaxed.

We advise designers, who are currently designing with the M25P10 or M25P05, to check that their designs will continue to be compliant when they are switched to using the M25P10-A or M25P05-A.

Table 2. Changes

Parameter		Unit	M25P05-A M25P10-A T7X	M25P05 M25P10 T6X	Operating Conditions to Check
Page Size		bytes	256	128	The data to be programmed should not go beyond the end of the page (that is, page programming roll-over should not be used)
Sector Erase Cycle Time	max	s	3	2	The end of an Erase or WRSR internal cycle is checked by reading the Write In Progress (WIP) bit in the status register.
Bulk Erase Cycle Time	max	s	6	4	
Write Status Register Cycle Time (t_W)	max	ms	15	5	
V_{CC} Absolute Max Rating	max	V	4	5	V_{CC} should not exceed 4V
V_{IH} Absolute Max Rating	max	V	V_{CC}+0.4	V_{CC}+1	
Release From Deep Power-down and Read Electronic Signature	max	µs	1.8 (t_{RES2})	—	Verify that the memory is not accessed before the end of this delay Remark: If the RES op code is used when the memory is not in deep power down mode, it is not necessary to wait until the end of the both delays.
Release From Deep Power-down Without Reading Electronic Signature	max	µs	3 (t_{RES2})	1.6 (t_{RES})	
Deselect Time	min	ns	100	50	The delay between the deselect and the select must be higher than 100 ns
Clock Slew Rate	min	V/ns	0.1	—	The clock falling edge must be faster than 0.1V/ns
M25P05 Electronic Signature			M25P05-A 05h	M25P05 10h	Applications using the 512 Kbit Serial Flash memory device must be able to accept 05h as a valid Electronic Signature.

Memory Page Size

The number of bytes per pages has been increased from 128 to 256.

This improvement offers the advantage of doubling the number of bytes that can be programmed in a single go, thereby allowing time to be saved in production. Each programming sequence consists of the instruction opcode (1 byte), the memory address (3 bytes), and as many bytes as there are data to be programmed (from 1 to 128 for the M25P10 and M25P05, and from 1 to 256 for the M25P10-A and M25P05-A).

To program the total memory area of the M25P10-A (1 Mbit), 512 programming sequences are required instead of 1024 for the M25P10. This allows the programming management to be simplified, and reduces the programming time.

- half as many switchings on and off of the internal high voltage pump
- half as many opcode and address bytes to be sent
- half as many select, deselect or Write In Progress (WIP) bit polling to be managed.

If the number of data bytes sent in the programming sequence is greater than the number of bytes from the start address of the programming sequence to the end of the page, the programming roll-over feature causes subsequent data bytes to be programmed at the beginning of the same page. Consequently, devices with a 128-byte page will behave differently to those with a 256-byte page.

Fortunately, our experience is that this method is seldom used in applications because it is not too useful, and is hard to manage.

In more usual case of the master not sending data beyond the 128-byte page boundary of the M25P10 and M25P05, no problem will be encountered within the 256-byte page boundary of the M25P10-A and M25P05-A, and the data will be stored at the expected address.

This difference between the 128-byte page of the M25P10 and M25P05, and the 256-byte page of the M25P10-A and M25P05-A, has no effect on compatibility during READ instructions. Indeed, the Random Sequential Read instruction does not consider the page size, and allows all the memory to be read as a single block. At the end of each page, the address counter automatically increments to the next page, even with the high speed access of the M25P10-A and M25P05-A.

Erase and Write Status Register Relaxed Times:

For technology reasons, some timing parameters that are, in our experience, less critical to the vast majority of applications, have been relaxed.

- The maximum time to erase a sector becomes 3s instead of 2s,
- The maximum time to erase the whole chip becomes 6s instead of 4s
- The maximum time to write the status register time becomes 15ms instead of 5ms.

These are generally found to be non-critical because the program code is seldom updated in the end-user's application, therefore the erase feature and the write of the status register, to protect or unprotect the memory, are seldom invoked.

Where these operations *are* invoked, there are two methods that the application designer might have chosen to ensure that the memory is not used while the internal operating is still in progress:

1) A delay is imposed after the Erase or Write instruction. The application designer takes the specified maximum time from the data sheet, and sets a timer in the application that prevents the use of the memory during its internal operation. If this method has been used, then there could indeed be problems when upgrading from the M25P10 and M25P05 to the M25P10-A and M25P05-A. The solution is to increase the delay to the worst case specified in the two data sheets (3 seconds for Sector Erase, 6 seconds for Bulk Erase, and 15 ms for the Write Status Register instruction). Fortunately, the timer method

has not been used in any known application because, even on the M25P10 and M25P05, it has a performance that is so sub-optimimal (always waiting the maximum time).

2) Polling the Write In Progress (WIP) bit. The application polls the Write In Progress (WIP) bit (in the status register) to check the exact moment when the memory switches from the Busy to Ready state. This method allows the application to adapt to the speed of the memory on the board, and naturally adapts to the relaxed timing of the erase operation and write status register operations of the M25P10-A and M25P05-A.

Maximum voltage without damage

Advanced technologies are often more sensitive to overvoltage, due to the thinner oxide, than the earlier technologies, and this is the case for the T7X technology. There is a limit of 4V maximum overvoltage without a risk of incurring damage.

Time to Exit the Deep Power Down Mode

The Deep Power Down mode is usually used when the application knows that access to the memory will not be needed for some time. It is a type of sleep mode in which many internal functions, such as the high voltage pump, can be switched off. This not only reduces the current consumption, but provides an additional data protection for the memory content. (In Deep Power-down mode, the memory only responds to a correctly formated Release From Deep Power-down instruction).

Reinitializing the internal logic takes time, following the successful receipt of a Release From Deep Power-down instruction. The application must wait a minimum delay (t_{RES}, t_{RES1} or t_{RES2}) before sending another command to the memory device.

If another instruction is sent to the device before the end of this period, the correct execution of this instruction is not guaranteed.

The “Release From Deep Power-down and Read Electronic Signature” instruction can be use in three different ways:

1) To Exit from Deep Power-down, without Reading the Electronic Signature. The 8-bit instruction byte, on its own, is sufficient to take the device out of Deep Power-down mode, but the application must allow a delay (t_{RES}=1.6µs for T6X and t_{RES1}=3µs for T7X) before sending another command to the device, to ensure that the device is ready.

2) To Exit the Deep Power-down and Read the Electronic Signature. In this case, the instruction must be followed by three dummy bytes. The Electronic Signature is output from the memory in the byte period after that.

The M25P10 and M25P05, working at maximum frequency (20 MHz, t=50 ns), are ready to receive another command immediately after that, since the three dummy bytes and electronic signature byte take 4x8x50 ns to output, which is 1.6µs. This delay imposed by the clock pulse needed to output the Electronic Signature is enough to guarantee that the device will have completely left the Deep Power-down mode.

Due to the higher possible clock frequency of the new technology, these clock pulses are no longer sufficient to guarantee that the device will have completely left the Deep Power-down mode. For this reason an extra delay (t_{RES2}=1.8µs) has been defined in the M25P10-A and M25P05-A specifications to ensure the good behavior of the memory .

3) To Read the Electronics Signature. The RES instruction can be simply used to identify the memory device when it is not in Deep power Down mode, for example after a Power-up. No delay (not even t_{RES2}) is required following this use of this instruction, and so there is no difference when switching from the M25P10 and M25P05 to the M25P10-A and M25P05-A.

Deselect Time

For safety, the method of validating the instruction sequence has been improved, and now requires more time. Reinitializing the internal logic takes time, too, at the moment that the device is deselected. The application must wait a period of 50 ns, for T6X, and 100 ns, for T7X, between a Chip Select being de-asserted and being asserted again for the next instruction.

This means that applications that were designed for T6X devices (M25P10 and M25P05) and are to be fitted with T7X devices (M25P10-A and M25P05-A) must put in an extra delay. For example, at 20 MHz (clock period = 50 ns), it must wait the equivalent of two clock pulses before the device is selected again.

Clock Slew Rate

A new AC parameter was recently introduced in the M25Pxx data sheets:

The minimum value of the Clock Rising/Falling Edges:

– The minimum Clock Slew Rate is 0.1V/ns (that is, the maximum rising/falling edge is 33 ns when Vcc=3.3V)

The M25Pxx-A is designed to run at a high clock frequency, and the M25Pxx-A output buffers are designed accordingly. These output buffers are able to drive fast changes on the Q output pin, when the bus master reads the memory content, thus inducing a current peak from the V_{CC} line. The peak of current sunk by the M25P20, for example, is mostly dependant on the Q line parasitic capacitor.

To avoid problems during a Read operation, two points must be taken into account:

- the application environment, driving the M25Pxx, must be able to deliver a stable voltage supply (V_{CC}) independent of the variations of I_{CC} current. A common solution is to place a decoupling capacitor on the V_{CC} supply to damp the voltage drop when the M25Pxx is sinking a surge of current.
- The SPI bus master must send sufficiently short rising and falling edges on the clock, as specified by the parameter in the data sheet.

Applications offering a clock falling edge within the new AC parameter table are guaranteed to be accessed properly the M25Pxx-A in Read Mode.

M25P05 Electronic Signature

To differentiate the M25P05-A from the M25P10-A, a dedicated Electronic Signature (05h) has been implemented in the 512 Kbit memory. This is instead of the common Electronic Signature being used with the T6X technology (10h for the M25P10 and M25P05).

This new feature simplifies the design of applications that can use either device (512 Kbit or 1 Mbit). However, an application designed to use the M25P05 must accept the new signature given by the M25P05-A replacement device.

CONCLUSION

Applications currently using M25P10 and M25P05 devices, in T6X technology, can be fitted with M25P10-A and M25P05-A devices, in T7X technology, instead, without causing any problems of incompatibility, provided that certain precautions are taken in the design of the application.

Alternatively, applications currently using M25P10 and M25P05 devices can be fitted with M25P10-A and M25P05-A devices, and can make immediate use of some of the many benefits that the new upgrade offers.

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.serial-flash@st.com (for application support)

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.

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