AN1509
APPLICATION NOTE

A VERY HIGH EFFICIENCY SILICON BIPOLAR TRANSISTOR

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1. ABSTRACT

The potential of a high-performance low-cost silicon bipolar technology for high-efficiency low-voltage RF power amplifiers was explored. To this end, a unit power cell was developed by optimizing layout design, collector thickness and doping level. On-wafer load-pull measurements were performed which showed an excellent power-added efficiency of 83% at 1.8GHz under a supply voltage of 2.7V. Additionally, a 1W output power and a 74% PAE were achieved by a multi-cell packaged device with on-board testing.

2. INTRODUCTION.

Extended operating time has become a fundamental requirement for battery-operated systems such as handsets for mobile communications. Power amplifiers are the most power consuming components in portable equipment, so high power-added efficiency (PAE) is mandatory to enable long talk time and save battery life. Moreover mobile telephones must be small and lightweight. Power amplifier supply voltage dictates the required number of battery cells which mainly affects overall size and weight. Therefore, supply voltage reduction is a key design goal too.

Meeting both high PAE and low supply voltage with a silicon bipolar technology is a difficult challenge. Indeed, under low voltage conditions silicon BJT conduction losses and charge storage effects become prominent, thus limiting the maximum achievable output power and efficiency. Despite recent efforts in the development of RF silicon bipolar technologies [1-5], PAE values higher than 70% have not yet been reported for power transistors operating at supply voltages lower than 3V.

In this work a set of test devices was developed and characterized in order to optimize the PAE performance of a low-cost silicon bipolar technology. The extremely high efficiency of 83% was achieved at 1.8GHz with a supply voltage as low as 2.7V. The results presented herein show that silicon bipolar power amplifiers can be considered as excellent candidates for low-voltage low-consumption transmitters in mobile handsets.

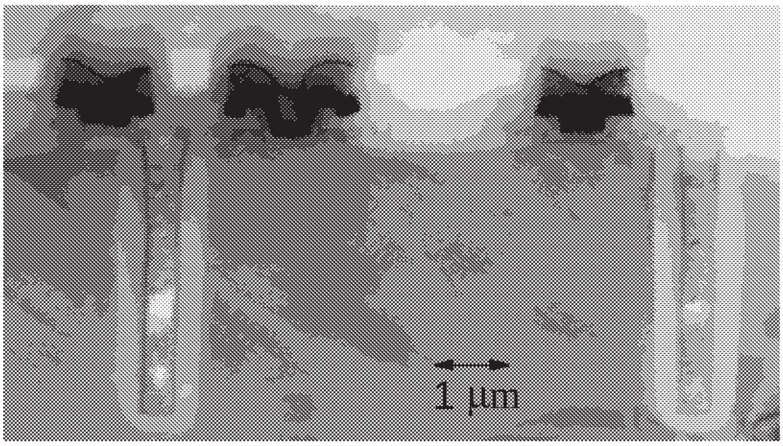
3. DEVICE DESIGN AND PERFORMANCE.

3.1 Fabrication Technology.

Devices were fabricated in a 46GHz-f_T double-poly 0.8µm self-aligned-emitter silicon bipolar process by STMicroelectronics (HSB3). An effective minimum emitter width down to 0.2µm is available and only 17 mask steps are required. The technology provides oxide trench isolation, three metal layers, optional gold metal layer, poly resistors, and metal-insulator-metal capacitors (0.7-fF/µm^2). On-chip spiral inductors are also available (3-µm-thick AlSiCu third metal layer) with Q values up to 9 at 1.9GHz and resonant frequencies above 10GHz.

Figure 1 shows a TEM cross section of a transistor with 0.8µm emitter mask size.

Figure 1: TEM Cross Section



3.2 Emitter Layout Improvement.

As a first step, the effect of layout design on the transistor power performance was investigated. To this end, two different power transistors were fabricated and tested, one with the standard continuous narrow strip (0.8µm) emitter and the other with a spot emitter. Mask-level spot size was set to 0.8µm × 2µm. Harmonic load-pull measurements were performed on the two test devices at a 2.7V supply voltage and a 1.8GHz operating frequency using a single tone continuous-wave (CW) input. Harmonic load impedances were tuned for maximum PAE, i.e. an open and a short circuit were provided at the second and the third harmonic, respectively, according to the dual Class F operation [6-8].

The comparison shown in figure 2 clearly suggests the best choice in the spot emitter layout which was further improved through a proper use of the higher metal layers for a better current draining. Figure 3 shows the layout of the optimized unit cell (48-spot emitter).

Figure 2: Comparison Of Measured Performance Parameters

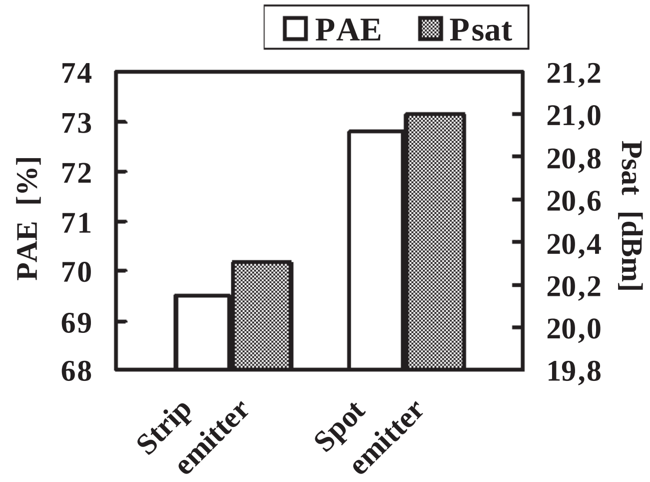


Figure 3: Layout Of The Optimized Unit Power Cell

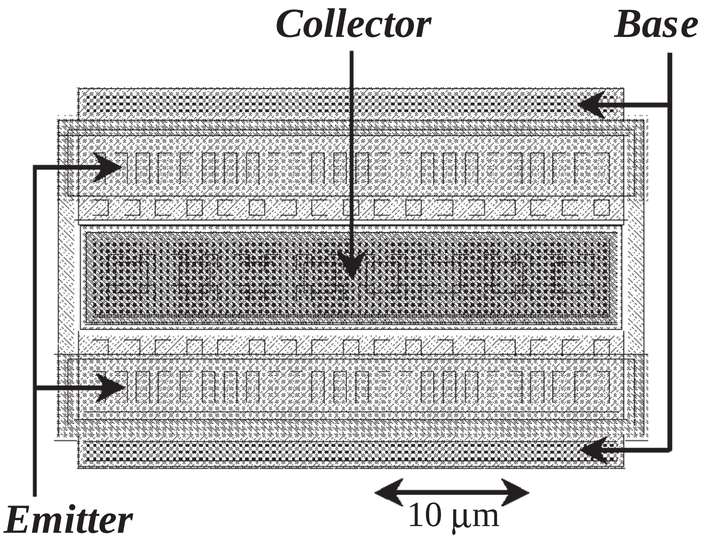


Table 1: Process Splits

Lot ID	Epi-layer thickness [µm]	Collector Dose
A	1.2 (standard)	Extra light
B	1.2	Light
C	0.8	Light
D	0.8	Standard

Table 2: Typical Performance Parameters

	A	B	C	D
$h_{FE\ max}$ (V_{CB} = 0V)	127	156	155	169
V_{AF} [V] (V_{BE} = 0.75V)	59	49	41	28
BV_{CEO} [V] (V_{BE} = 0.75V, I_B = 0A)	6.4	5.3	4.3	3.4
$f_{T\ max}$ [GHz] (V_{CB} = 0V)	22	28	32	45
f_{max} [GHz] (V_{CB} = 0V)	29	30	30	33
MAG [dB] (f = 5GHz, V_{BE} = 0.9V, V_{CB} = 0V)	8	13	15	17
P_{sat} [dBm] (f = 1.8GHz, V_{CC} = 2.7V, CW test)	17.7	17.8	20.3	20.4
PAE_{max} [%] (f = 1.8GHz, V_{CC} = 2.7V, CW test)	69	71	82	83
P_{sat} [dBm] (f = 1.8GHz, V_{CC} = 1.8V, CW test)	-	-	-	17.3
PAE_{max} [%] (f = 1.8GHz, V_{CC} = 1.8V, CW test)	-	-	-	75

3.3 Collector Optimization.

At the second step, the 48-spot power cell was used as the reference device to test the effect of both the collector thickness and doping concentration on transistor performance. Four process splits were carried out as shown in Table 1. For comparison purposes, the results of DC, *S*-parameters, and harmonic load-pull measurements are summarized in Table 2.

The best efficiency was achieved by reducing the epi -layer thickness to 0.8µm and with a standard SIC dose. The P_{out} and PAE performance was measured by the harmonic load-pull setup as mentioned before. A record 83%PAE and a 20.4dBm saturated CW output power were achieved at a 1.8GHz operating frequency and a 2.7V supply voltage, as shown in figure 4. The small-signal power gain was 18dB. A very good PAE of 75% was also obtained with a supply voltage as low as 1.8V. The Gummel plot and the f_T characteristics of the optimized unit device are shown in figure 5 and figure 6, respectively.

3.4 Multi-Cell Device Performance.

A multi-cell device (1000-spot emitter) was fabricated for on-package testing. The die was molded in a small plastic 20-lead EP TSSOP package which provides an exposed bottom pad for RF grounding and heat dissipation.

Package size is 4.4 × 6.5 × 0.9mm and thermal performance achieves a θJA of 40°C/W. A 25-mil clearance around the die allows downbonding, thus providing a low inductance path to the board ground. Moreover, the wafers were lapped to a 9-mil thickness for shorter downbonds. The critical emitter parasitic inductance was lowered to a suitable value by means of an on-chip ground plane (3rd metal layer) and a large number of downbonding wires.

Figure 4: P_{out} and PAE versus Pin For The Unit Power Cell (V_{CC}=2.7V, *f*=1.8GHz, CW test)

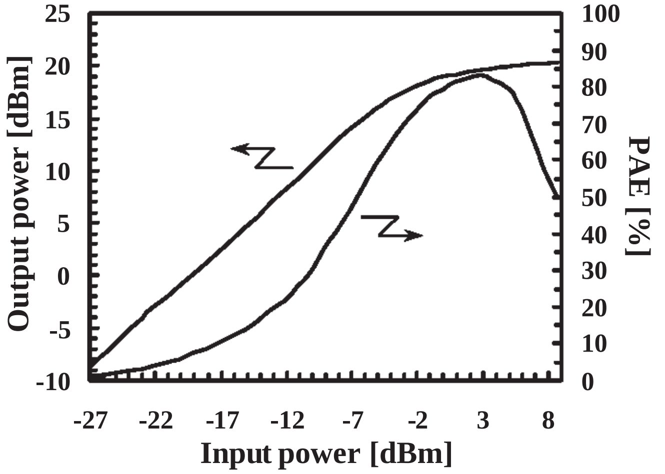


Figure 5: Gummel Plot Of The Unit Power Cell (V_{CB}=0V)

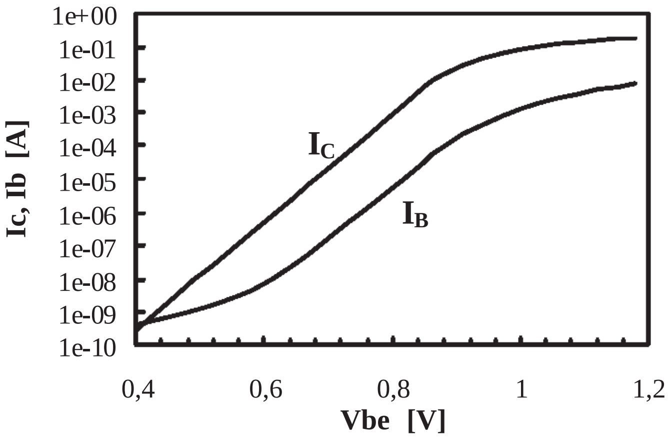
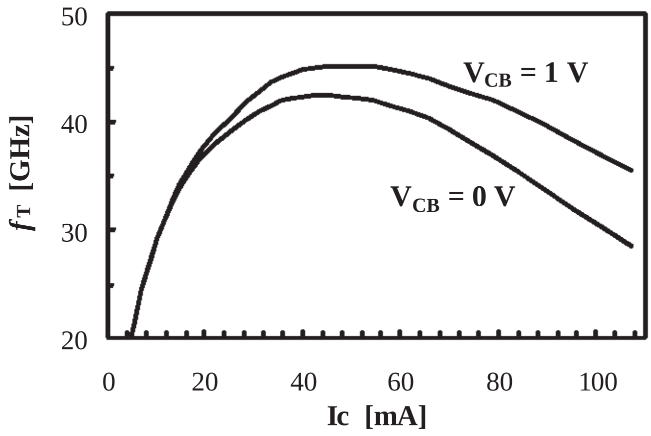


Figure 6: f_T versus IC For The Optimized Unit Power Cell



A die photo of the PA is shown in figure 7. The chip size is 2.8mm by 1.4mm, but a large part of this area (80%) was spent for the ground plane and ground wire pads.

The implementation of a Class-F-like multi-resonant load is quite difficult at RF frequencies because of package parasitics and process tolerances. Therefore, a single-resonator solution was selected for on-board testing (only second harmonic control was performed). According to nonlinear circuit simulations, the best power performance is achieved when a high reactive impedance tending towards an open circuit is provided for the harmonics of the fundamental frequency, i.e. by using a series -resonant load. Such a load leads to a pulsed collector voltage and a sinusoidal collector current (mixed-C mode [7] or Class C-E [9]). Dual waveforms, i.e. pulsed current and sinusoidal voltage, are generated by a parallel-resonant load. However, such a load produces a higher current peak, which causes an increased voltage drop across the collector series resistance and hence a reduction in PAE.

Figure 7: Die Photo Of The Multi-Cell Power Amplifier

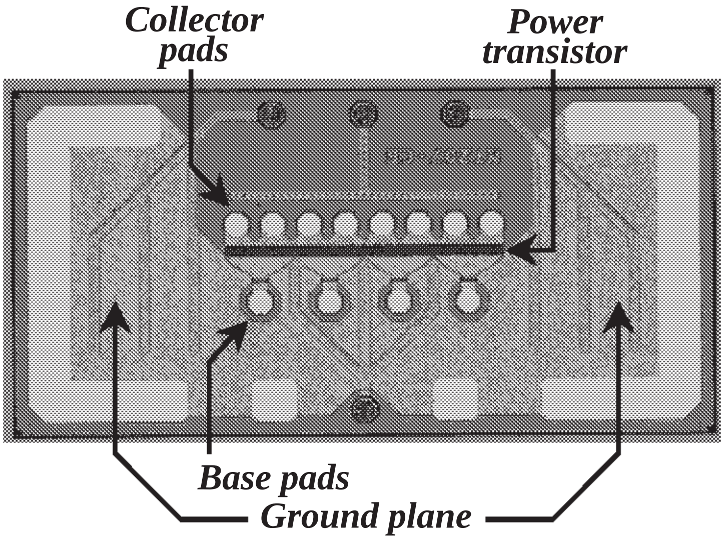


Figure 8: Matching Network At The PA Output

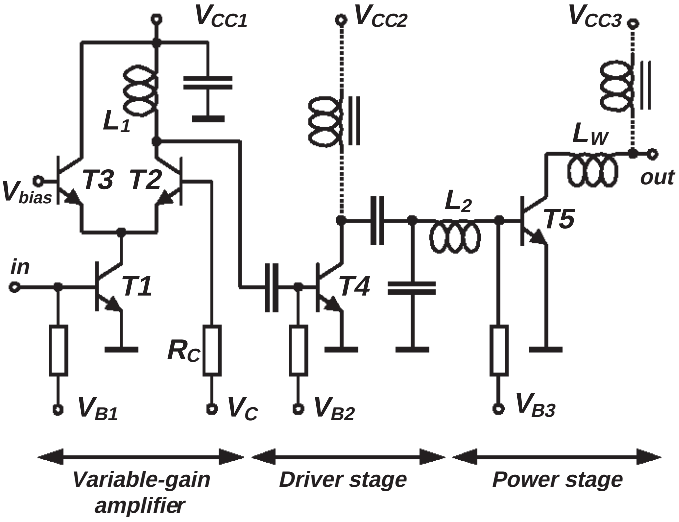
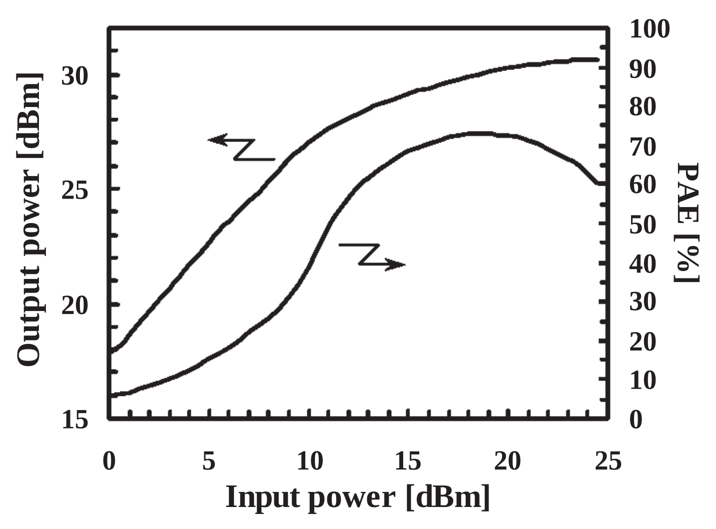


Figure 9: P_{out} and PAE versus Pin For The Multi-Cell Power Amplifier (V_{CC}=2.7V, f=1.8GHz, CW test)



Measurements were performed on a 400-thick FR4 substrate to agree with the low-cost production environment. Partially distributed impedance transformation networks were used for input and output matching as outlined in figure 8. Both lead and bondwire inductances (L_W) were properly taken into account to provide the device with an optimum second-harmonic load, i.e. a high reactive impedance performing an open circuit termination.

Figure 9 shows the CW output power and PAE performance versus input power at 1.8GHz. A 74% maximum PAE was obtained at a 30dBm output power level while operating with a 2.7V power supply. The small-signal power gain was 18dB. The second and third harmonics at the 50Ω load were 40dB and 32dB below the carrier, respectively.

4. CONCLUSION.

The low-voltage power capabilities of a high-performance low-cost silicon bipolar process were investigated. Variations in the emitter finger layout, epi-layer thickness, and selective collector implantation were been carried out in order to study the effects on PAE. Measurements showed that the combination of a spot emitter and a reduced epi-layer thickness enables very good device performance. Efficiency values up to 83% were achieved by on-wafer load-pull measurements on single-cell test devices operating at 1.8 GHz and 2.7 V power supply. Moreover, a 74%PAE and 30dBm output power were obtained with a multi-cell packaged device with on-board testing.

These results amount to the best power performance reported so far for a silicon bipolar device operating in the 1.8GHz band under a supply voltage lower than 3V.

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