



AN1351 APPLICATION NOTE

VIpower AND BCDmultipower: MAKING LIFE EASIER WITH ST's HIGH SIDE DRIVERS

P. Laupheimer

1. ABSTRACT

Industrial environments need high side switches in applications like PLC (programmable logic controllers) as actuators of lamps, valves and relays. STMicroelectronics is covering the complete spectrum of needed high side drivers combining high power handling capabilities, self-protection operations and diagnostic feedback.

Moreover, the robust design of the ICs ensures reliability and stability of such features even in very hostile environment conditions. It is then suitable to call such devices "Intelligent Power Switches" (IPS). This paper aims at explaining the most commonly faced problems in the Industry when dealing with IPS.

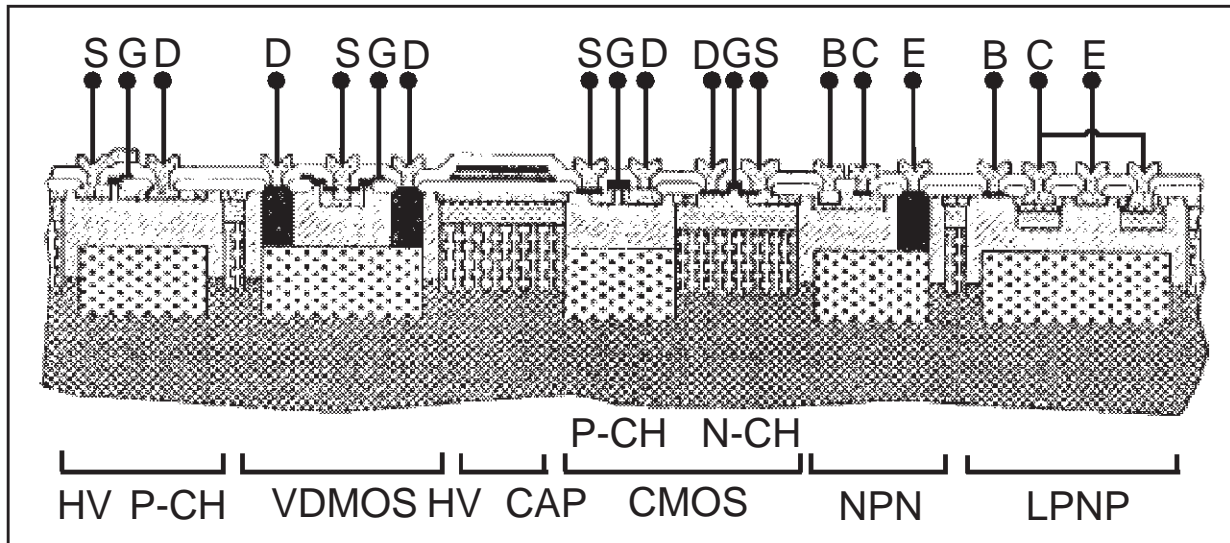
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The IPS spectrum of STMicroelectronics can be divided into two families depending on the technology process being used.

The first family is realized in BCD technology combining BIPOLAR, CMOS and Power DMOS on the same chip.

Figure 1: Example of Available Structures in BCD Technology



The BCD technology offers great design flexibility and allows the integration of very complex and precise circuitry.

Table 1: Available IPS in BCD Technology

Device	Function	Input(s)	Diagnostic	Current Limitation	Package
TDE1898	0.5A MONO IPS	Differential	2-bit	Internally set	SO-20L DIP-8
TDE1897	0.5A MONO IPS	Differential	2-bit	Internally set	SO-20L DIP-8
L6376	0.5A QUAD IPS	Single ended	1-bit	Internally set	PowerSO-20™
L6377	0.5A MONO IPS	Single ended	1-bit	Externally settable	SO-14 DIP-8
L6375	0.5A MONO IPS	Single ended	2-bit	Internally set	SO-20
L6370	2.5A MONO IPS	Differential	2-bit	Externally settable	PowerSO-20™

The second family is realized in VIPower® Technology (vertical intelligent power), a vertical process which monolithically combines a power stage with vertical current flow and a low voltage circuitry in a P-type buried layer, being thus capable of handling the same amount of power as discretes, while offering on-board a logic section and full protection.

Figure 2: Example of VIPower® M0 Technology

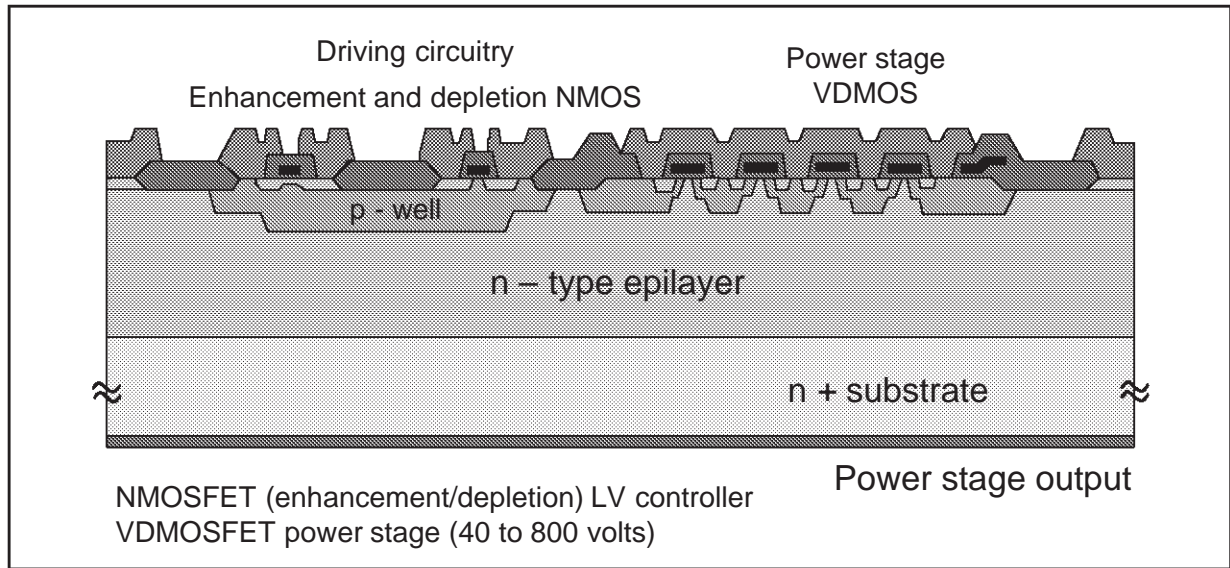


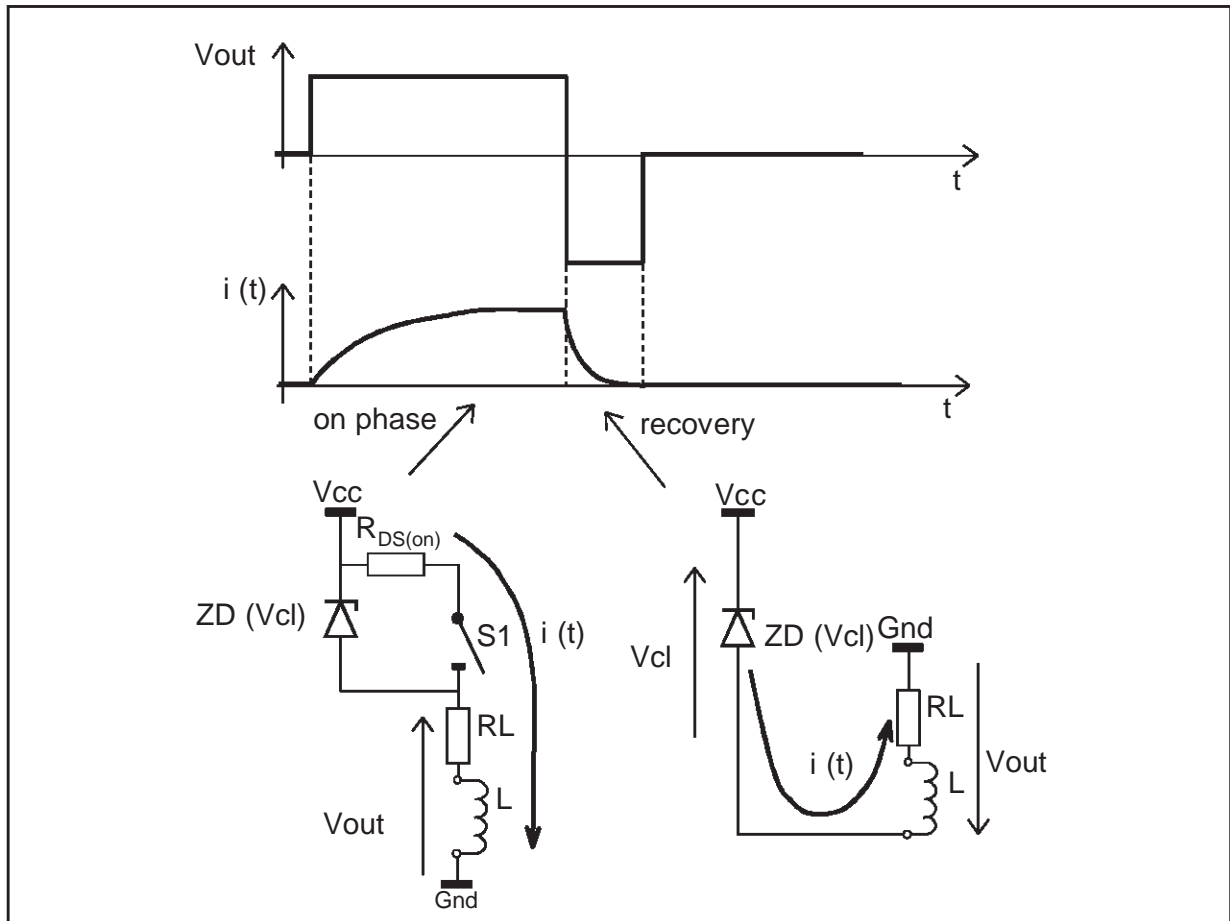
Table 2: Available IPS in VIPower® Technology

Device	Function	Input(s)	Diagnostic (All open drains)	Package
VN340SP	0.7A QUAD IPS	Single ended	1-bit/channel Short/thermal	PowerSO-10™
VN330SP	0.7A QUAD IPS	Single ended	1-bit Short/thermal	PowerSO-10™
VNQ860	0.35A QUAD IPS	Single ended	1-bit/channel Short/thermal	SO-20
VN800PT	0.7A MONO IPS	Single ended	1-bit/channel Short/thermal	PPAK SO-8
VN808	0.7A OCTAL IPS	Single ended	1-bit/channel Short/thermal	PowerSO-36 (in development)
VN540SP	2.5A SINGLE IPS	Single ended	1-bit/channel Short/thermal	PowerSO-10™

3. INDUCTIVE LOADS SWITCHING.

Typical inductive loads in industrial environment can range between several mill Henries and Henries. The worst case is normally considered to be 1.1H, 48W. The supply voltage is nominally 24V but can rise up to 30V.

Figure 3: Inductive Switching Exemplification



This means that the load can store energy up to:

$$E = \frac{1}{2} \cdot L \cdot I^2 = 215mJ$$

This energy has to be properly recovered at the switch off. Without appropriate circuitry the output voltage would sink at very negative values thus recovering the stored energy through the power transistor's breakdown. To avoid this, the output has to be clamped at $|V_{cl}| < |V_{Br}|$ with the addition of somewhat taking care of the discharge of the inductive load. According to figure 3 the demagnetization can be described by the equations:

$$I(t) = \frac{V_{out}}{R_l + s \cdot L} \quad V_{out} + V_{cl} = V_{cc}$$

and further:

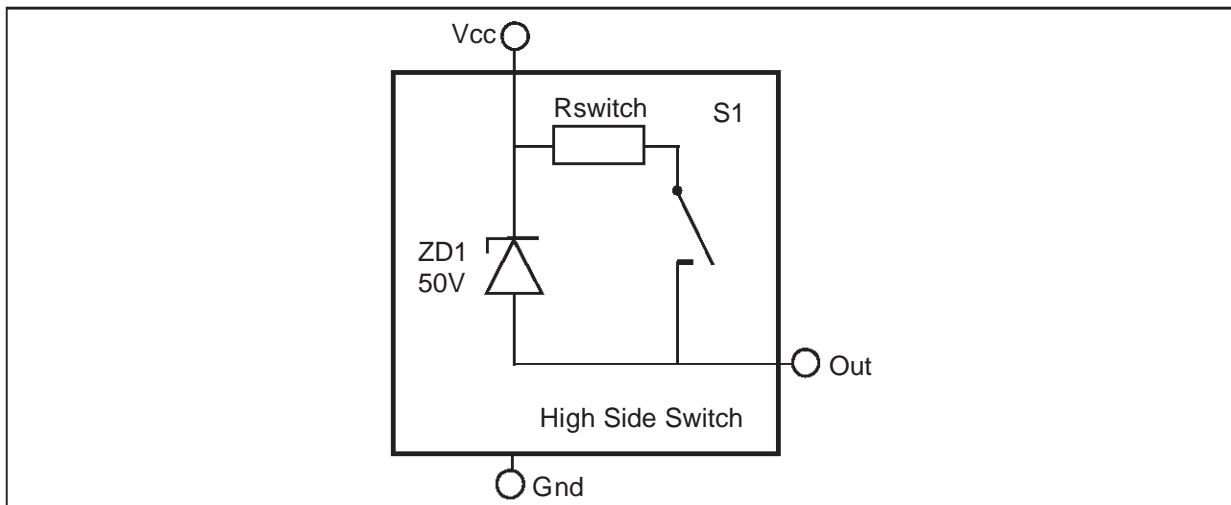
$$t = \left(-\frac{L}{R_l}\right) \ln \left[\frac{(V_{cc} - V_{cl} - I(t) \cdot R_l)}{-V_{cl}} \right] \quad (eq1.1a)$$

Eq.1.1 is to be respected until the load is completely discharged and the current reaches zero, which happens at T_{disc} with:

$$T_{disc} = \frac{L}{R_l} \cdot \ln \left[\frac{V_{cl}}{V_{cl} - V_{cc}} \right] \quad (eq1.2)$$

The value of the voltage V_{cl} will decide the duration T_{disc} of the demagnetization: the faster we want to switch off the bigger $|V_{cl}|$ compared with $|V_{cc}|$ has to be. STMicroelectronics' IPSs provide a "fast demagnetization" output structure, an integrated solution for fast switch off of inductive loads.

Figure 4: IPS Simplified Structure



It is basically a ZENER diode with about a 50V breakdown and high power dissipation capability connected between output and Vcc as in figure 4. Normally the output voltage is then clamped at $V_{cl} = V_{cc} - 50$, thus depending on supply voltage.

Although it is attractive because of place saving and component count, the integrated "fast demagnetization" structure cannot always be used: power dissipation inside the chip has to be limited. A detailed analysis of thermal behavior related to inductive loads switching is mandatory to avoid improper utilization of the IPSs.

3.1: Thermal considerations.

There are several contributions to power dissipation depending on the status of the device and on the way it has been chosen to demagnetize the load.

Off status: at any time the chip is dissipating a power P_{bias} just for its self-maintenance:

$$P_{bias} = I_{pol} \cdot V_{cc} \quad (eq1.3)$$

and solving it:

$$I(t) = I_0 \cdot \left(1 - e^{-\left(\frac{R_l}{L} \cdot t\right)} \right)$$

being $I_0 = \frac{V_{cc}}{R_{DS(on)} + R_l} \cong \frac{V_{cc}}{R_l}$ where R_l is the resistive value of the load and $R_{DS(on)}$ is the resistance

of the switch itself.

Then the power P_{dcon} dissipated inside the device during the on phase is:

$$P_{dcon} = \lim_{\infty} \frac{1}{t} \cdot \int_0 R_{DS(on)} \cdot I^2(t) \cdot dt = R_{DS(on)} \cdot I_0^2 \quad (eq1.4)$$

(supposing that $T_{on} \gg L/R_{DS(on)}$)

This thermal contribution to thermal dissipation is present just through T_{on} .

Switch off: the inductive load has been previously charged up to I_0 , at the switch off the corresponding stored energy has to be recovered.

Going back to eq.1.1a, the shape of the discharge current for a topology like the one in figure 3 is given by:

$$I(t) = \left(\frac{V_{cc} - V_{cl}}{R_l} \right) + \frac{V_{cl}}{R_l} \cdot e^{-\frac{R_l}{L} \cdot t} \quad (eq1.1b)$$

Equation (1.1b) is respected in the range $t=0$ (turn off) $t=T_{disc}$ (load completely discharged). According to figure 3 during this elapse the current $I(t)$ is flowing through the ZENER diode ZD. The amount of energy $E_{dturnoff}$ related to the turn off transition is then:

$$= \frac{V_{cl}}{R_l^2} \cdot L \cdot \left[V_{cc} + (V_{cc} - V_{cl}) \cdot \ln\left(\frac{V_{cl}}{V_{cl} - V_{cc}}\right) \right] \quad (eq1.5)$$

$$E_{dturnoff} = \int_{t=0}^{t=T} V_{cl} \cdot I(t) \cdot dt = \int_{t=0}^{t=T} V_{cl} \cdot \left[\left(\frac{V_{cc} - V_{cl}}{R_l} \right) + \frac{V_{cl}}{R_l} \cdot e^{-\frac{R_l}{L} \cdot t} \right] \cdot dt$$

The power $P_{dturnoff}$ dissipated by ZD during the turn off is then:

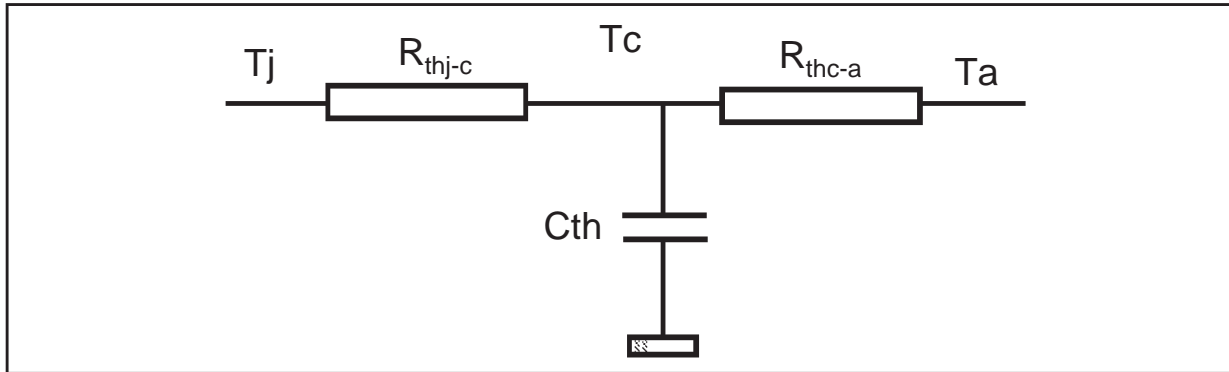
$$P_{dturnoff} = \frac{E_{dturnoff}}{T_{disc}} \quad (eq1.6)$$

This power is dissipated at each turn off in the element recovering the load's energy, this means we can either affect or not effect the junction temperature of the IPS, depending on whether the integrated fast demagnetization structure is used or not.

Internal fast demagnetization then leads to higher junction and case temperatures. Even if protected by thermal shut down integrated circuitry, it has to be avoided that the single energy surge, driving the IC into thermal shut down, overheats the junction: a wild transition could increase the local temperature (hot spot) a lot and damage the chip. The package and its overall on-board installation are then of vital

importance fixing the thermal impedance and consequently the dynamic thermal response of the silicon. The thermal model of a generic IPS can be exemplified like in figure 5: R_{thj-c} and R_{thc-a} represent the junction to case and the case to ambient thermal resistance, whereas C_{th} is the predominant thermal capacitance and it has basically to do with the package itself.

Figure 5: IPS Thermal Model



C_{th} is filtering the junction's thermal fluctuations: the case to ambient thermal resistance will then be interested just by the medium power and the case temperature will result to be more or less constant.

The aim of the designer will be to provide the lowest possible junction–ambient thermal impedance, in order to minimize the chip temperature jump-up.

To know the case temperature we need then the medium power:

$$P_{mean} = P_{bias} + P_{dcon} + E_{dturnoff} \cdot f_{switch} \quad (eq1.6)$$

Being T_a the ambient temperature is:

$$T_{case} = T_a + P_{mean} \cdot R_{thc-a} \quad (eq1.7)$$

$$T_{junction}^{mean} = T_{case} + (R_{thj-c} + R_{thc-a}) \cdot P_{mean}$$

Instead, the junction temperature will be sensible to instant power reaching then its maximum at the switch off because of internal fast demagnetization.

$$T_{junction}^{max} = T_{case} + R_{thj-c} \cdot \frac{E_{dturnoff}}{T_{disc}} \quad (eq1.8)$$

To simplify the designer's life ST provides its IPSs in packages representing a good compromise between provided thermal impedance and inexpensive price: that is basically the reason why very smaller silicon dies are placed in such big cases.

A numerical evaluation based on the previous equations can be now be easily performed: it will help in understanding the physical limitations that the board designer has to take into account.

3.2: An example: VN340.

The VN340SP is a monolithic device made using STMicroelectronics VIPower® Technology, intended for driving four loads.

Figure 6: VN340 Block Diagram

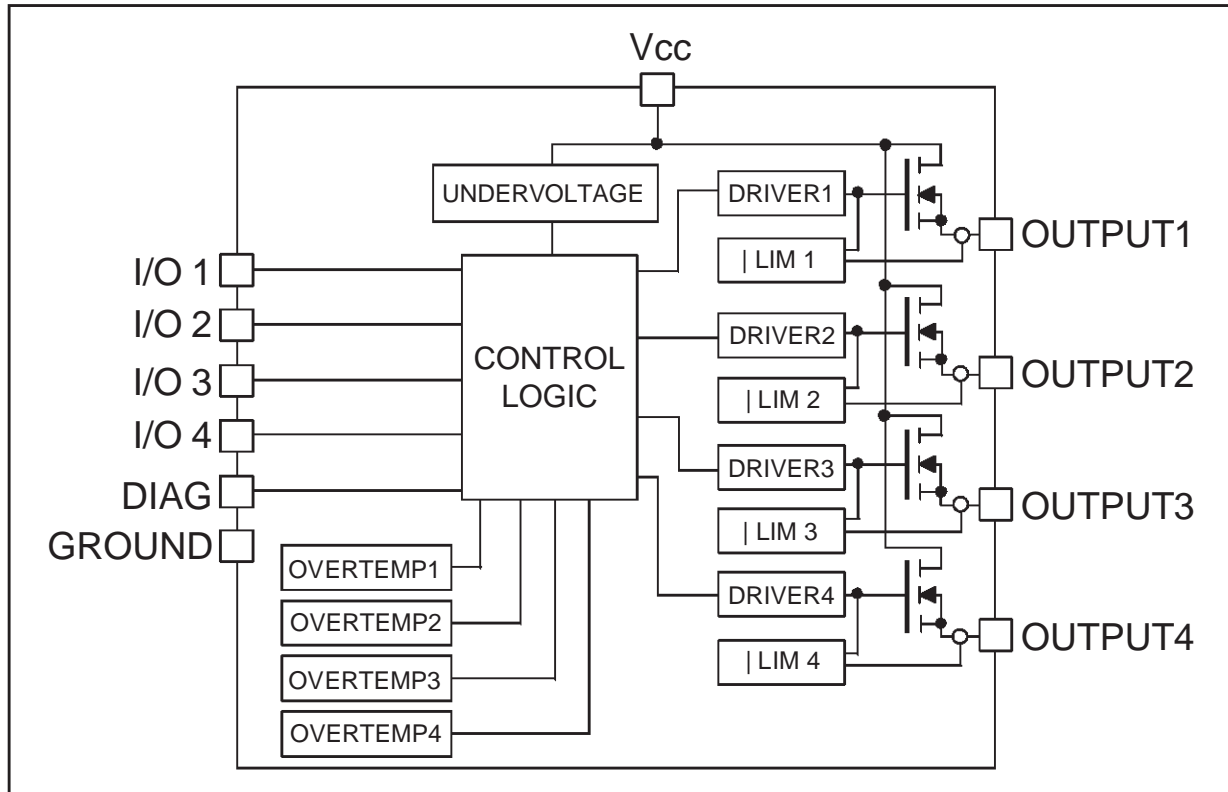
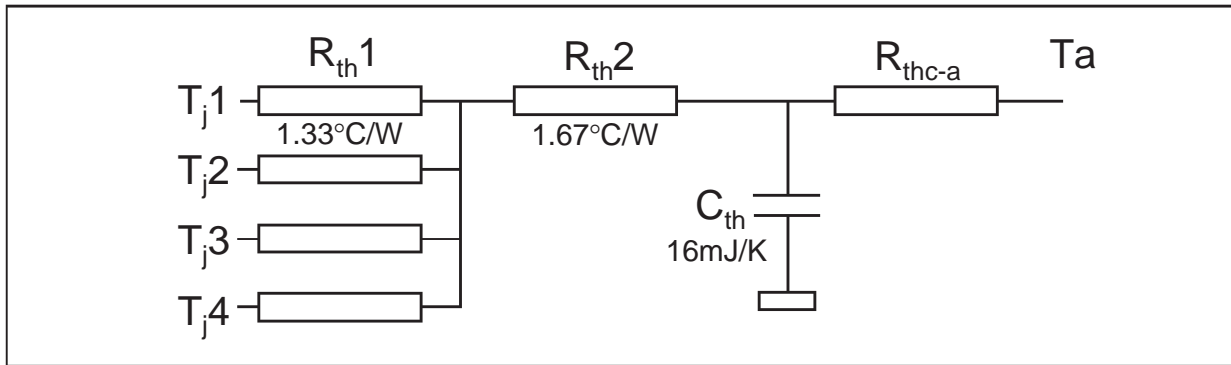


Table 3: VN340's Main Characteristics

<ul style="list-style-type: none"> - Output current 0.7A per channel - Digital I/Os clamped at 32V minimum voltage - Short loaded and over temperature protections - Built-in current limiter - Supply current 1mA (all channels off) to 6mA (all channels on, no load) 	<ul style="list-style-type: none"> - Under voltage shut down - Open drain diagnostic output - Fast demagnetization of inductive loads (@ $V_{cc} - 55V$) - Protection against loss of ground - $R_{DS(on)} = 0.32\Omega$ per channel (@ $T_j = 85^\circ C$), $R_{DS(on)} = 0.4\Omega$ per channel (@ $T_j = 125^\circ C$)
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It is presumed that all channels are on for 50% of the time, the switching frequency being 0.5Hz. Only one channel is switched off at a time (this implies 90° phase shift between the different inputs). The supply voltage is considered to be the maximum one: $V_{cc}=30V$, worst case. The load is 480hm + 1.15H.

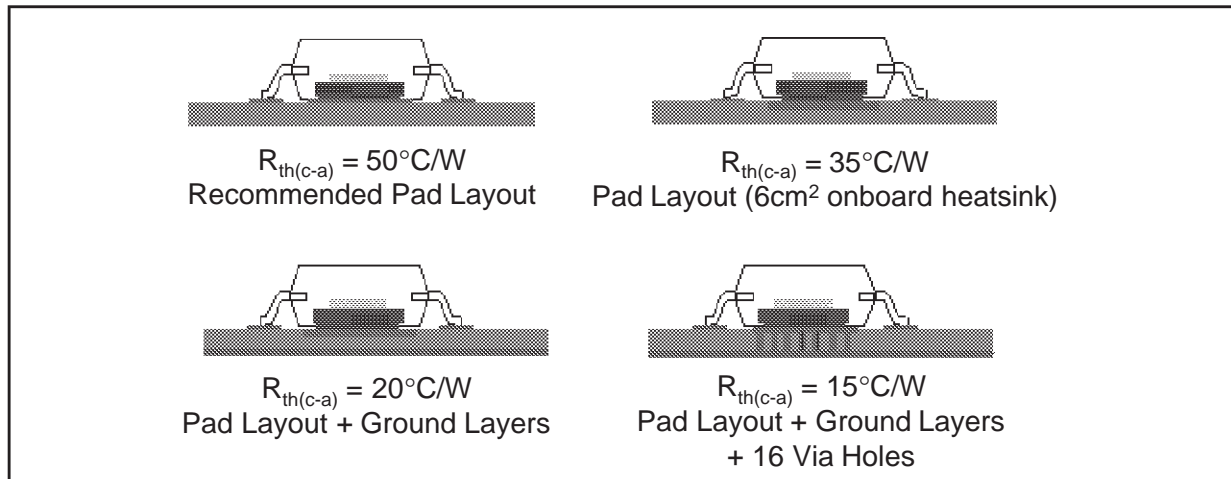
Figure 7: Simplified Thermal Model for VN340, 4-channel IPS



Note: In PowerSO-10™ there is a thermal time constant of 50msec without heatsink.

The VN340 has a typical R_{thj-c} of about 3°C/W for each single channel. On the other hand, being placed in a PowerSO-10™ package, the case to ambient thermal resistance will depend a lot on the final installation (see figure 8).

Figure 8: PowerSO-10/20™ Recommended Layout for High Power Dissipation Capability



In free air the PowerSO-10™ has a R_{thc-a} of about 50°C/W. Since it is very easy to reach much lower values of thermal impedance, for the calculations we will consider $R_{thc-a} = 40°C/W$.

The power dissipated due to simple biasing of the IC is (eq1.3):

$$P_{bias} = 180mW \quad (max)$$

The power dissipated during on phase is (eq1.4):

$$P_{dcon} = 156.25mW$$

for just one channel always on.

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Then, the 4 channels being on for 50% of the time the following has to be considered:

$$P_{dcontot} = P_{dcon} \cdot 4 \cdot 0.5 = 312.5mW$$

The energy dissipated during the turn off is (eq1.5):

$$E_{dturnoff} = 282mJ$$

Then assuming the ambient temperature $T_a = 60^\circ C$ the case temperature is (eq1.7):

$$T_c = 60^\circ C + [180mW + 312.5mW + (282mJ \cdot 0.5Hz) \cdot 4] \cdot 40^\circ C/W = 102.26^\circ C$$

The duration of the demagnetization phase is (eq1.2):

$$T_{disc} = 18.1ms$$

Finally the maximum junction temperature will be (if only one channel is switched off at each time!) (eq1.8):

$$T_{junction}^{max} = 102.26^\circ C + \frac{282mJ}{18.1ms} \cdot 3^\circ C/W = 149^\circ C$$

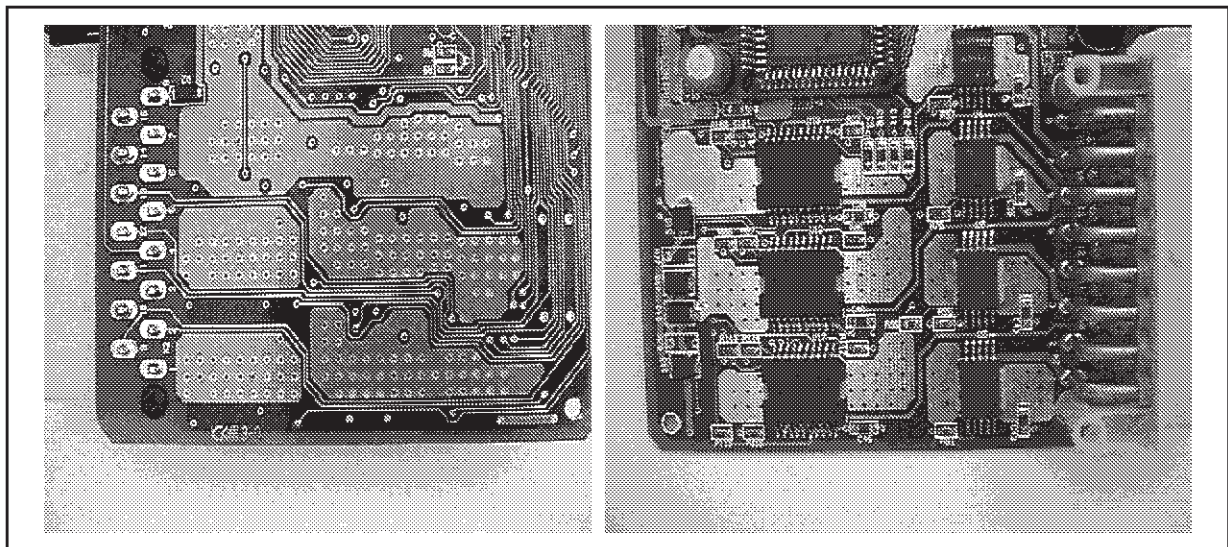
The device results then being operated in a safe condition (heating the junction to about $150^\circ C$ should generally be avoided).

Should the ambient temperature be higher than $60^\circ C$, the power handling capability of the PowerSO-10™ can be exalted providing a double metal layer on both sides of the PCB (connected one to each other by via holes), directly underneath the chip: the case to ambient thermal resistance drops to $15^\circ C/W$. This means that the case temperature will be now just $\Delta T_c = 15.85^\circ C$ higher than the ambient temperature, being:

$$\Delta T_c = [180mW + 312.5mW + (282mW \cdot 0.5) \cdot 4] \cdot 15^\circ C/W = 15.85^\circ C$$

Since the case to junction temperature gap will remain of about $42.26^\circ C$, the junction to case temperature drop is then about $58.11^\circ C$; this means that the junction temperature can be kept below the $150^\circ C$ even with $T_{ambient} = 90^\circ C$ (always if just one channel is switched off at a time!).

Figure 9: Top and Bottom of a PCB ($15^\circ C/W$ R_{thj-a} per each PowerSO-20™)



Caution: with internal fast demagnetization the safe turn off of 2 channels (248Ohm + 1.1H & $V_{cc}=30V$) simultaneously is also possible, but under precise installation conditions!

It is supposed that the thermal layout is well done (as in figure 9) and the designer achieved the 15°C/W of case to ambient thermal resistance. The ambient to case temperature drop is:

$$\Delta T_{c-a} = [180mW + 312.5mW + (282mW \cdot 0.5) \cdot 4] \cdot 15^\circ C/W =$$

Due to the energy of the 2 loads being simultaneously discharged the junction temperature will rise above the case temperature according to:

$$T_{jmax} = 50 + 15.85 + 93.48 = 160^\circ C$$

Now consider the worst case: the 4 channels switched off simultaneously. In this case ΔT_{j-c} has to be doubled, thus being: $\Delta T_{j-c} = 186.96^\circ C$ we have:

$$T_{jmax} = 50 + 15.85 + 186.96 = 252.8^\circ C$$

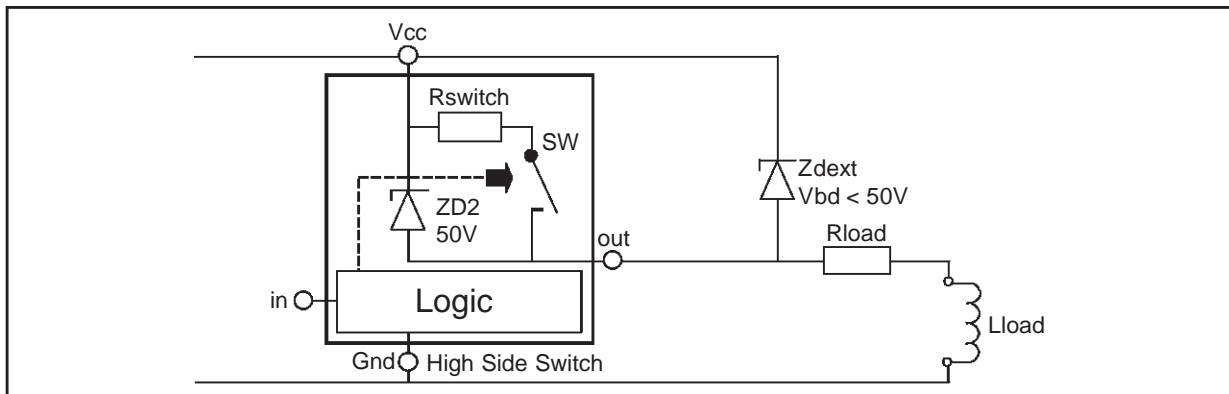
In these extreme operating conditions ($V_{cc}=30V$, Load=48+1.1H, $f_{switch}=0,5Hz$ d=50%) **no more than 2 channels should be switched off at a time if the integrated fast demagnetization structure has to be used!**

3.3: Switching Activity Above 0.5Hz.

Anywhere heavy inductive loads (such as 1,1H/48Ω, or energetically equivalent i.e. 215mJ) have to be switched above 0.5Hz, external demagnetization has to be used in order to lower the power dissipated inside the device.

A recommended solution for the external recovery is the replication of the internal structure: a zener diode between the output pin (anode) and V_{cc} (cathode). The zener should have a breakdown voltage of less than 50V, which represents the breakdown voltage of the internal zener: in this way the recovery will surely perform externally, in any operating condition.

Figure 10: Correct Topology for External Recovery



Demagnetization to ground is also surely possible but discouraged, since the clamping voltage of the external element will result to be fixed at $-V_{breakdown}$ (and if just one protective diode has to be used it will have to be bi-directional with $V_{breakdown} > V_{cc}$ to avoid conduction during normal operation) while the internal structure will react at a voltage depending on the supply: $V_{cc} - V_{zd2}$ (where V_{zd2} is the integrated

structure's breakdown voltage. This means that the energy will be externally recovered just if $V_{cc} - V_{zd2} < V_{breakdown}$, that is for low supply voltages!

External demagnetization is also strongly recommended each time it is needed to have the power outputs protected from surge pulses. To know more about this please refer further to the section "POWER OUTPUTS".

4. KEY TO IMMUNITY.

The industrial environment results in being a noisy and harsh environment. Nevertheless the applications have to stay reliable. Therefore most of the typical disturbances coming out in such an environment have been modeled. The aim is to simulate those disturbances, check whether they can affect the application to be used or not, and consequently to ensure a proper operation once plugged in the real environment. In the present section it is intended to examine a typical application in the industry field: multi-channel high side driver modules. The following pages show also the importance of correct layout in reducing the stress on components.

Two examples will be further given, using two different high side driver products from STMicroelectronics: VN800 and L6377. But before doing this let's go a bit more inside the alchemy of immunity.

4.1 The Norms in Brief.

4.1.1 General Statements.

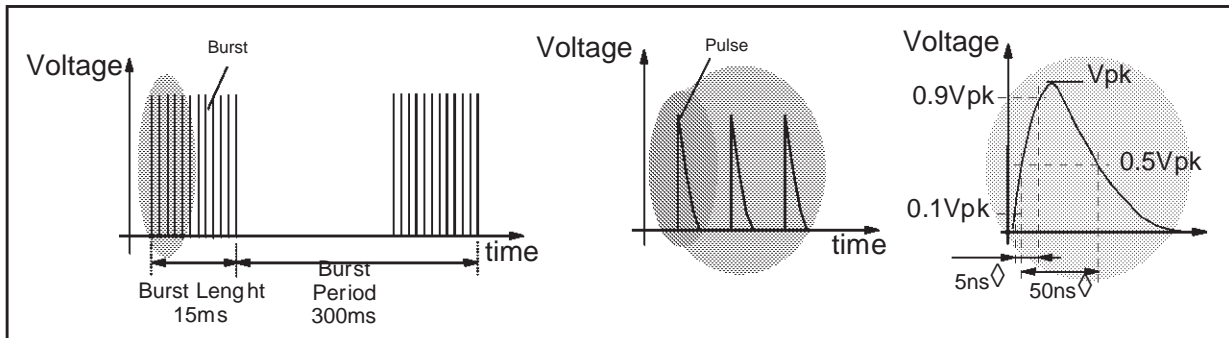
For all of the normative standards to be introduced after this one, different levels of the test signal to be applied are defined. Corresponding to each of these levels, the test results are usually classified into four different categories depending on the related behavior of the EUT:

- 1: normal performance;
- 2: temporary degradation or loss of function or performance, with automatic return to normal operation;
- 3: temporary degradation or loss of function with requirement of external intervention to recover normal operation;
- 4: degradation or loss of function, needed substitution of damaged components to recover normal operation.

4.1.2 Electric Fast Transients (bursts, IEC801-4; EN61000-4-4).

Mechanical switching of inductive loads can generate high voltage spikes in form of repetitive pulses. The test signal is shown in the below picture and is the periodic repetition of fixed length packets of spikes (bursts, henceforth shortly called EFT). The single spike contained in one packet has a very short duration, and despite its high amplitude, the related energy is low (the maximum deliverable energy into 50ohms with a peak amplitude of 2kV is 4mJ for each pulse).

Figure 11: EFT - Rising and Duration Time ($\pm 30\%$) are Referred to a 50ohm Load



Due to its really fast rising edge (5nsec!) the EFT has a very rich spectrum up to high frequencies. The frequency with the highest energetic content is about 150–200MHz, with further harmonics at higher frequencies. Due to this spectral distribution this disturbance can easily penetrate inside electronic devices following parasitic paths.

It is very easy to couple the bursts from one cable to another especially if those cables are close one to each other and parallel to each other.

For evaluation purposes EFTs have to be applied both on supply lines, by means of CDN (coupling decoupling network; basically a passive network ensuring that just the equipment under test will be, at least directly, affected from the disturbance), and on signal and power lines, by means of a capacitive coupling clamp, through which the cables to be perturbed flow. Amplitude and repetition rate of single pulses internally at each burst are below reported.

Table 4: EFT Test Severity Levels Classification

Severity Level	Supply Line Test Voltage	I/O Lines Test Voltage
1	0.5kV (@5kHz)	0.25kV (@5kHz)
2	1kV (@5kHz)	0.5kV (@5kHz)
3	2kV (@5kHz)	1kV (@5kHz)
4	4kV (@2.5kHz)	2kV (@5kHz)

During evaluation EFTs have to be applied to the equipment under test (henceforth called EUT) for at least one minute.

4.1.3 Surge (IEC801-5; EN61000-4-5).

With “surge” a single non-repetitive high-energy pulse is intended. Basically it can be a consequence of switching operations in the power grid or even of nearby lightning strikes. The high–energy content is coming out of high peak voltage value and long time duration of the test signal.

This pulse can be applied by means of three different coupling methods. For the supply lines the test signal can be applied both directly from one line to the other one and from one of the two (for a single phase power supply) lines to the PE. For the other lines just the line to PE coupling is possible.

For each of the security levels fixed from the standard, different values of the peak voltage of the test

signal are defined, depending on the type of line to be tested and the selected coupling method.

Table 5: Surge Test Severity Level Classification

Severity Level	Supply Line (Line to Line)	Supply Line (Line to PE)	Signal Line (Line to PE Only)
1	-	0.5kV	0.5kV
2	0.5kV	1kV	1kV
3	1kV	2kV	2kV
4	2kV	4kV	-

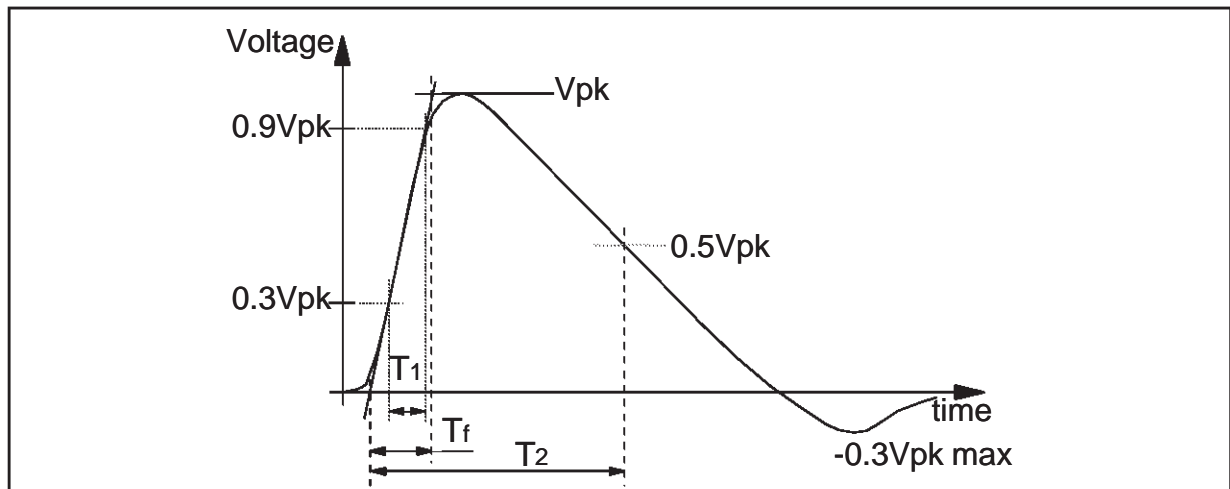
The generator impedance is variable as reported in the next table, depending on the lines to be tested and the coupling to be adopted.

Table 6: Surge Generator's Impedance Depending on Test Coupling

Supply (Line to Line)	Supply (Line to PE)	Generic Line (Line to PE)
2ohm	12ohm	42ohm

Therefore the current delivering capability of the test signal can vary a lot rising up to a theoretical maximum of about 1kA.

Figure 12: Surge Waveform



Note: front time $T_f = 1.67 \times T_1 = 1.2 \mu\text{sec}$; time to half value $T_2 = 50 \mu\text{sec}$

The harmonic content of the surge is extending from 3 to 300kHz, thus resulting not critical regarding parasites. Instead, peak current and peak power are the most problematic issues. During evaluation at least 5 pulses have to be applied for each polarity with a maximum repetition rate of one pulse each minute.

4.1.4 Current Injection (IEC801-6; EN61000-4-6).

Due to many radio frequency transmitters the environment is heavily polluted by electromagnetic fields. Consequently in a real environment all of the cables will act as receiving antennas, with possible impact on the device’s performances. The test signal is basically a sinusoidal waveform whose frequency is sweeping from 150kHz up to 80MHz; with a 80% amplitude modulation at 5kHz of the same signal. The analytic expression is this following one:

$$S_{test}(t) = V_{test} \cdot \sin(2 \cdot \pi \cdot f_{sweep} \cdot t) \cdot [1 + 0.8 \cdot \sin(2 \cdot \pi \cdot f_{mod} \cdot t)]$$

where $V_{test} = V_{rms} \cdot \sqrt{2}$ (see table below), $f_{mod} = 1kHz$ and f_{sweep} varies linearly with the time from 150kHz up to 80MHz.

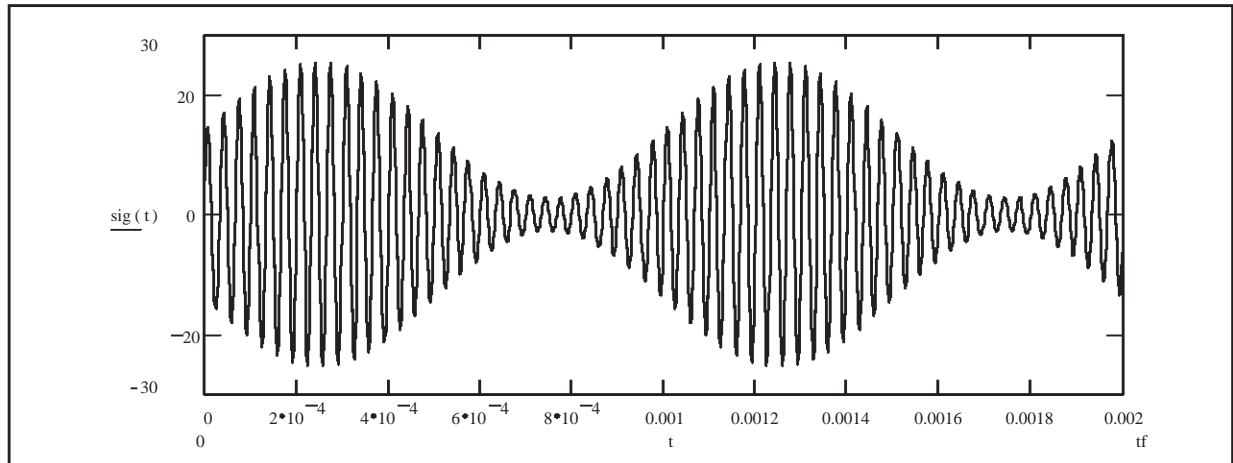
Three amplitude levels are specified corresponding to different immunity levels.

Table 7: Current Injection Test Severity Level Classification

Severity Level	Test Signal (V_{rms})
1	1V
2	3V
3	10V

Figure 13 gives an idea about what the test signal looks like for a given f_{sweep} and $V_{rms}=10V$.

Figure 13: Current Injection Test Waveform



The sweep in frequency is too slow to be estimated in a few sinus cycles; it is up to the reader to imagine the external envelope (due to the 1kHz amplitude modulation) fixed and the internal sinus wave faster and faster.

This test signal can be applied both on supply lines (by means of CDN), and on I/Os (by means of a capacitive coupling clamp).

4.2 Measuring Tips.

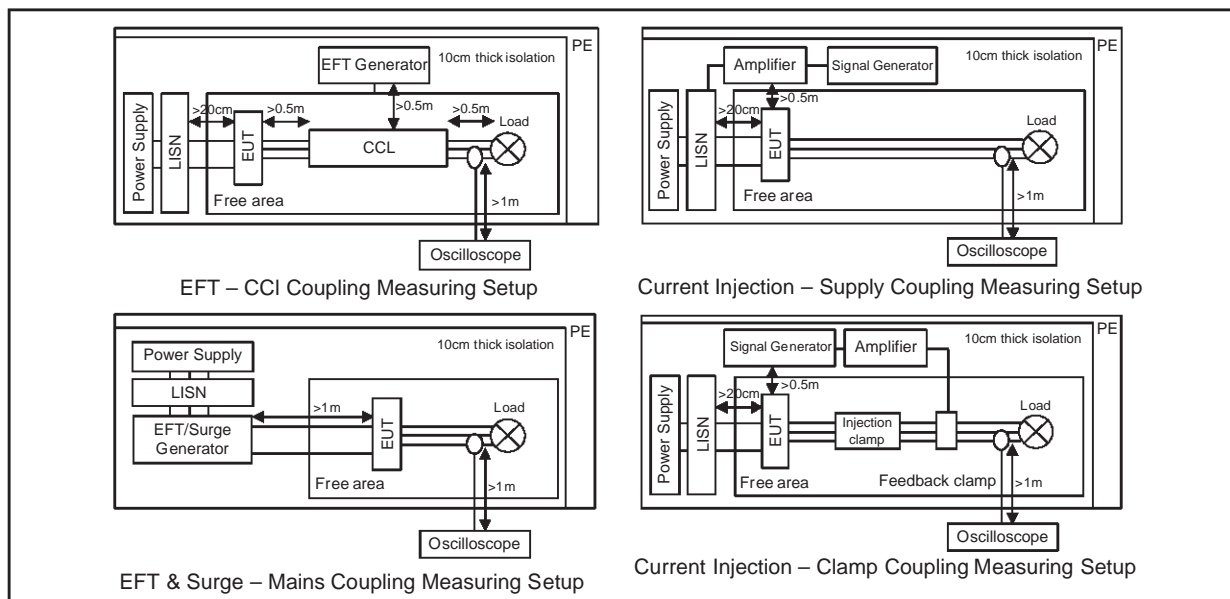
The first problem to face investigating immunity is to avoid perturbing the system, while observing it. There are several ways to check if the EUT is working properly, but they are not all equivalent in practical terms.

Performing immunity tests, current measurements (through current probe) should always be preferred, when the values to be measured are compatible (typ. > 10mA). Current probes provide a contactless view of the electrical behavior of the EUT. This avoids injecting additional noise, a thing really easy to be done especially when applying EFT, due to their rich harmonic content. Anyway normal voltage probes should always be avoided due to the fact that the ground lead will close a loop to the protective earth (henceforth called PE) producing a huge increase in injected disturbance. Then if no current probe can be used to perform the measurements, differential voltage probes must be used. For sure the results will not be as good as when a current probe is used, since the parasitic capacitance given by a differential probe is much bigger. In case of EFT the antenna effect provided from the probe itself and its cables must be considered too.

Even proceeding with current probes, excess noise can be coupled too: the probe's cables must not lay on PE or on metallic surfaces, as well as they should not run parallel and close to the perturbed lines or the capacitive coupling clamp itself. A good thumb rule is to let them lean on a insulating material ensuring at 10cm distance between the cable itself and PE. The closest distance between the probes (intended as both sensing element and cables) and the complex EFT generator plus capacitive coupling clamp should be at least 50cm. Further reduction in captured noise is achieved disposing the probe's cable in orthogonal direction to that of the capacitive coupling clamp.

Anywhere it is possible it is suggested to use batteries as power supply, in many cases it can happen that, even perturbing just the signal lines, the power supply is indirectly affected too, because of its low immunity capability. It is then possible to have a non determined output voltage and consequently the EUT can fail. It happens very often that the power supply output latches to the maximum output voltage.

Figure 14: Measuring Setup



Note: The PE is a conductive plane placed on a 1m high wooden table

5. THE LAYOUT.

Of course filtering is important but it must not be forgotten that layout is of vital importance as well. With optimized layout much simpler filtering solutions can be chosen, or, even worse, with a bad layout immunity cannot be achieved at all, even with huge filters.

What does "good layout" mean? Basically parasitic inductances have to be reduced as much as possible, capacitive filtering must be effective and geometry has to be regular and symmetric. Now we can examine in detail each single part of the board and discover what should always be done to get the best out of our application.

5.1 V_{CC} and GND lines.

V_{CC} and ground lines should lay on top of each other, minimizing the area of the closed loop increasing the capability of the application to reject the environmental noise.

Another big advantage provided by this solution is the reduction of parasitic inductance on the lines. This is especially important on lines carrying high dv/dt and di/dt .

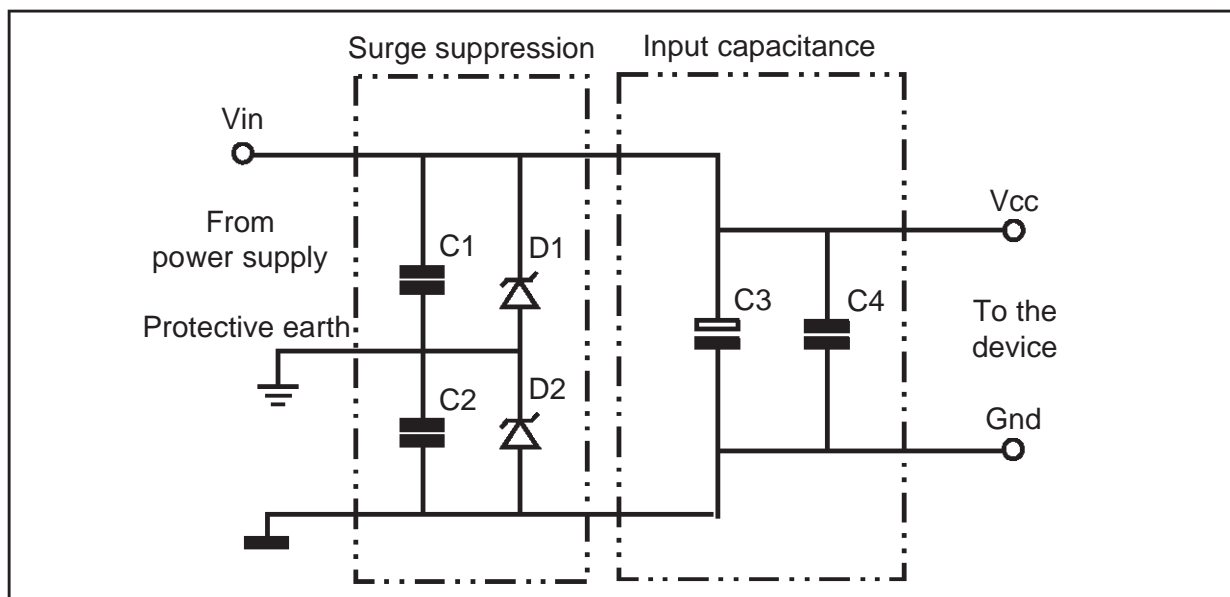
Two layer boards are consequently strongly recommended (for details see the application note AN358 "Environment design rules..." by B.Maurice).

Generally it is best to place the high current PCB wire going into the application on one side and the PCB wire going out just below on the opposite side of the PCB.

5.2 Input structure (Supply).

The suggested structure is like a chain: surge suppression block followed by the input capacitance block.

Figure 15: Suggested Input Structure



5.2.1 Surge Suppression Block.

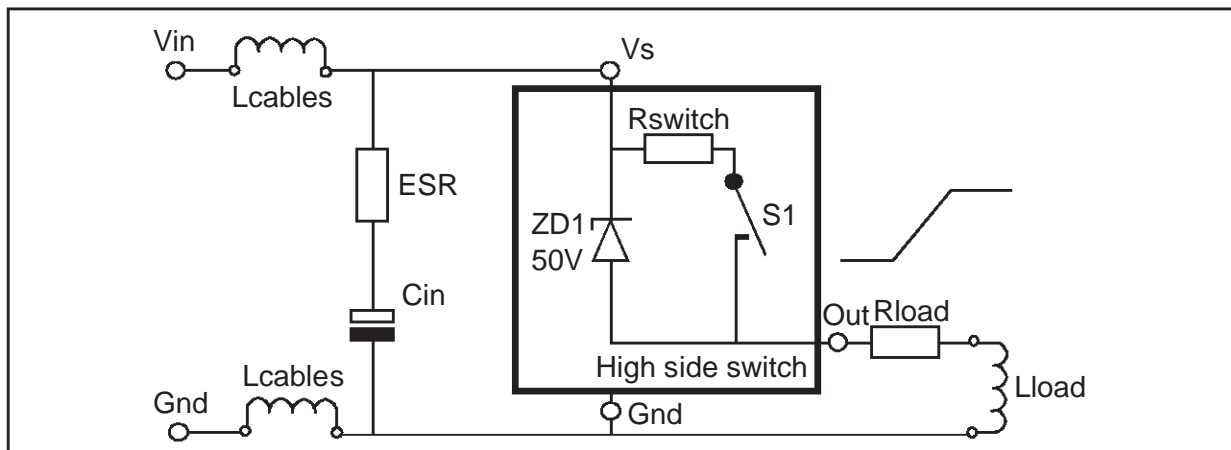
A surge suppression block is a two unidirectional Transil (for a reference guide about ST Transil clamping voltage, current and power dissipation capability please refer to: <http://us.st.com/stonline/products/index.htm>) serial structure (refer also to the section “REVERSE BATTERY”). This serial structure (D1+D2) brings the great advantage to double the current capability of the protection stage. For a bus voltage of +24V SMCJ18A-TR diodes are strongly recommended. The out-coming structure has a standoff voltage of 36V and a breakdown voltage of 40V.

5.2.2 Input Capacitor Block.

An electrolytic capacitor (C3) must be placed immediately after the surge suppression block. This has to be a low ESR capacitor, it would be even better to place on the other side of the PCB, as close as possible to the electrolytic (ideally just underneath), one or more low ESR, SMD ceramic capacitor (C4; suggested vale: 100nF).

The size of the electrolytic capacitor has to be chosen depending on the slope of the output current, the impedance of the complex power supply and cables, as well as the maximum allowed voltage drop across the device. Typically in an industrial environment the load will be partly resistive (Rload) and partly inductive (Lload). At the turn on of one channel the worst case is the pure resistive one, since it has the highest *di/dt*. Due to their inductance the supply cables will hinder the delivery of the current, which will have to be supplied by the electrolytic capacitor. The local supply voltage will then drop according to the dimension of the electrolytic capacitor. To simplify it can be presumed that in case of pure resistive load (fastest transition) the supply lines have very high impedance at the turn on, thus delivering no current at all till the DC condition has been reached. Of course this assumption leads to an excess estimation of the capacitor value, the real drop across the capacitor will be in reality less than the expected one.

Figure 16: IPS Switching a Typical Load Through Long Power Supply Cables



Generally, considering an electrolytic capacitor of value *Cin* and parasitic serial resistance *ESR*, $R_{load}=48\text{ohm}$, $L_{load}=0\text{H}$, $L_{cables}=\infty$, $V_{cc}=24\text{V}$ it will be:

$$\frac{s \cdot C_{in} \cdot V_s}{s \cdot ESR \cdot C_{in} + 1} = -\frac{m}{R_{load}} \cdot t \quad (eq3.1)$$

where *m* is the *dv/dt* of the output voltage

$$\Delta V_s = \frac{m}{R_{load}} \cdot \left(\frac{T_{turnon}^2}{2 \cdot C_{in}} + ESR \cdot T_{turnon} \right) \quad (eq3.2)$$

where $T_{turnon} = V_{cc}/m$.

ST is manufacturing IPS with controlled output voltage slope, in order to minimize the electrical pollution of the bus. As an example the VN340, according to the data sheet, has a typical dV_{out}/dt of about 0.25V/ μ sec (@ $R_{load}=48\text{ohm}$, $V_{cc}=24\text{V}$).

Once given the allowed maximum voltage drop, it is then possible to calculate the needed capacitance value:

$$C = \frac{V_{cc}^2}{2 \cdot m \cdot (R_{load} \cdot \Delta V_s - ESR \cdot V_{cc})} = 25\mu\text{F}/\text{channel}$$

if $\Delta V_s=1\text{V}$.

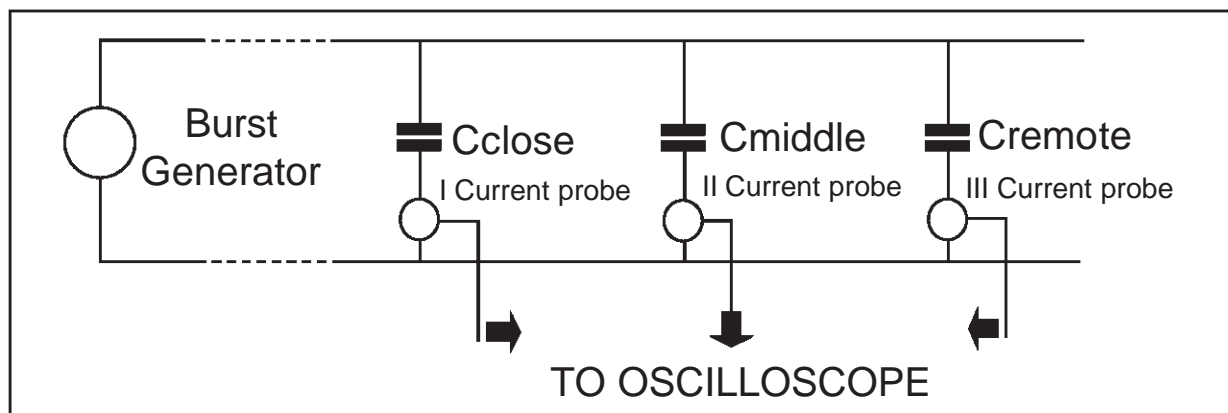
For an 8 bit module it is then suggested to have a 220 μ F.

The input capacitor block plays a major role in electric fast transients filtering as well.

Due to the harmonic distribution, capacitive paths are the preferred ones for such a disturbance. Typically it is observed that 1nF are negligible impedances to the single burst pulse. In addition, the energetic content is very low. Consequently even a very fast TRANSIL will act on the burst thanks to its parasitic capacitance (normally in the order of 1nF). A good approach in filter EFT on V_{cc} lines would then be to place a capacitor immediately after the input surge suppression block. Basically it will be the most efficient suppressor of these fast electrical transients. Due to power spectrum distribution of EFT this capacitor could even just be in the magnitude order of 10nF.

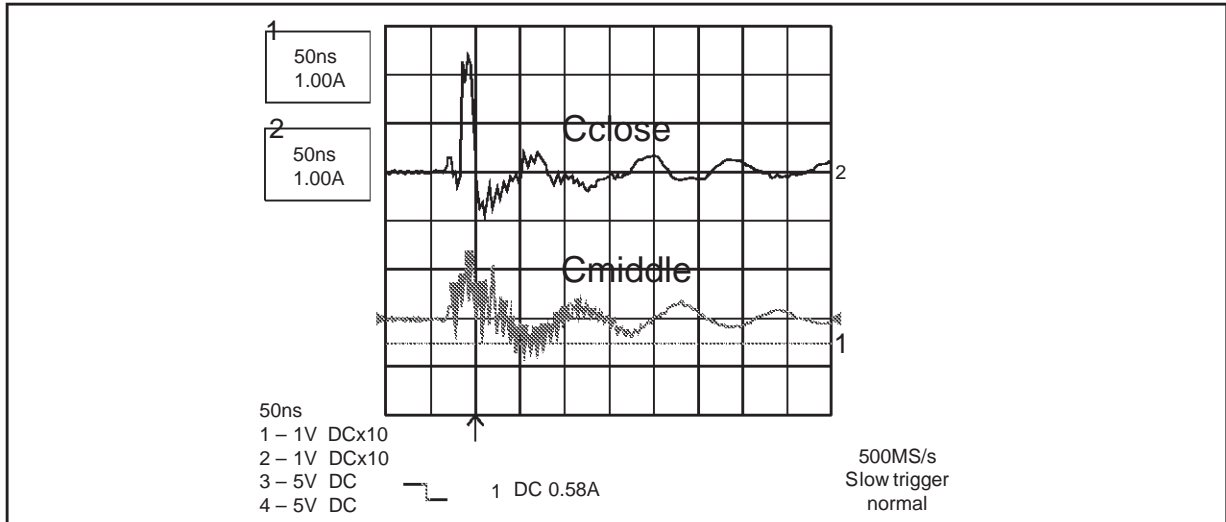
LABORATORY EXAMPLE: To better understand the difference between schematic and PCB when speaking about EFT it is possible to perform a simple "play". Just build a ladder with 3 identical ceramic capacitors and 2 metal wires. Put the capacitors as close as possible to each other, just providing the required space to measure with a current probe the current flowing in each one of them.

Figure 17: Ladder Test Network



When applying an EFT burst at one end of the ladder it is then noticed that the capacitors are, in reality, not parallel to each other. The current sharing is very different from capacitor to capacitor: the closer the EFT generator, the more overstressed the capacitor will be.

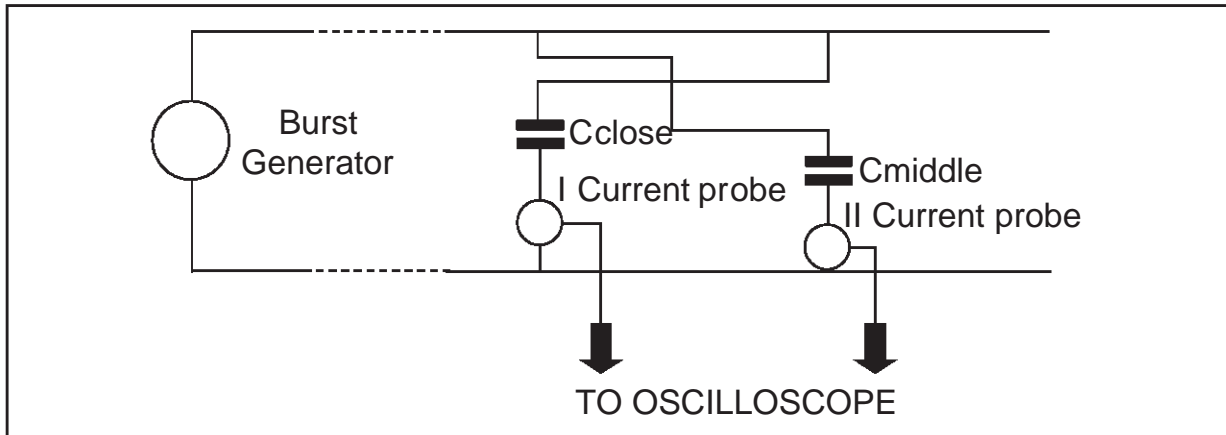
Figure18: Current Sharing in C_{close} and C_{middle} (unbalanced layout)



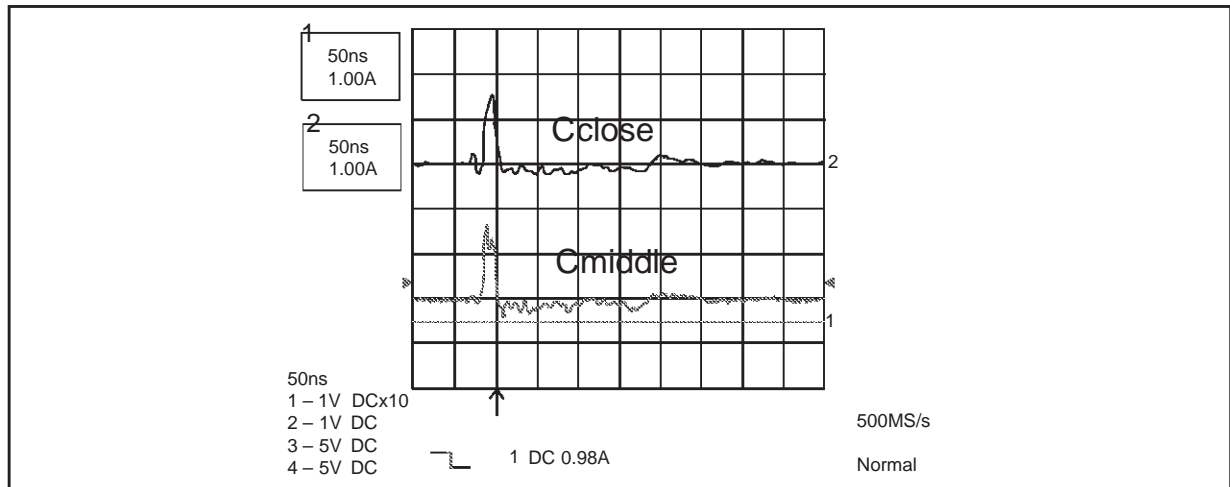
Then the other capacitors placed in parallel to the first one are not effective.

It is basically due to the “unbalanced layout” designed: it is now possible to cross the capacitors in order to balance the layout providing almost the same path impedance to each capacitor.

Figure 19: “Balanced” Ladder Test Circuit



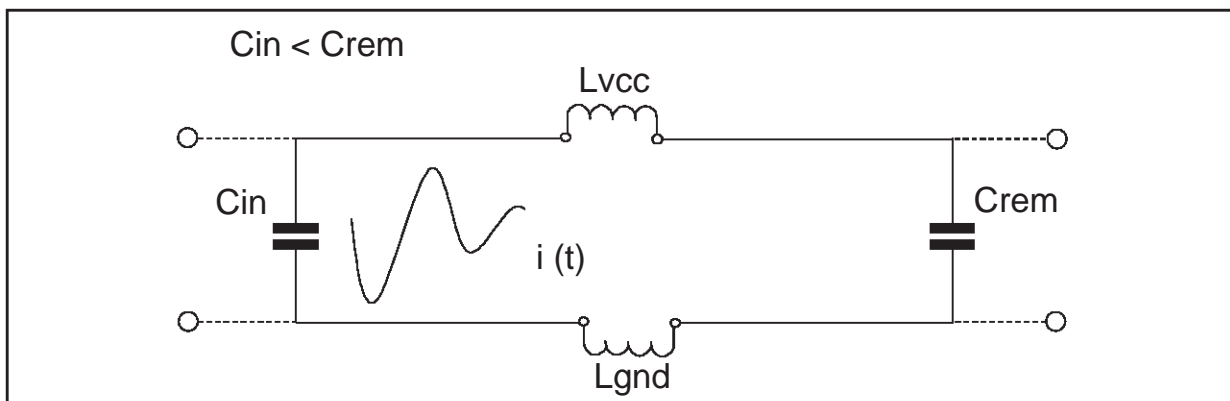
In this way the current is equally shared, the filtered voltage is lower and no capacitor is overstressed.

Figure 20: Current Sharing Between C_{close} and C_{middle} (balanced layout)

It is then very important to notice that it is not just a question whether to place a capacitor or not, but how to place it in order to obtain the highest possible efficacy.

The biggest constraint is the capacitor's ESR, which is surely giving the dominant contribution to the clamping voltage for big values of capacitance. Therefore with a low ESR input capacitor it is expected to have an efficient clamping of the burst. However this is still far to ensure a safe environment for the devices on board. If a bigger capacitor than the input one is present a high frequency oscillation (typically in the range of 1 to 10MHz, with peak to peak current up to 4A) will arise on V_{CC} and ground lines.

Figure 21: Induced Oscillations Layout



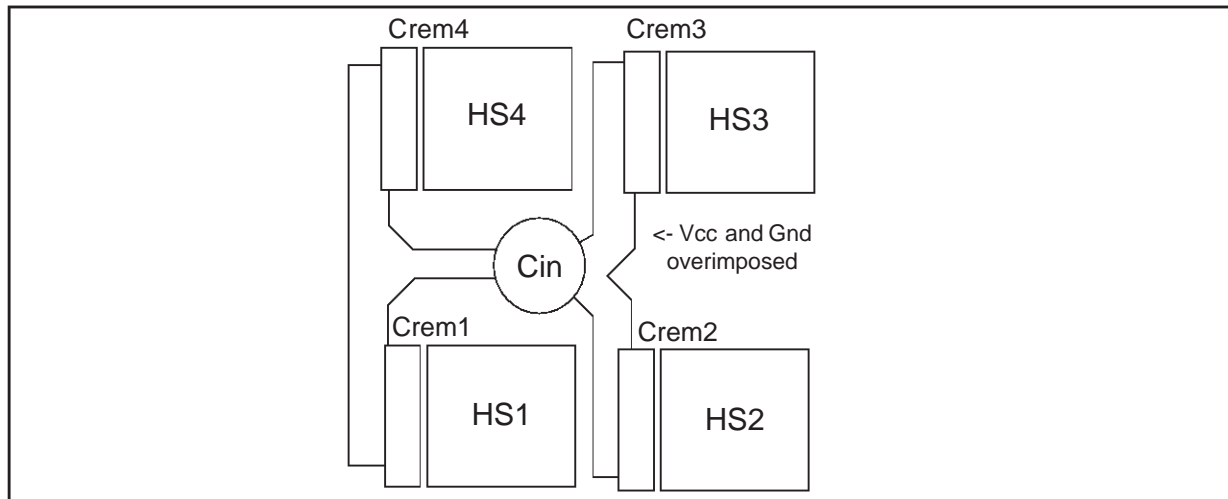
This phenomenon can be very dangerous for the connected devices and has to be avoided. The oscillation frequency is fixed by the capacitors' value and by the parasitic inductance value of the path between these two capacitors. This oscillation is just lightly smoothed because of low resistive value of the lines between the capacitors, then it can persist for a relatively long time.

Consequently, stray inductances have to be minimized, and the input capacitor block should immediately follow the surge suppression block. This capacitor should be much bigger than the others distributed on boards as well in order to avoid further oscillations.

5.3 Repeated Structures.

In multi channel high side driver modules symmetry and balance of the structure are necessary to ensure the same condition of operation for all of the electronic switches. The layout should then provide equivalent connection lengths for all of the channels.

Figure 22: Symmetrical Distribution of IPS



Moreover, this allows using a single electrolytic capacitor for one complete array of switches. As we know this can even help in EFT filtering, in case the electrolytic has a very low ESR and it has a proper size and proper location on board. In repeated structures some redundancy is anyway needed.

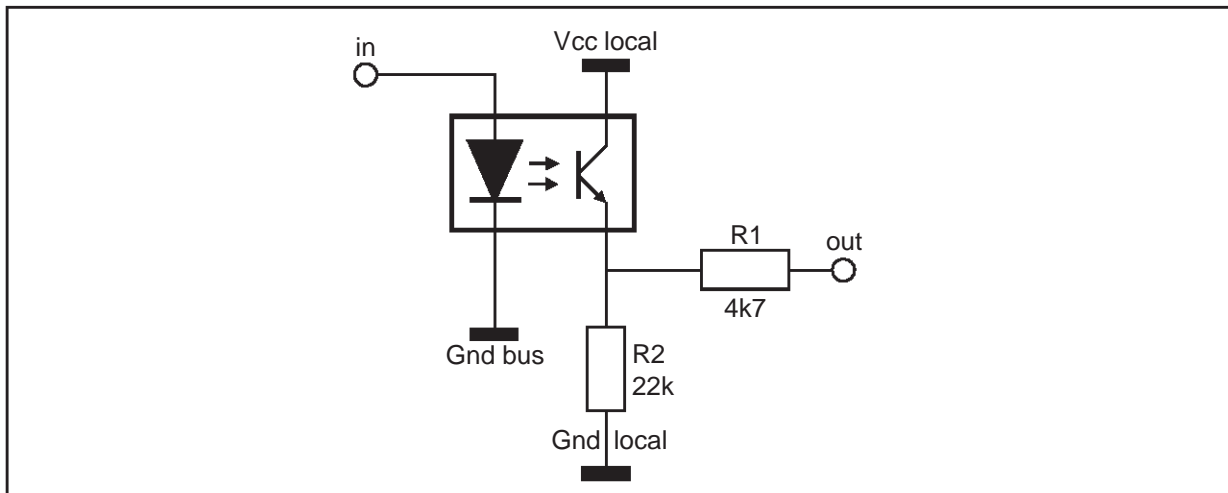
Each high side driver (HSX in figure 22) should have a ceramic SMD, low ESR capacitor (Crem in figure 22) as close as possible to its ground and supply pins. The size should be variable in the range of 10 to 68nF for single channel chip and 100 to 220nF for quad channel chips.

5.4 Signal Inputs / Diagnostic Outputs.

In the industrial field there is usually the need for electric isolation of the signal I/Os.

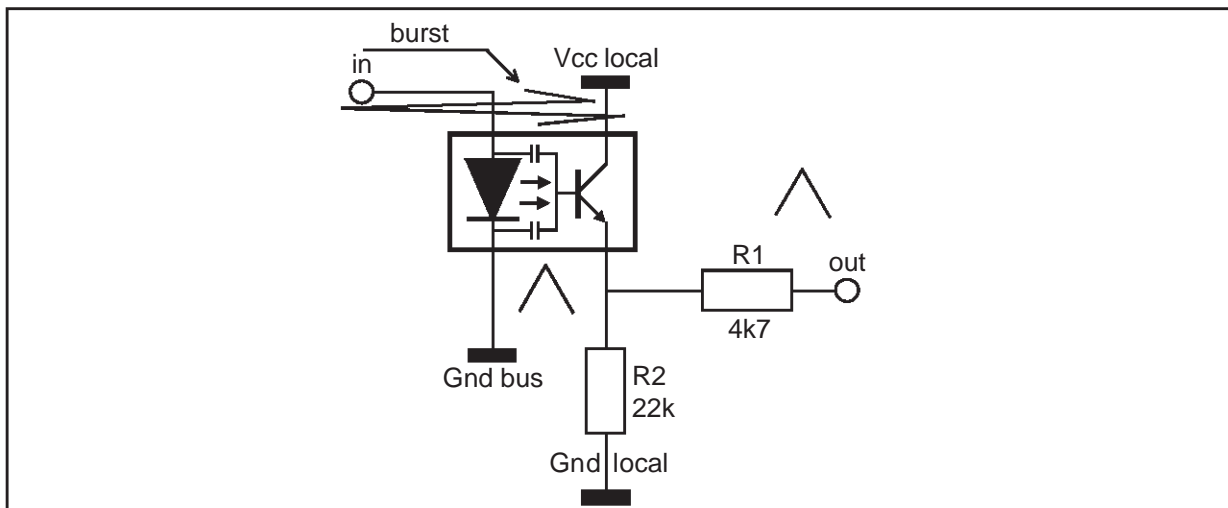
Optocouplers are widely used and multi-channel optocouplers represent a very attractive solution. The use of multi-channel optocouplers can be problematic particularly in terms of immunity to EFT.

Figure 23: Typical Isolated Input



EFT can result in switching shortly on one or more of the optocoupler's channels, the corresponding output signal is consequently altered. This can lower the category of immunity of the EUT from category 1 (normal performance) to category 2 (temporary degradation or loss of function or performance): one (or more) high side(s) can switch on for a short time due to alteration of the input signal, or the diagnostic can display a commutation then being misunderstood from the controller section. The phenomenon can be described in this way: the primary and secondary sides of the optocouplers are isolated but they still have parasitic capacitance "bonding" one to each other. This parasitic capacitance can result in injecting current through the base emitter junction of the phototransistor when one half of the optocoupler is "tight" by fast voltage transients with respect to the other.

Figure 24: Burst Pulses Affecting One Input

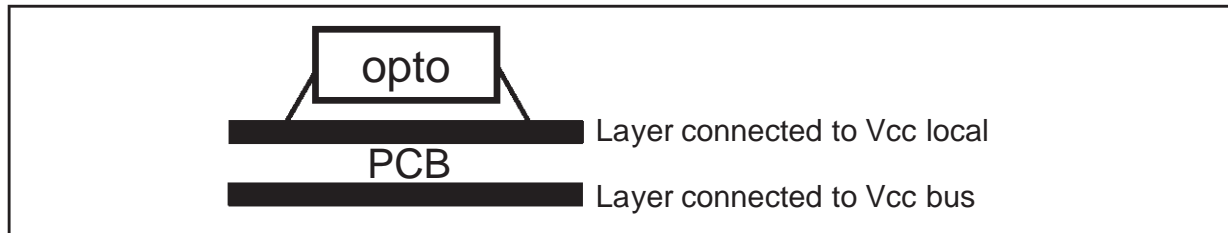


If the optocoupler is used in an emitter follower configuration, like it usually happens in this kind of applications, it is possible to induce a high emitter voltage signal by applying EFT even opening the collector termination. An efficient way to prevent this induced turn on is to provide a conducting plane on the bottom layer of the PCB, under the optocoupler, connected (for emitter follower configuration) to the

collector voltage.

Optocouplers dedicated to diagnostic functions result to be the most sensitive, since the efficiency of this parasitic process is higher when the half of the optocoupler containing the LED is directly perturbed and tied with respect to the phototransistor. In this case a second additional conductive plane (on the remaining free side of the PCB under the optocoupler) should be provided and connected to the anode voltage.

Figure 25: Cross Section of the PCB



Moreover multi channel optocouplers should be used in “unidirectional” way: all of the channels’ transistors must face either the bus or the module to improve the rejection of disturbances.

If several multi channel optocouplers have to be used, the best results are achieved using for each optocoupler separated supply lines directly coming from the integrated circuit they are driving / are driven by.

5.5 Power Outputs.

Power outputs are heavily perturbed as well. The common ground cable of the different loads should directly be connected to the input capacitor block. Star connection is recommended in order to avoid coupling of excess noise on other lines.

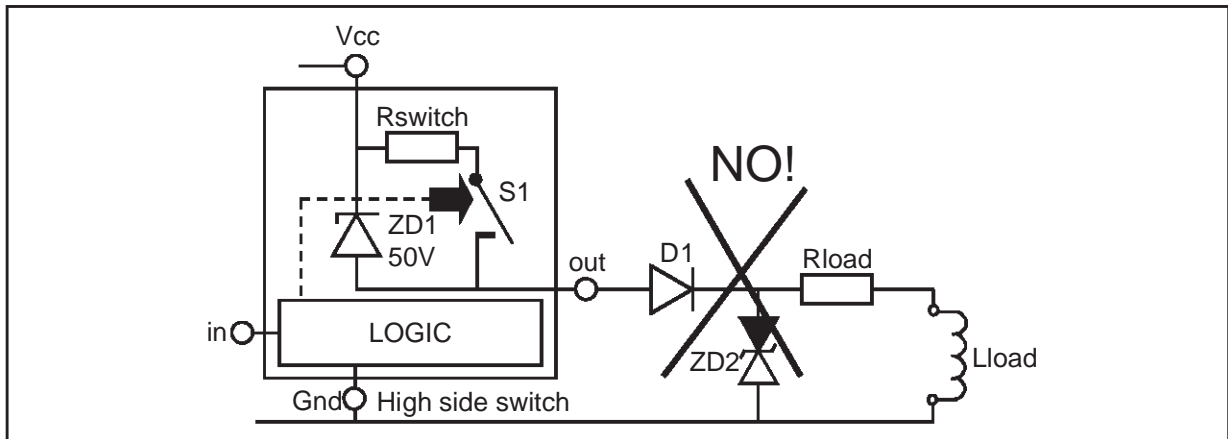
For the **IEC801-6** it will normally be useful to place a **10nF(or bigger), low ESR, ceramic capacitor** on the outputs, being very careful regarding the layout of the connection to ground, avoiding to disturb the IC’s ground.

5.6 Power Outputs (2) – Surges on Outputs.

Negative surge on power outputs during switching.

When the application must be protected from surges on power outputs, due to the high energy of the pulse (capable to deliver in theory up to $2000V / 42\Omega = 48A$, in the worst case) it is mandatory to adopt external protections. One channel of a typical application with fully protected power outputs can be simplified like in the picture below:

Figure 26: Wrong Approach to Power Output Protection



ZD2 is an external TRANSIL, for example SM6T33CA, with a typical breakdown voltage of 33V. D1 has to protect the device output from positive surges ensuring that ZD2 is absorbing the energy and hindering the path (through the device) towards Vcc.

The high side driver, connected between the output and Vcc, has an internal zener diode (c.a. 50V breakdown) for fast demagnetization of inductive load. This means that for supply voltage above about $(50-33)=17\text{V}$ it will be the internal zener diode to bring the current in the inductive load down to zero. As an example for $V_{cc}=24\text{V}$, ZD2 would like to clamp the output voltage at -33V , but it will never see that voltage since the internal zener is clamping at $(24-50)=-26\text{V}$.

Why should this be a problem?

If the driver is either on, off or switching and a positive surge is applied nothing bad can happen since the D1 will be reversely polarized and ZD2 will clamp and absorb the energy.

But if the surge pulse is negative and the driver is switching off, with supply voltages higher than 17V, the internal ZD1 will be conducting and it will give to ZD2 any chance to enter into conduction and absorb the energy surge. Therefore ZD1 will have to take all of the current and typically it will be destroyed because of power dissipation.

Why negative surges are not destructive in others condition?

If the high side switch is simply either off or on (as well as switching from off to on), a negative surge will not affect the device.

This is due to several reasons: forward peak turn on voltage of ZD1 and D1 (higher than for ZD2, that basically has better dynamic performances) and relatively short duration of the surge itself, compared to the response of ZD1+D1.

How is it possible to verify this statement?

This test can be done: lower Vcc down to 10 or 12 V. In this case the external diode will be conducting during turn off of the high side driver. Applying surges, no failure should happen, whatever the status of the IC.

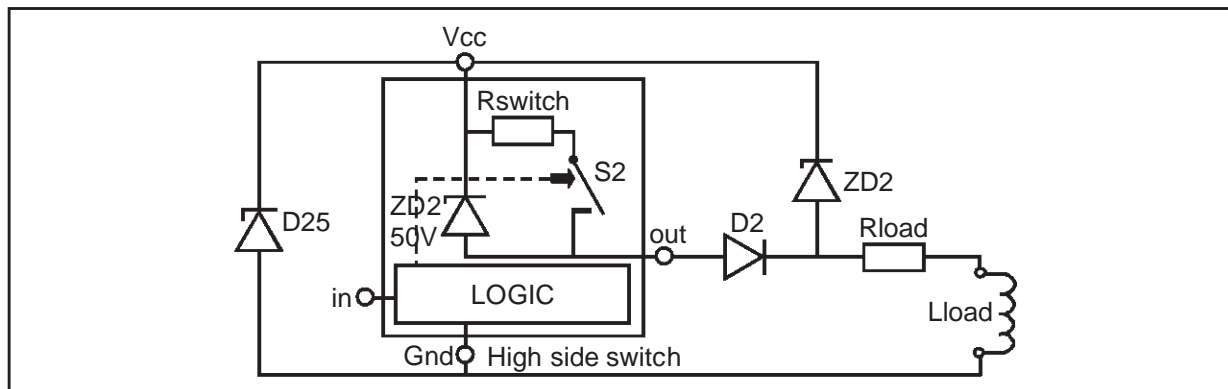
How to solve the problem in reality?

During turn off we need to recover the energy charged in the inductor externally to the IC, in order to prevent the occurrence of one surge when ZD1 is conducting. Different solutions can be implemented.

The easiest case would be: fast demagnetization not needed, then ZD2 could be substituted with a unidirectional Transil. Otherwise, two different breakdown voltages would be needed, positive and negative. The positive should remain above 30V, being the highest allowed supply voltage and the negative should be smaller (in absolute value) than $(V_{ccmax}-50)=c.a.-20V$. But this is expensive.

The third and best solution is to duplicate externally the internal structure. This means ZD2 should be placed between output and V_{cc} instead of between output and Gnd. In this case the selected breakdown voltage could be 45V.

Figure 27: Correct Approach to Power Output Protection



Advantages of this solution:

- ZD2 can be unidirectional;
- it is always sure that during the turn off it will recover the energy instead of the internal zener, whatever the supply voltage is.

Disadvantages:

- bit higher power dissipation in ZD2 in case of negative surge, compared to the demagnetization to ground topology;
- D25 (Unidirectional protection transil between Gnd and Vcc) is working as well in case of positive surge on output, while before it was not affected.

6. REVERSE BATTERY CONNECTION.

Depending on the current capability of the power supply and the duration of the reversed battery connection, the two serial transils input structure (figure 14) could however be injured. In this case bi-directional transils can be used but then most probably the reverse supply voltage across the device would exceed its maximum rating (which is $-4V$ in case of the VN340). The reverse current through the IC must be limited by the insertion of appropriate impedance between the ground pin of the device and the supply ground (this to limit the power losses during normal operation: just the biasing current will be flowing!). For the VN340 suggested impedance to be inserted is a Schottky diode paralleled to a 1kOhm resistor. Should the load be simply resistive, the impedance can be a 150Ohm resistor.

Another possible connection fault is an output pin connected to the high supply voltage and V_{CC} pin shorted to the supply ground. In this case a high reverse current will flow through the body diode of the output Power MOSFET. If this current is exceeding the maximum rating specified in the datasheet, this will certainly result in permanent injury of the IC.

To avoid this a serial diode can be placed on the output towards the load like D2 in figure 27.

7. TWO PRACTICAL EXAMPLES (VN800PT, L6377).

Two application examples are reported. The corresponding layout solutions can always be imported and applied in any high side driver board design. The two boards can withstand:

IEC801-4 Class1 Level 3 on supply lines; Class 1 Level 4 on I/Os

IEC801-5 Class1 Level 3 on supply lines

IEC801-6 Class1 Level 2

7.1 VN800PT - 8 Channel Application Reference Board.

Figure 28: Block Diagram of the VN800PT

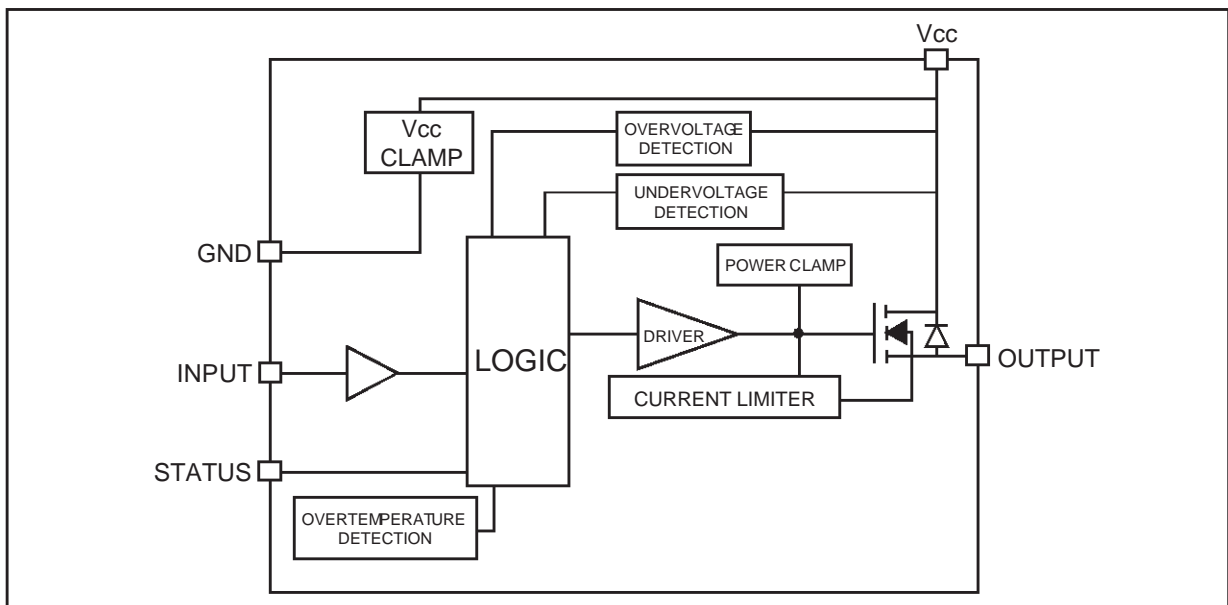


Table 8: VN800PT Main Characteristics

<ul style="list-style-type: none"> - Output current: 0.7A - CMOS compatible input - Thermal shutdown - Current limitation - $R_{DS(on)}=135m\Omega$ 	<ul style="list-style-type: none"> - Shorted load protection - Under voltage and over voltage shutdown - Protection against loss of ground - Very low standby current (20μA max in off state; 3.5mA max in on state)
---	---

The proposed application is an 8-bit module, with just 2 diagnostic outputs. To be observed the layout of the supply and ground lines must allow the safe use of very light filtering despite high immunity level achieved. Particular care was taken for the signal outputs and inputs in order to minimize the impact of disturbances and enhance immunity (shielding layers for the multi channel optocouplers).

Figure 29: Application Schematic of VN800PT - 8 Channel Module

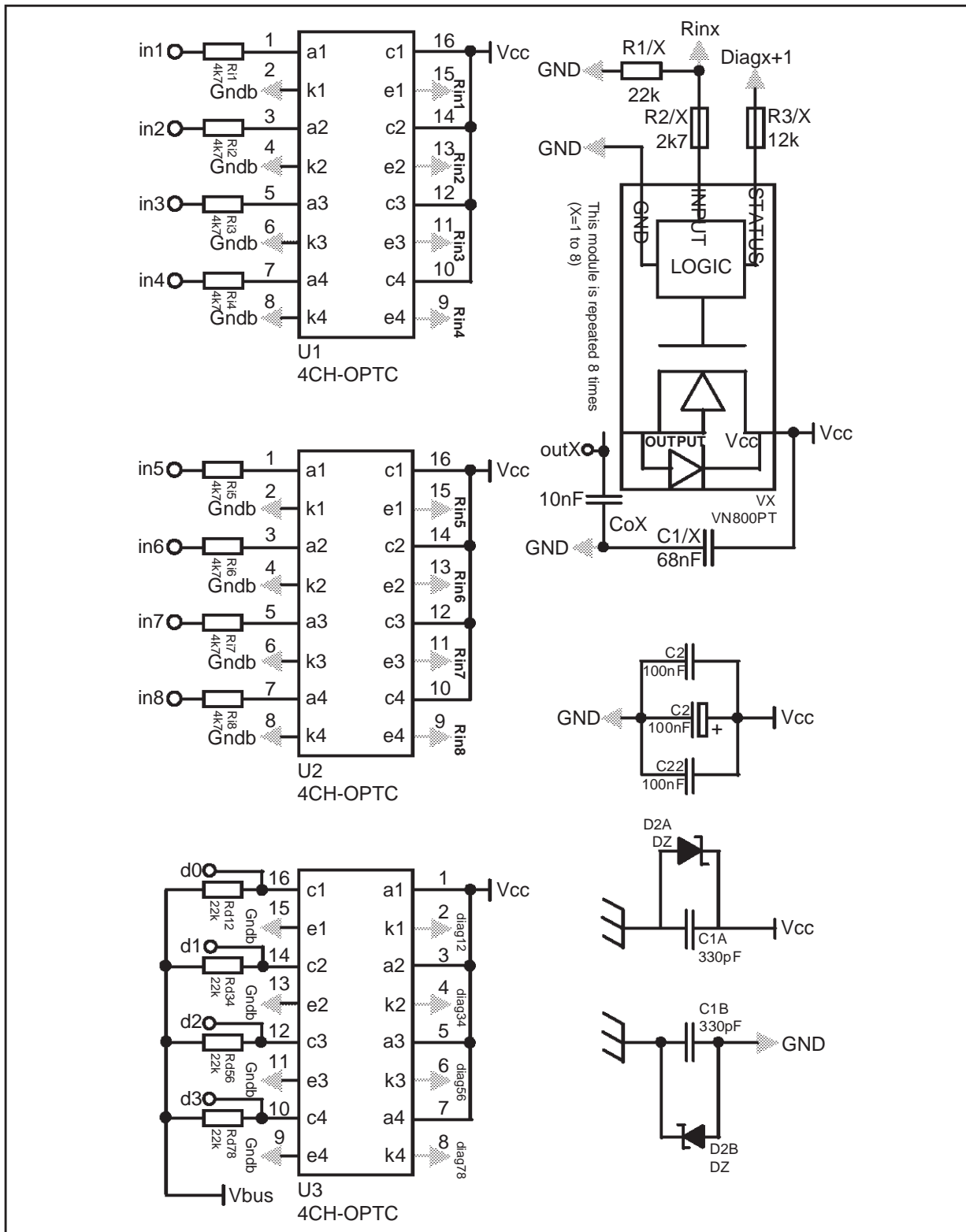


Figure 30: The Top Layer of VN800PT - 8 Channel

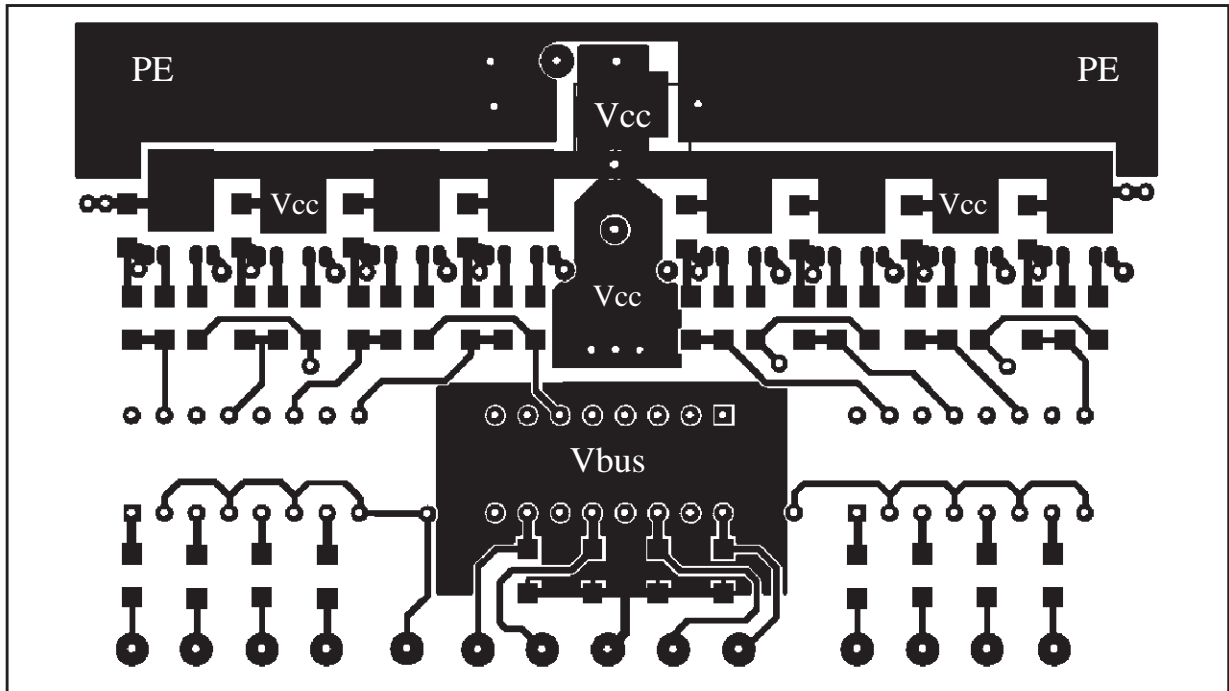


Figure 31: The Bottom Layer (Not Mirrored) of VN800PT - 8 Channel

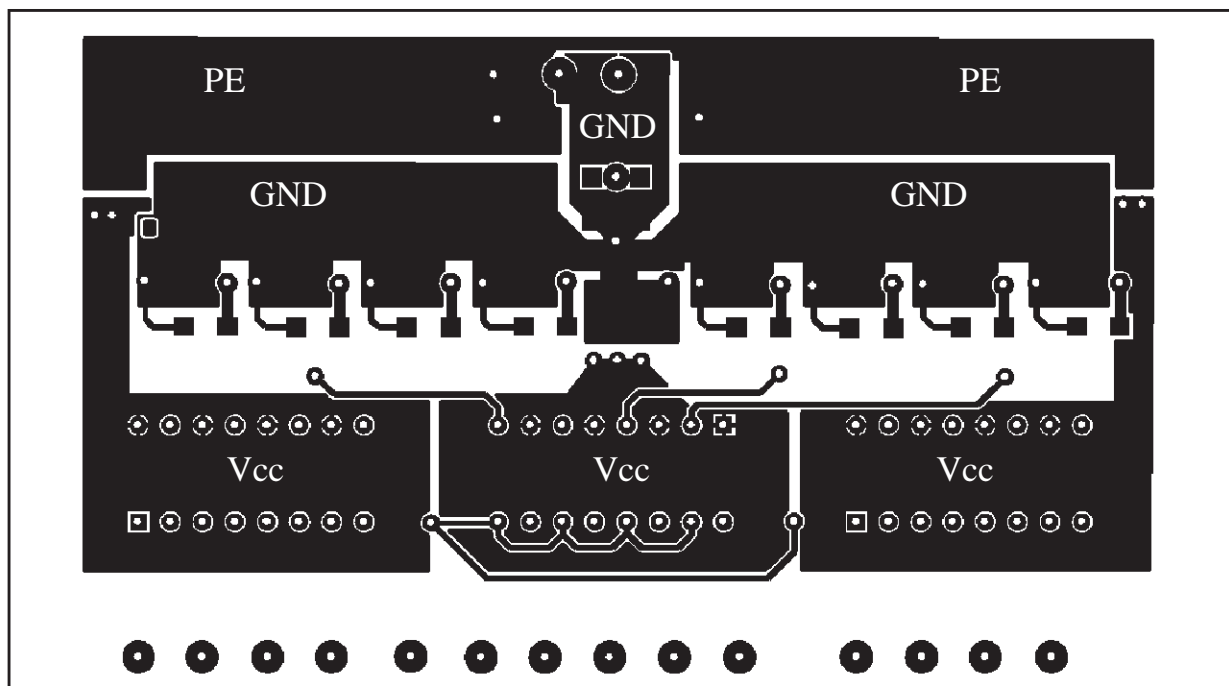


Figure 32: The Top Paste Layer of VN800PT - 8 Channel

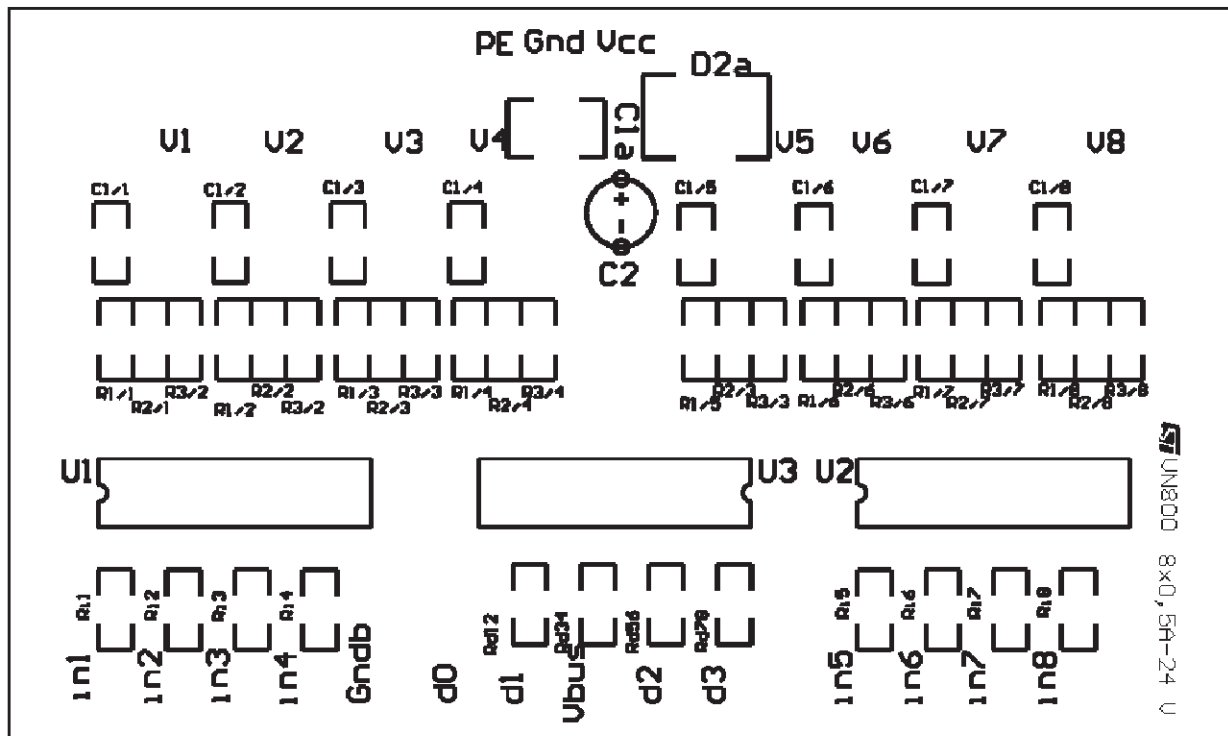
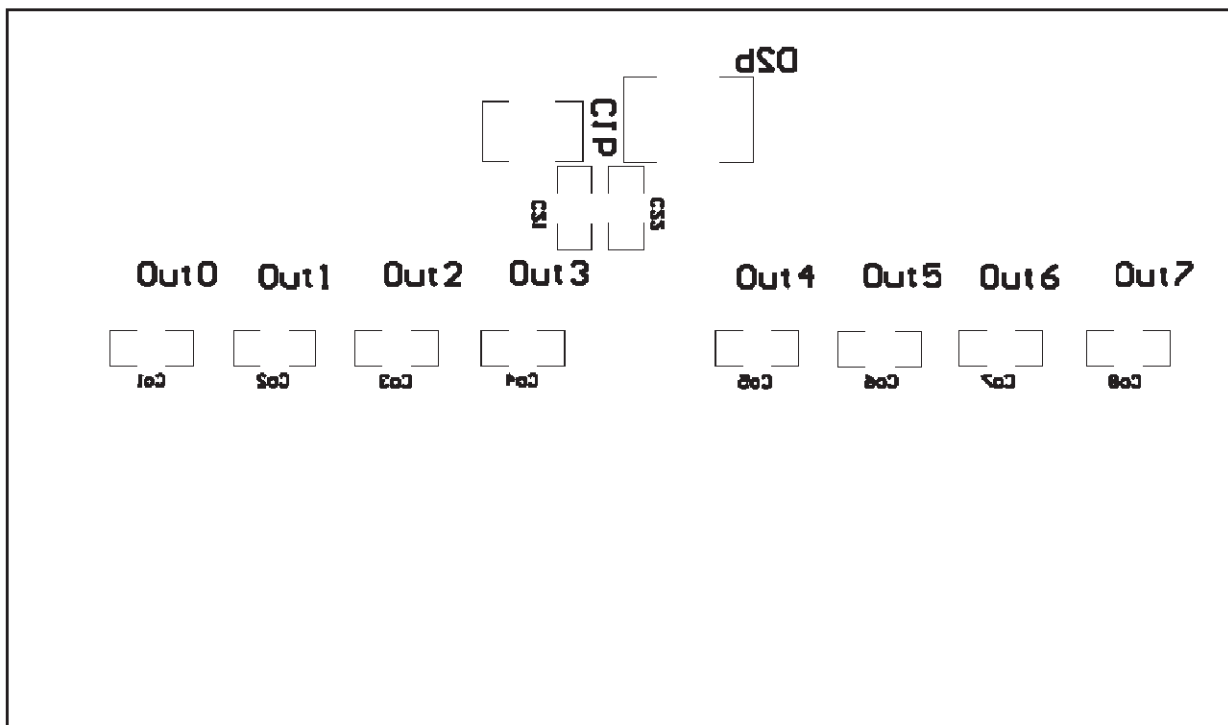


Figure 33: The Bottom Paste Layer of VN800PT - 8 Channel



7.2 L6377 - Dual Channel Application Reference Board.

Figure 34: L6377 Block Diagram

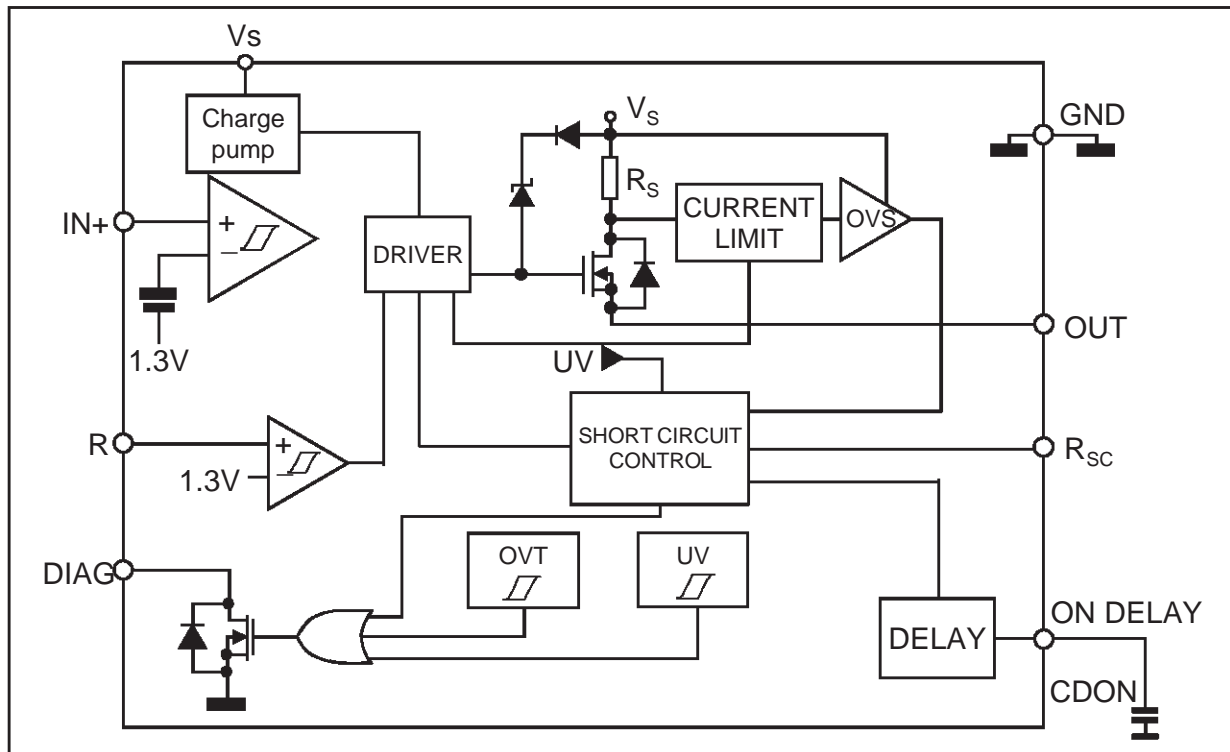


Table 9: L6377 Main Characteristics

<ul style="list-style-type: none"> - 0.5 Output current - Externally programmable current limit - Non dissipative over-current protection - Thermal shutdown - Under voltage lockout - $R_{DSonmax} = 640m\Omega$ (typ. @ $T_j=125^\circ C$) 	<ul style="list-style-type: none"> - Diagnostic output for over-voltage, over temperature and over-current - Asynchronous reset input - Settable delay for over-current diagnostic - Open ground protection - Low quiescent current (800mA in off state, 1.6mA in on state)
--	--

The proposed application is a 2-bit module with just 1 diagnostic output. To be observed the layout of the supply and ground lines must allow the safe use of very light filtering despite high immunity level achieved. Particular care was taken for the signal outputs and inputs in order to minimize the impact of disturbances and enhance immunity (shielding layers for the optocouplers).

Figure 35: Application Scheme of L6337 - Dual Channel

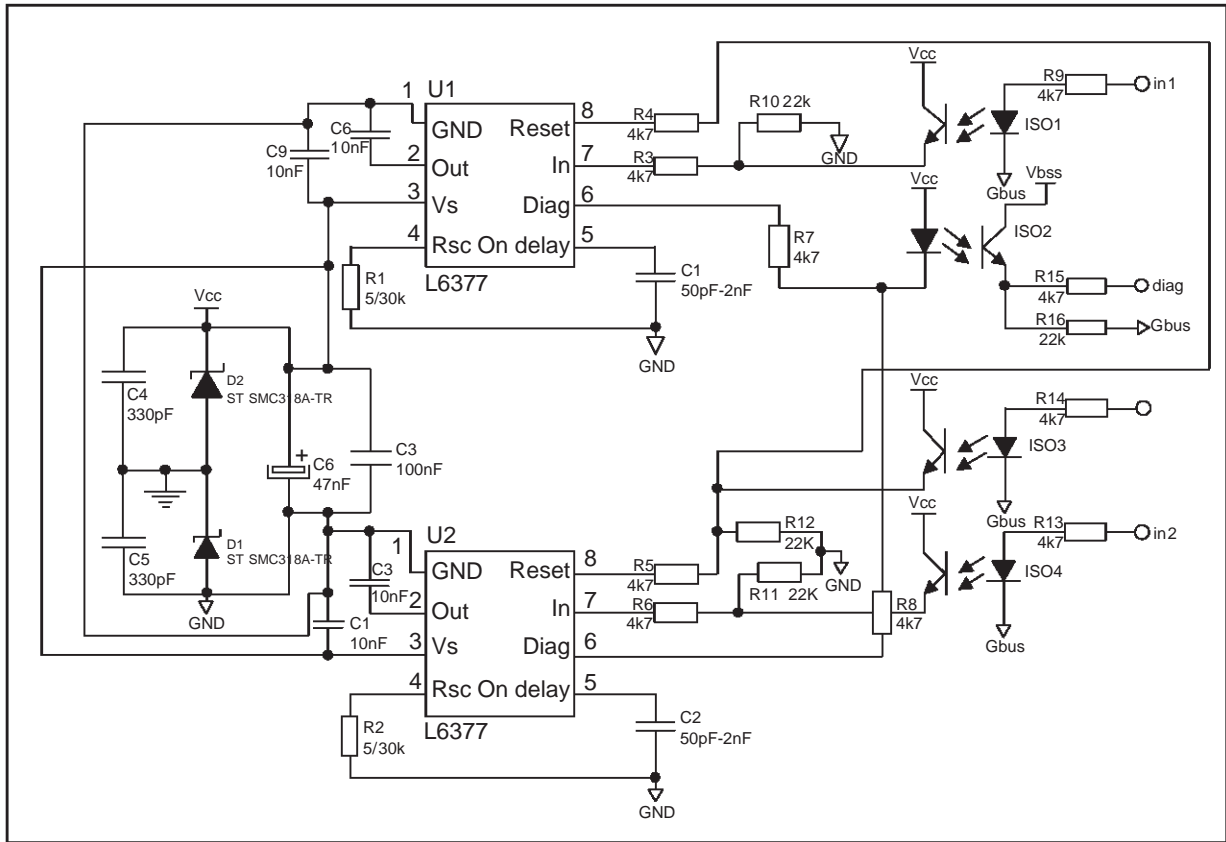


Figure 36: The Top Layer of L6337 - Dual Channel

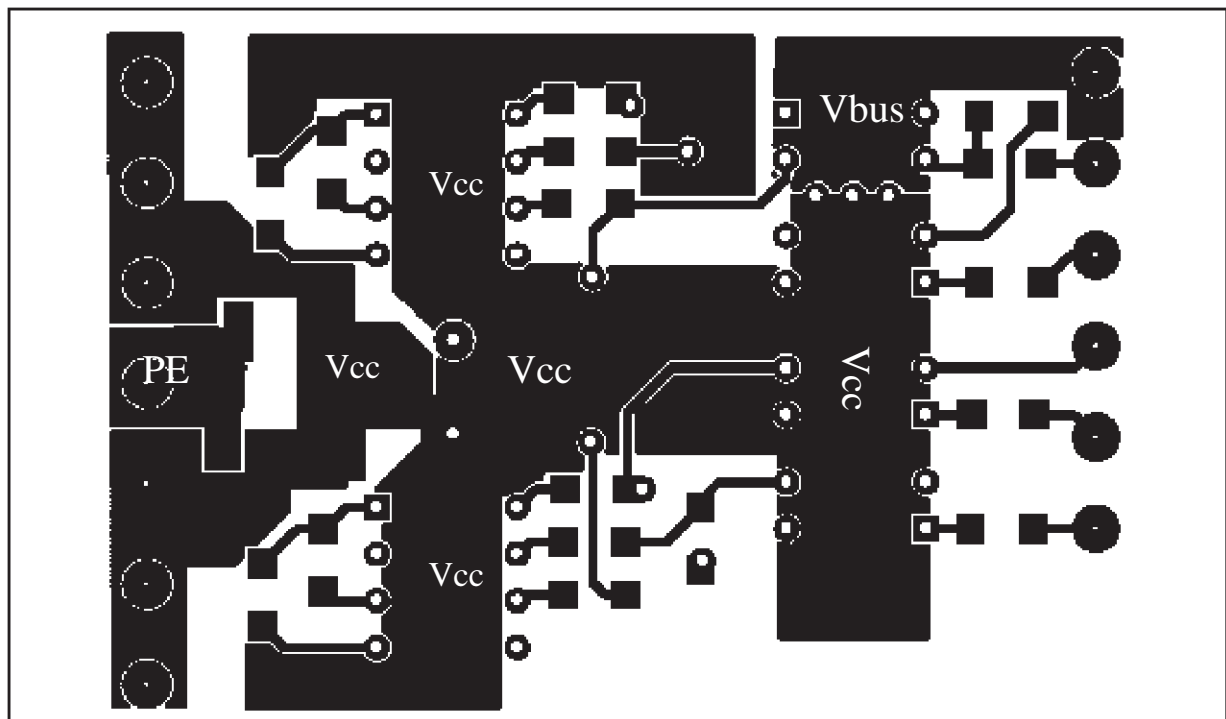


Figure 37: Components Disposition on Upper Side of L6377 - Dual Channel

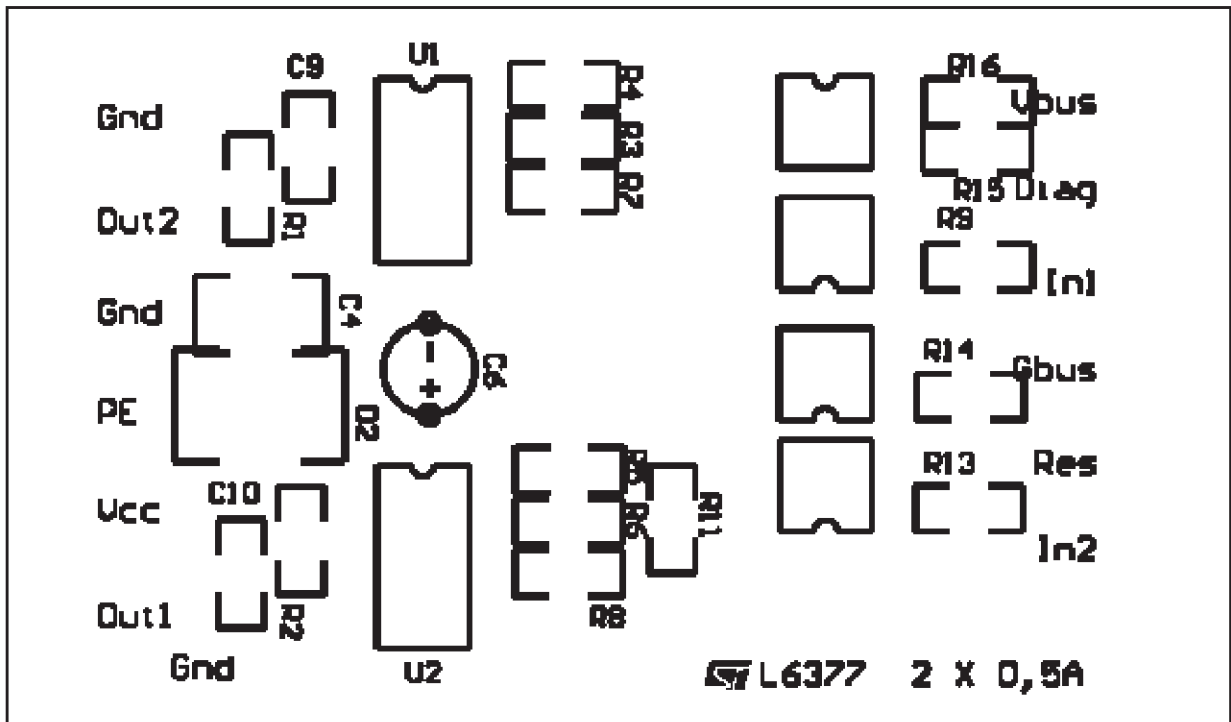


Figure 38: The Bottom Layer of L6377 - Dual Channel

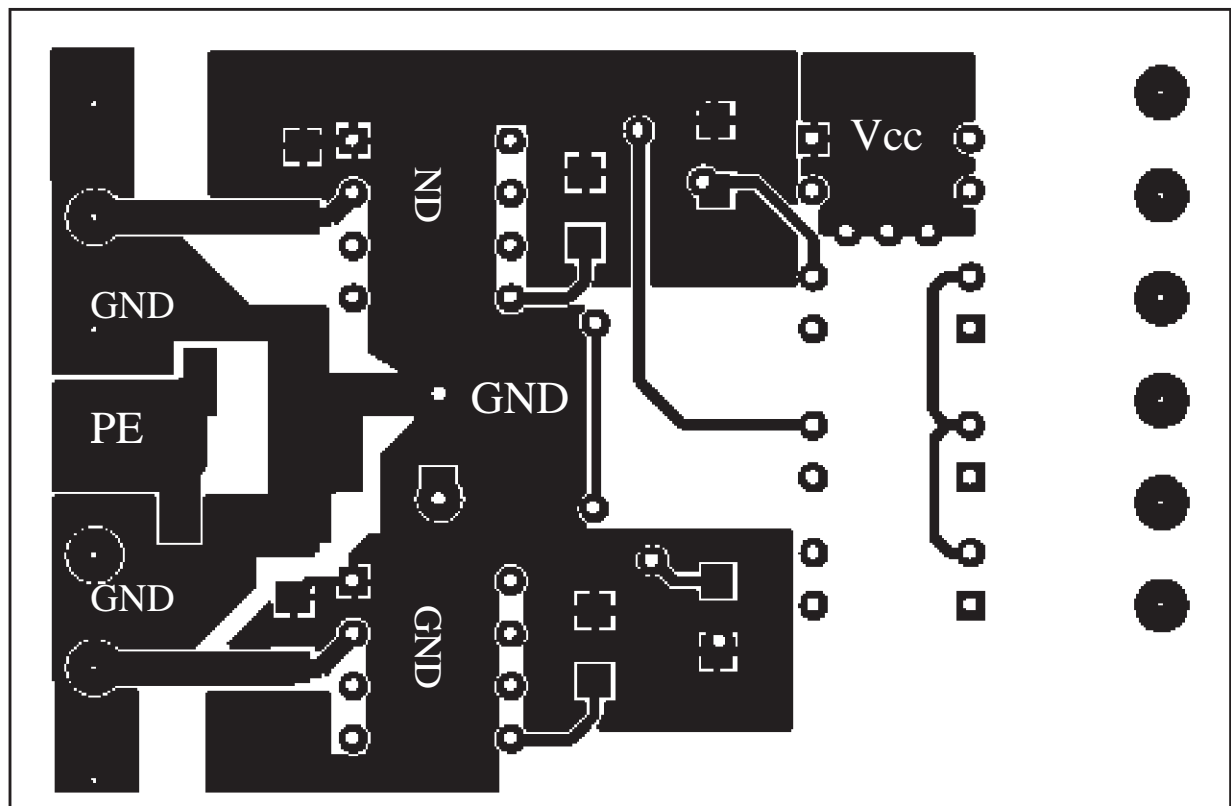
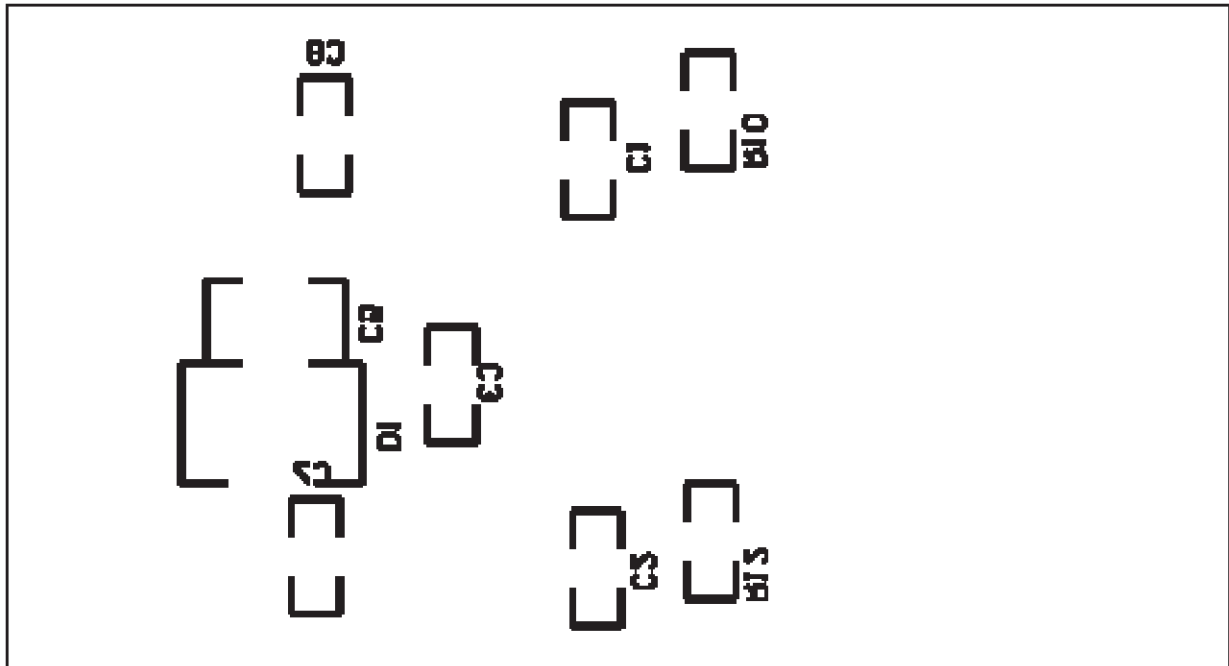


Figure 39: Components Disposition on Bottom Side of L6377 - Dual Channel



7. CONCLUSION

The schematic is often very different from our physical reality. The board layout should be made in such a way as to minimize this gap, bringing reality close to idealizations. It is not just electrical connections, it is how to handle power, noise and immunity.

Inductive switching, thermal analysis and general considerations about I.P.S. are based on studies and evaluation by: G.Commandatore, P.Laupheimer, A.Pavlin and F.Pulvirenti.

For complete technical data documentation about the specific products please refer to the official datasheet.

All of the measurements and considerations on electromagnetic immunity were performed in Ottobrunn, Germany, inside the industrial application laboratory.

Test equipment as following:

LeCroy LC 334 AM 500MHz Oscilloscope;
LeCroy AP015 Current Probe;
Keytek CE Master EMC Immunity System;
PMM 3000 Signal Generator;
PMM 6000N Power Amplifier;
FCC P/N F-33-1 Feedback Current Probe;
FCC F120-9A Bulk Current Injection Probe;
PS 2403D 0/40 V Laboratory Power Supply;
24V Battery.

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