# AN1330
# APPLICATION NOTE

## DESIGNING WITH L5970D, 1A HIGH EFFICIENCY DC/DC CONVERTER

**by Massimiliano Merisio**

### L5970D INTRODUCTION

The L5970D is a step down monolithic power switching regulator capable to deliver up to 1A at output voltages from 1.235V to 35V. The operating input voltage ranges from 4.4V to 36V. It is realized in BCDV technology and the power switching element is realised by a P-Channel D-MOS transistor. It doesn't require a bootstrap capacitor, and the duty cycle can range up to 100%.

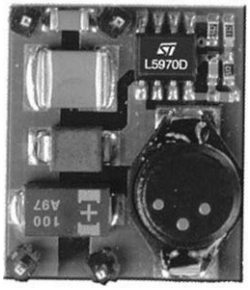
An internal oscillator fixes the switching frequency at 250KHz. This minimizes the LC output filter.

Synchronization pin is available in the case higher frequency (up to 500KHz) is requested.

Pulse by pulse and frequency foldback overcurrent protections offer an effective short circuit protection.

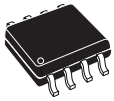
Other features are voltage feed forward, protection against feedback disconnection, inhibit and thermal shutdown.

**Figure 1. Demoboard**



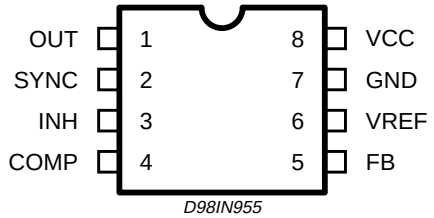

**L5970D (SO8) Board Dimensions: 23 x 20 mm**

**Figure 2. Package**



**SO8**

**Figure 3. Pins connection**



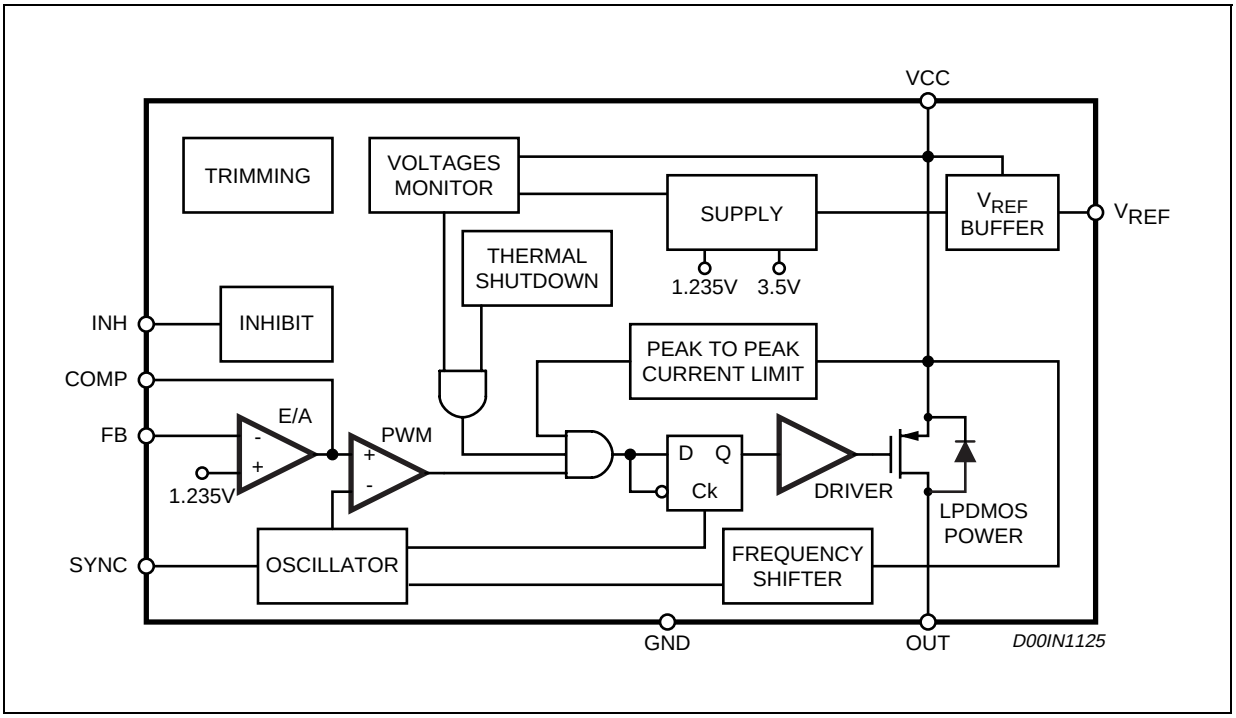

*D98IN955*

## PINS FUNCTIONS

| N. | Name | Description |
|---|---|---|
| 1 | OUT | Regulator Output. |
| 2 | SYNC | Master/Slave Synchronization. When it is open, a signal synchronous with the turn-off of the internal power is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal.<br>Connecting together the SYNC pin of two devices, the one with the higher frequency works as master and the other one, works as slave. |
| 3 | INH | A logical signal (active high) disables the device. With IHN higher than 2.2V the device is OFF and with INH lower than 0.8V, the device is ON.<br>If INH is not used the pin must be grounded. When it is open, an internal pull-up disables the device. |
| 4 | COMP | E/A output to be used for frequency compensation. |
| 5 | FB | Stepdown feedback input. Connecting the output voltage directly to this pin results in an output voltage of 1.235V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7K). |
| 6 | $V_{REF}$ | Reference voltage of 3.3V. No filter capacitor is needed to stability. |
| 7 | GND | Ground. |
| 8 | $V_{CC}$ | Unregulated DC input voltage. |

## BLOCK DIAGRAM

**Figure 4. Block Diagram**



## FUNCTIONAL DESCRIPTION

The main internal blocks are shown in Fig. 4, where is reported the device block diagram. They are:

- A voltage regulator that supplies the internal circuitry. From this regulator, a 3.3V reference voltage is externally available.
- A voltage monitor circuit that checks the input and internal voltages.
- A fully integrated sawtooth oscillator whose frequency is 250KHz ±15%, including also the voltage feed forward function and an input/output synchronization pin.
- Two embedded current limitations circuitries which control the current that flows through the power switch. The Pulse by Pulse Current Limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the Frequency Shifter reduces the switching frequency in order to strongly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- An high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation.
- A circuit to realize the thermal protection function.

## POWER SUPPLY &VOLTAGE REFERENCE

The internal regulator circuit (shown in Figure 5) consists of a start-up circuit, an internal voltage Preregulator, the Bandgap voltage reference and the Bias block that provides current to all the blocks.

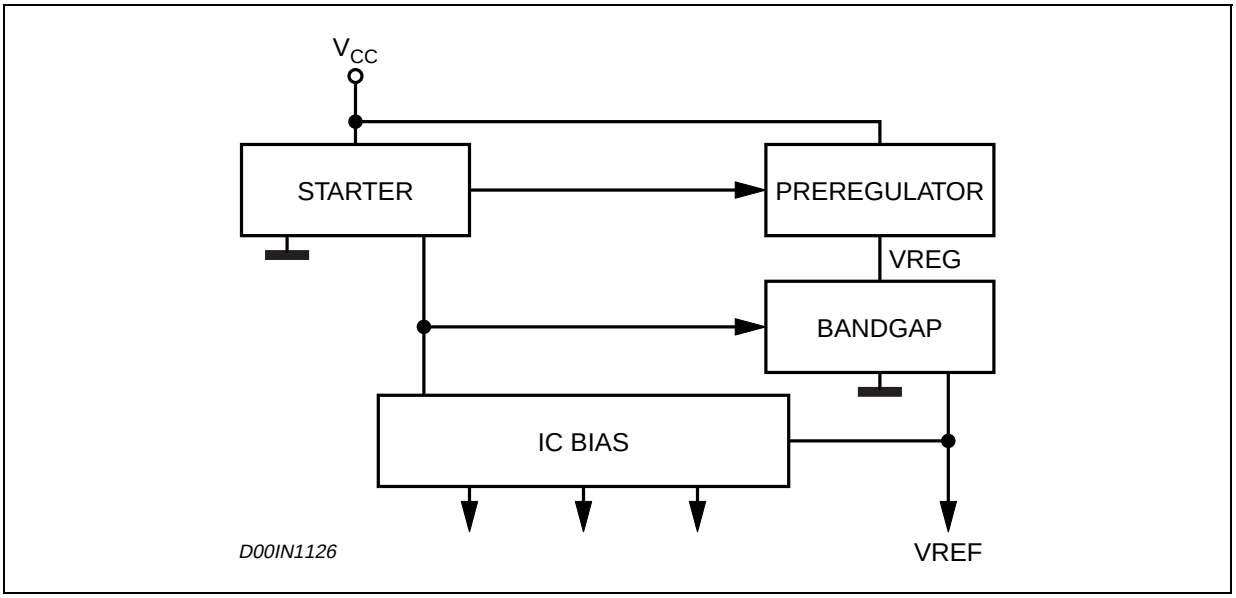
The Starter gives the start-up currents to the whole device when the input voltage goes high and the device is enabled (inhibit pin connected to ground).

The Preregulator block supplies the Bandgap cell with a preregulated voltage $V_{REG}$ that has a very low supply voltage noise sensitivity.

## VOLTAGES MONITOR

An internal block senses continuously the $V_{cc}$, $V_{ref}$ and $V_{bg}$. If the voltages go higher than their thresholds, the regulator starts to work. There is also an hysteresis on the $V_{CC}$ (UVLO).

**Figure 5. Internal Regulator Circuit**



### OSCILLATOR & SYNCHRONIZATOR

Figure 6 shows the block diagram of the oscillator circuit.

The Clock Generator provides the switching frequency of the device that is internally fixed at 250KHz. The frequency shifter block acts reducing the switching frequency in case of strong overcurrent or short circuit. The clock signal is then used in the internal logic circuitry and is the input of the Ramp Generator and Synchronizator blocks.

The Ramp Generator circuit provides the sawtooth signal, used to realize the PWM control and the internal voltage feed forward, while the Synchronizator circuit generates the synchronization signal. Infact the device has a synchronization pin that can works both as Master and Slave.

As Master to synchronize external devices to the internal switching frequency.

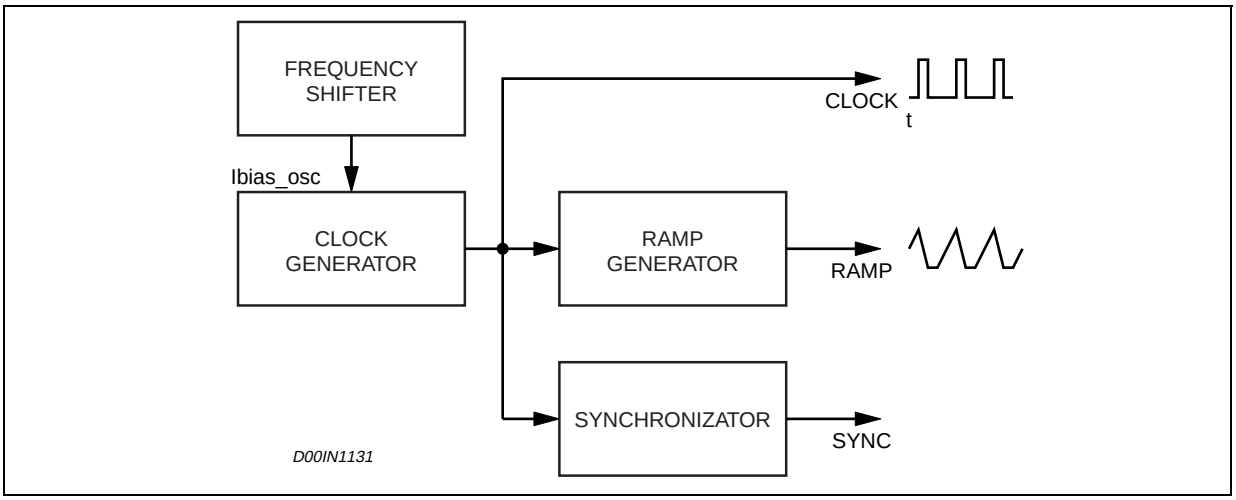
As Slave to synchronize itself by external signal up to 500KHz.

In particular, connecting together two devices, the one with the lower switching frequency works as Slave and the other one works as Master.

To synchronize the device, the SYNC pin has to pass from a low level to a level higher than the synchronization threshold with a duty cycle that can vary approximately from 10% to 90%, depending also on the signal frequency and amplitude.

The input can be driven directly from a TTL logic signal and the synchronization signal must be at least higher than the internal switching frequency of the device (250KHz).

**Figure 6. Oscillator Circuit Block Diagram**




### CURRENT PROTECTION

The L5970D has two current limit protections, pulse by pulse and frequency fold back.

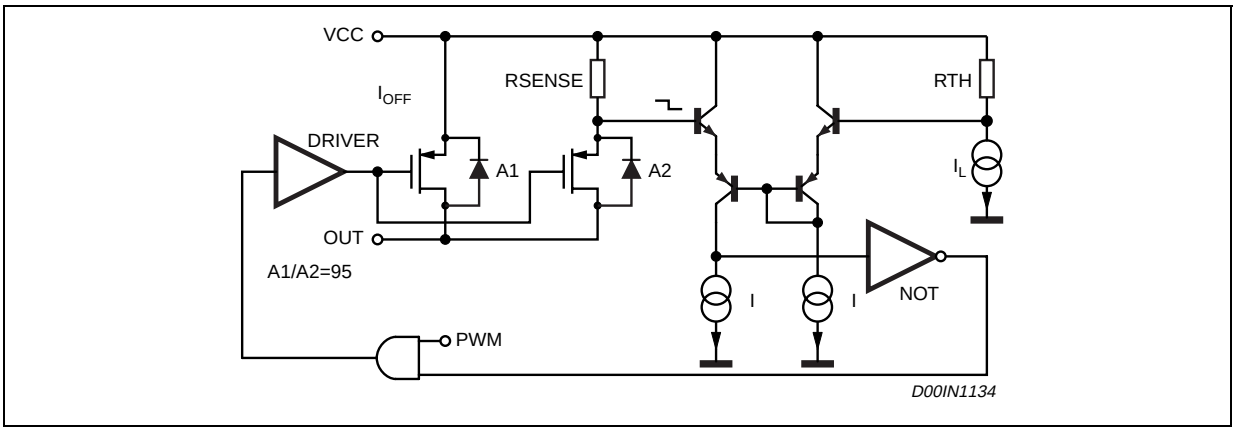
The schematic of the current limitation circuitry for the pulse by pulse protection is shown in figure 7.

The output power PDMOS transistor is split in two parallel PDMOS. The smallest one has a resistor in series, $R_{SENSE}$. The current is sensed through Rsense and if reaches the threshold, the mirror is unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse.

Due to this reduction of the ON time, the output voltage decreases.

Since the minimum switch ON time (necessary to avoid false overcurrent signal) is not enough to obtain a sufficiently low duty cycle at 250KHz, the output current, in strong overcurrent or short circuit conditions, could increase again. For this reason the switching frequency is also reduced, so keeping the inductor current under its maximum threshold. The Frequency Shifter (see fig. 6) depends on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases too.

**Figure 7. Current Limitation Circuitry**




**ERROR AMPLIFIER**

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network.

The uncompensated error amplifier has the following characteristics:

| | |
|---|---|
| Transconductance | 2300µS |
| Low frequency gain | 65dB |
| Minimum sink/source voltage | 1500µA/300µA |
| Output voltage swing | 0.4V/3.65V |
| Input bias current | 2.5µA |

The error amplifier output is compared with the oscillator sawtooth to perform PWM control.

**PWM COMPARATOR AND POWER STAGE**

This block compares the oscillator sawtooth and the error amplifier output signals generating the PWM signal for the driving stage.

The power stage is a very critical block cause it has to guarantee a correct turn on and turn off of the PDMOS.

The turn on of the power element, or better, the rise time of the current at turn on, is a very critical parameter to compromise.

At a first approach, it looks like the faster it is the rise time, the lower are the turn on losses.

But there is a limit introduced by the recovery time of the recirculation diode.

In fact when the current of the power element equals the inductor current, the diode turns off and the drain of the power is free to go high. But during its recovery time, the diode can be considered as an high value capacitor and this produces a very high peak current, responsible of many problems:

- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasitics.
- Turn on overcurrent causing a decrease of the efficiency and system reliability.
- Big EMI problems.
- Shorter freewheeling diode life.

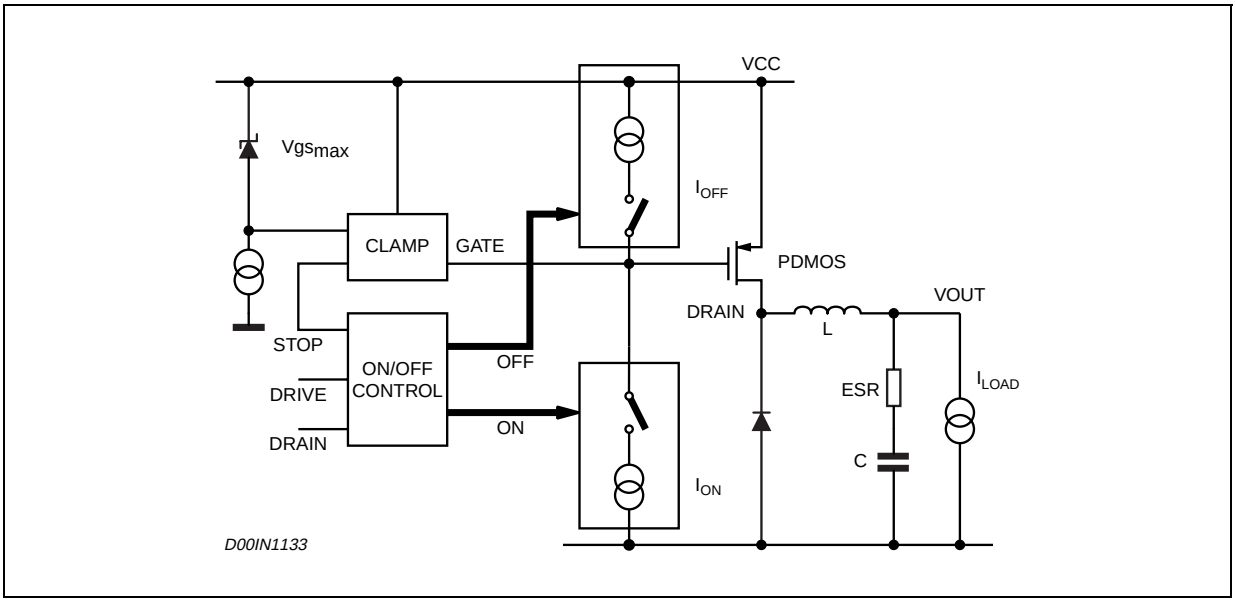
The fall time of the current during the turn off is also critical. In fact it produces voltage spikes (due to the parasitics elements of the board) that increase the voltage drop across the PDMOS.

In order to minimize all these problems, a new topology of driving circuit has been used and its block diagram is shown in fig. 8.

The basic idea is to change the current levels used to turn on and off the power switch, according with the PD-MOS status and with the gate clamp status.

This circuitry allow to turn off and on quickly the power switch and to manage the above question related to the freewheeling diode recovery time problem. The gate clamp is necessary to avoid that Vgs of the internal switch goes higher than Vgsmax. The ON/OFF Control block avoids any cross conduction between the supply line and ground.

**Figure 8. Driving Circuitry**




### INHIBIT FUNCTION

The inhibit feature allows to put in stand-by mode the device. With INH pin higher than 2.2V the device is disabled and the power consumption is reduced to less than 100µA. With INH pin lower than 0.8V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also Vcc compatible.

### THERMAL SHUTDOWN

The shutdown block generates a signal that turns off the power stage if the temperature of the chip goes higher than a fixed internal threshold (150°C). The sensing element of the chip is very close to the PDMOS area, so ensuring an accurate and fast temperature detection. An hysteresis of approximately 20°C avoids that the devices turns on and off continuously

### ADDITIONAL FEATURES AND PROTECTIONS

### FEEDBACK DISCONNECTION

In case of feedback disconnection, the duty cycle increases versus the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is turned off if the feedback pin remains floating.

## OUTPUT OVERVOLTAGE PROTECTION

The overvoltage protection, OVP, is realized by using an internal comparator, which input is connected to the feedback, that turns off the power stage when the OVP threshold is reached. This threshold is typically 30% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage (see figure 14), the OVP intervention will be set at:

$$V_{OVP} = 1.3 \cdot \frac{R_1 + R_2}{R_2} \cdot V_{FB}$$

Where $R_1$ is the resistor connected between the output voltage and the feedback pin, while $R_2$ is between the feedback pin and ground.

## ZERO LOAD

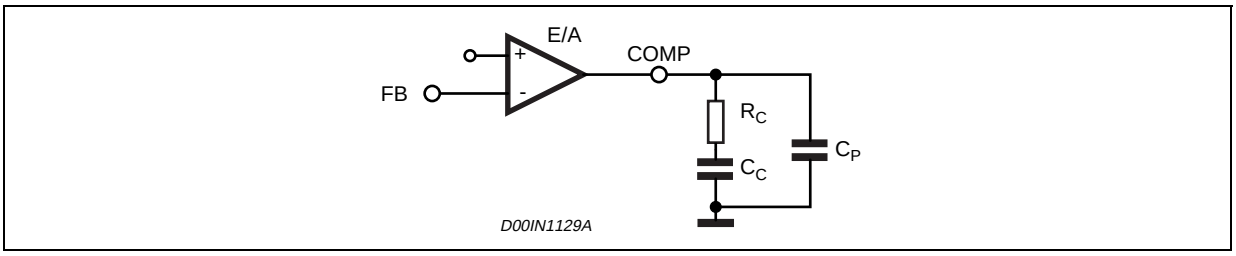
Due to the fact that the internal power is a PDMOS, no boostrap capacitor is required and so, the device works properly also with no load at the output. In this condition it works in burst mode, with random repetition rate of the burst.

## CLOSING THE LOOP

### Compensation Network

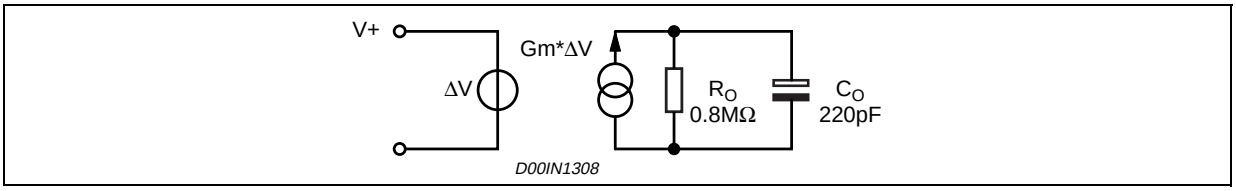
The output L-C filter of a step down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and ground is added. The simplest loop compensation network is shown in fig. 9. $R_C$ and $C_C$ introduce a pole and a zero in the open loop gain. $C_P$ doesn't affect really the system stability but is useful to reduce the noise of the COMP pin.

**Figure 9. Compensation Network**




The equivalent circuit of the error amplifier is shown in fig.10

**Figure 10. Error Amplifier Equivalent Circuit**




Considering $R_C$ = 2.7kΩ, $C_C$ = 22nF and $C_P$ = 220pF (see fig. 14), the transfer function $A_o(s)$ of the error amplifier and its compensation network becomes:

$$A_o(s) = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot (C_o + C_p) \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot (C_o + C_p) + R_c \cdot C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

The poles and zeroes of this transfer function are:

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot [0.8 \cdot 10^6] \cdot 22 \cdot 10^{-9}} = 9Hz$$

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_o + C_p)} = \frac{1}{2\pi \cdot 2.7 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 134kHz$$

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2\pi \cdot 2.7 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 2.673kHz$$

Fp1 is the low frequency pole that sets the bandwidth while the zero Fz1 is usually put near to the frequency of the double pole of the L-C filter (see below). Fp2 is usually at a very high frequency.

The transfer function of the L-C filter is given by:

$$A_{LC}(s) = \frac{1 + ESR \cdot C_{OUT} \cdot s}{L \cdot C_{OUT} \cdot s^2 + ESR \cdot S + 1}$$

The poles and zeroes of this transfer function are:

$$F_{PLC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} = \frac{1}{2\pi \cdot \sqrt{22 \cdot 10^{-6} \cdot 100 \cdot 10^{-6}}} = 3.393kHz$$

$$F_o = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}} = \frac{1}{2\pi \cdot 0.08 \cdot 100 \cdot 10^{-6}} = 19.89kHz$$

Fo is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the control loop. $F_{pLC}$ is the double pole of the L-C filter.

The PWM gain is given by the following formula:

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

Where $VOSC_{MAX}$ is the maximum value of a sawtooth waveform and $VOSC_{MIN}$ is the minimum one. A voltage feed forward is realized to have $G_{PWM}$ constant. This feature is obtained generating a sawtooth waveform directly proportional to the input voltage $V_{CC}$.

$$V_{OSCMAX} - V_{OSCMIN} = K \cdot V_{CC}$$

Where K is equal to 0.076.

Therefore the PWM gain is also equal to

$$G_{PWM}(s) = \frac{1}{K} = Const$$

This means that also if the input voltage changes, the error amplifier doesn't change its value to keep the loop in regulation, so ensuring a better line regulation and line transient response.

To sumup the Open Loop Gain can be written as:

$$G(s) = G_{PWM}(s) \cdot \frac{R_2}{R_1 + R_2} \cdot A_o(s) \cdot A_{LC}(s)$$

The Gain and Phase Bode are plotted in figures 11 and 12.

**Figure 11. Module Plot**

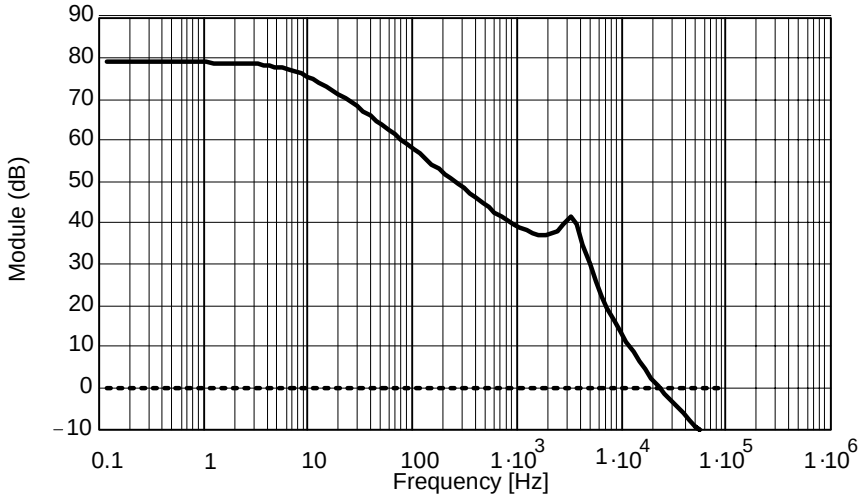
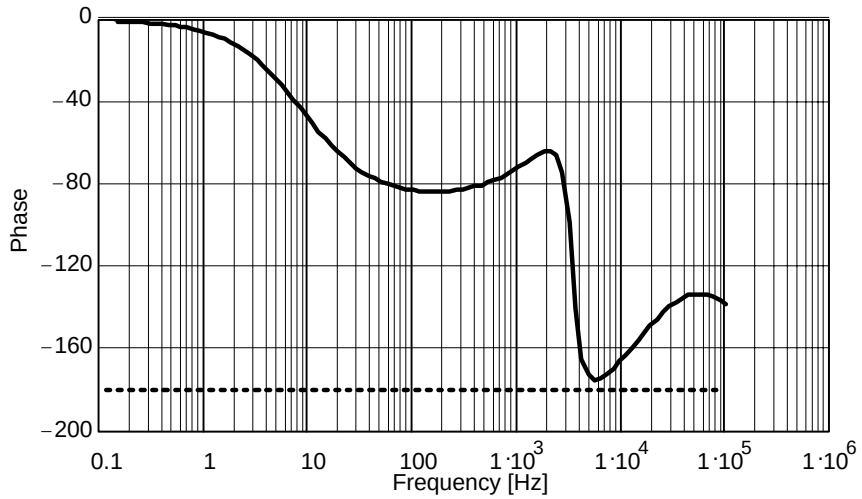



**Figure 12. Phase Plot**




The cut off frequency and the phase margin are:

$F_C$ = 22.8KHz  Phase Margin = 35°

## APPLICATION INFORMATIONS

### COMPONENTS SELECTION

#### Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current that can be up to the load current divided by two (worst case, with duty cycle of 50%).

For this reason, the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, so improving the system reliability and efficiency.

The critical parameter is usually the RMS current rating that has to be higher than the RMS input current.

The maximum RMS input current (flowing through the input capacitor) is:

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

Where $\eta$ is the expected system efficiency, D is the duty cycle and Io the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to $I_O$ divided by 2 (considering $\eta$ = 1).

The maximum and minimum duty cycles are:

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}} \quad \text{and} \quad D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where $V_F$ is the freewheeling diode forward voltage and $V_{SW}$ the voltage drop across the internal PDMOS. Considering the range $D_{MIN}$ to $D_{MAX}$ it is possible to determine the max $I_{RMS}$ following through the input capacitor.

Different capacitors can be considered:

- Electrolytic Capacitors.

  These are the most used cause are the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors.

- Ceramic Capacitors.

  If available for the requested value and voltage rating, these capacitors have usually an higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the quite high cost.

- Tantalum Capacitor.

  Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. Infact, they can be subjected to high surge current when connected to the power supply.

#### Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor

introduces a zero in the open loop gain, that helps to increase the phase margin of the system. If the zero goes at very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually good for this use.

Below there is a list of some tantalum capacitors manufacturer.

**Table 1.**

| Manufacturer | Series | Cap Value (µF) | Rated Voltage (V) | ESR (mΩ) |
|---|---|---|---|---|
| AVX | TPS | 100 to 470 | 4 to 35 | 50 to 200 |
| KEMET | T494/5 | 100 to 470 | 4 to 20 | 30 to 200 |
| SANYO POSCAP(*) | TPA/B/C | 100 to 470 | 4 to 16 | 40 to 80 |
| SPRAGUE | 595D | 220 to 390 | 4 to 20 | 160 to 650 |

(*) POSCAP capacitors have characteristic very similar to tantalum ones.

**Inductor**

The inductor value is very important cause it fixes the ripple current flowing through output capacitor.

The ripple current is usually fixed at 20-40% of Iomax, that is 0.2-0.4A with Iomax = 1A. The inductor value is approximately obtained by the following formula:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where $T_{on}$ is the ON time of the internal switch, given by $D \cdot T$.

For example, with $V_{OUT}$ = 3.3V, $V_{IN}$ = 12V and $\Delta I_O$ = 0.3A, the inductor value is about 35µH.

The peak current thought the inductor is given by:

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be seen that if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. So, fixed the peak current, higher value of the inductor permit higher value for the output current.

In the following table some inductor manufacturer are listed.

**Table 2.**

| Manufacturer | Series | Inductor Value (µH) | Saturation Current (A) |
|---|---|---|---|
| Coilcraft | DO1813HC | 22 to 33 | 1 to 1.2 |
| | DO3316 | 33 to 47 | 1.6 to 2 |
| Coiltronics | UP1B | 22 to 33 | 1 to 1.2 |
| | UP2B | 33 to 47 | 1.7 to 2 |
| BI | HM76-2 | 22 to 33 | 1 to 1.2 |
| | HM76-3 | 33 to 47 | 2 to 2.5 |
| Murata | LQN6C | 22 to 33 | 0.9 to 1.2 |
| PANASONIC | ELLATV | 22 to 47 | 1.4 to 2.05 |
| SUMIDA | CR75 | 22 to 33 | 1.05 to 1.25 |

## LAYOUT CONSIDERATIONS

The layout of switching DC/DC converters is very important to minimize noise and interference.

Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference and so they should be as far as possible from the high current paths.

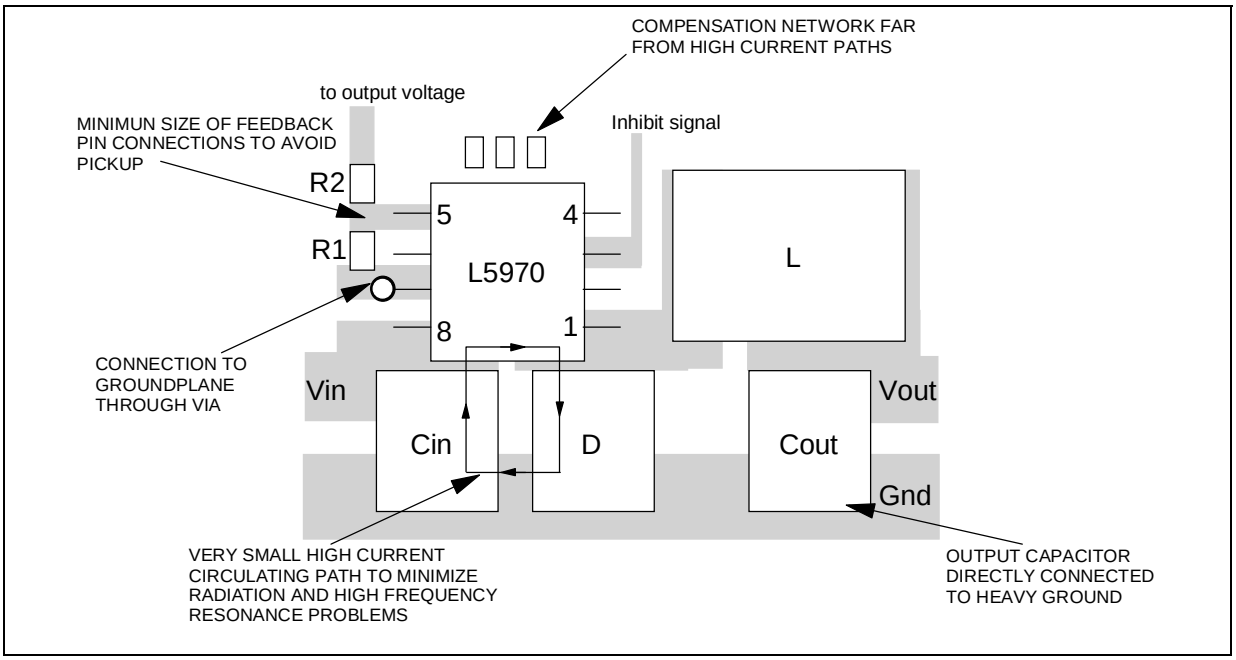
Below there is a layout example (Fig. 13).

The input and output loops are minimized to avoid radiation and high frequency resonance problems.

The feedback pin connections to the external divider are very close to the device to avoid pick up noise.

Moreover the GND pin of the device is connected to the ground plane directly with VIA on the bottom side of the PCB.

**Figure 13. Layout example**




## THERMAL CONSIDERATIONS

The dissipated power of the device is related to three different sources:

- switch losses due to the not negligible $R_{DSON}$. These are equal to:

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between Vout and Vin, but in practical is quite higher than this value to compensate the losses of the overall application. Due to this reason, the switch losses related to the $R_{DSON}$ increases compared with the ideal case.

- Switch losses due to its Turn On and Off. These are given by the following relation:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

Where $T_{ON}$ and $T_{OFF}$ are the overlap times of the voltage across the power switch and the current flowing into

it during the Turn On and Turn Off phases. $T_{SW}$ is the equivalent switching time.

- Quiescent current losses.

$$P_Q = V_{IN} \cdot I_Q$$

Where $I_Q$ is the quiescent current.

Example:

Vin = 5V

Vout = 3.3V

Iout = 1A

$R_{DSON}$ has a typical value of 0.25Ω @ 25°C and increases up to a maximum value of 0.5Ω @ 150°C. We can consider a value of 0.4Ω.

$T_{SW}$ is approximately 120ns.

$I_Q$ has a typical value of 2.5mA @ $V_{in}$ = 12V.

The overall losses are:

$$P_{TOT} = R_{DSON} \cdot (I_{OUT})^2 \cdot D + V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} + V_{IN} \cdot I_Q =$$

$$= 0.4 \cdot 1^2 \cdot 0.7 + 5 \cdot 1 \cdot 120 \cdot 10^{-9} \cdot 250 \cdot 10^3 + 5 \cdot 2.5 \cdot 10^{-3} \cong 0.44W$$

The junction temperature of device will be:

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

Where $T_A$ is the ambient temperature and $Rth_{J-A}$ is the thermal resistance junction to ambient.

Considering that the device in SO8 package mounted on board with a good groundplane has a thermal resistance junction to ambient ($Rth_{J-A}$) of about 115°C/W and considering an ambient temperature of about 70°C

$$T_J = 70 + 0.44 \cdot 115 \cong 121°C$$

### APPLICATION CIRCUIT

In figure 14 is shown the demo board application circuit for the device in SMD version, where the input supply voltage, Vcc, can range from 4.4V to 25V due to the rated voltage of the input capacitor and the output voltage is adjustable from 1.235V to $V_{cc}$.

**Figure 14. Demo board Application Circuit**

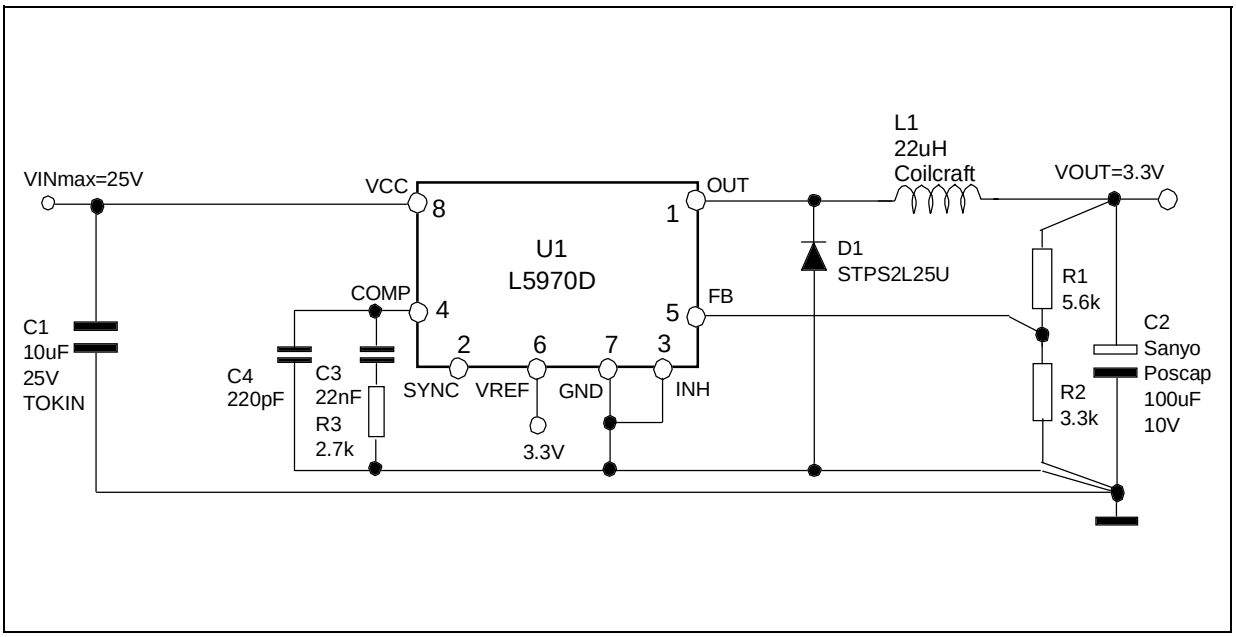



**Table 3. Component List**

| Reference | Part Number | Description | Manufacturer |
|---|---|---|---|
| C1 | | 10µF, 25V | TOKIN |
| C2 | 10TPB100M | 100µF, 10V | Sanyo, POSCAP |
| C3 | C1206C223K5RAC | 22nF, 10%, 50V | KEMET |
| C4 | C1206C221J5GAC | 220pF, 5%, 50V | KEMET |
| R1 | | 5.6K, 1%, 0.25W | Neohm |
| R2 | | 3.3K, 1%, 0.25W | Neohm |
| R3 | | 2.7K, 1%, 0.25W | Neohm |
| D1 | STPS2L25U | 2A, 25V | ST |
| L1 | DO3316P-333 | 22µH, 1.2A | COILCRAFT |

**Figure 15. PCB layout (component side)**

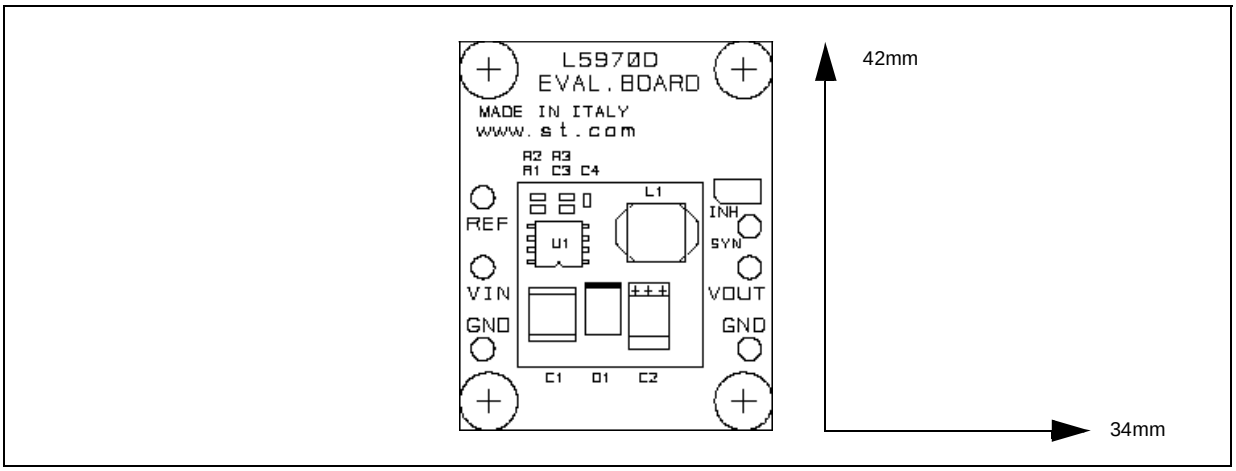



**Figure 16. PCB layout (bottom side)**

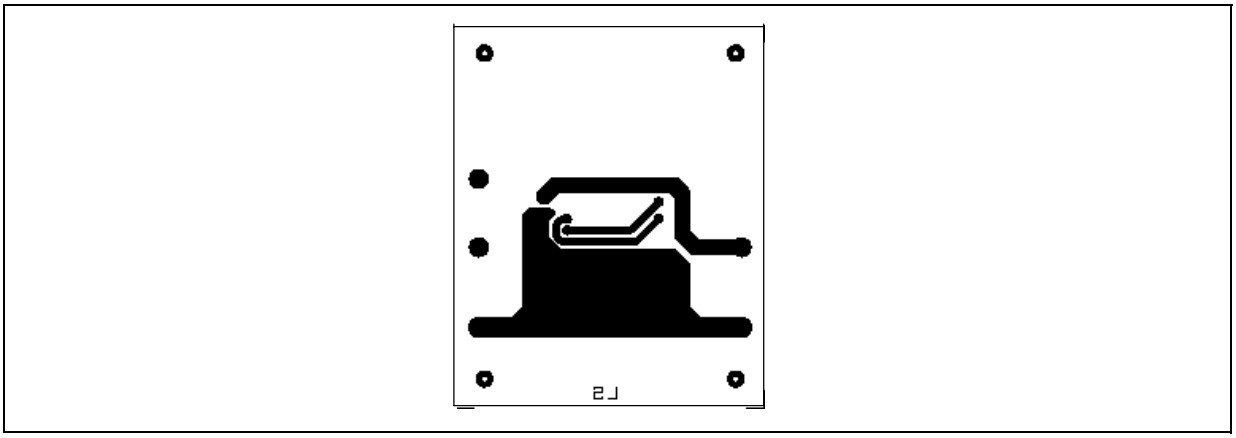
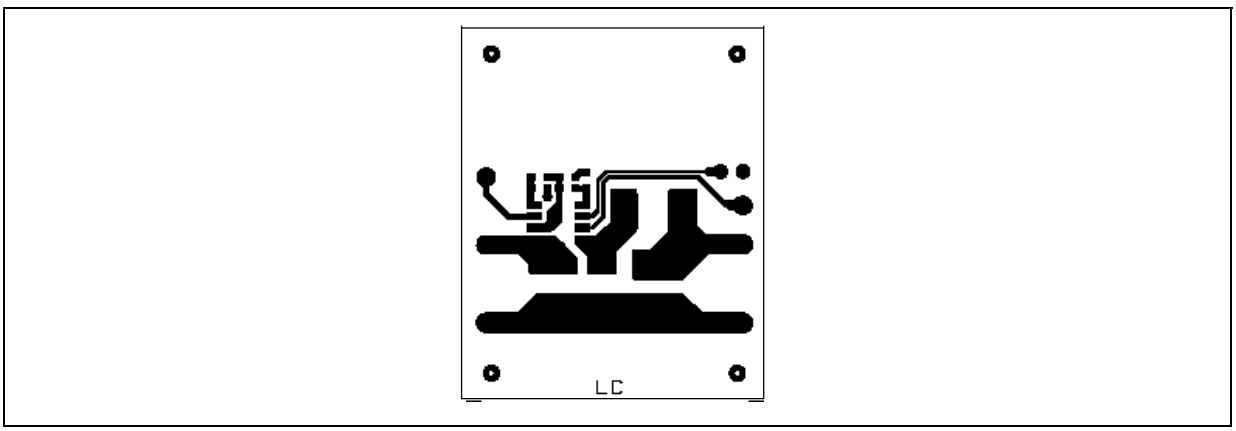


**Figure 17. PCB layout (front side)**



Below some graphs show the Tj versus output current in different conditions of the input and output voltage and some efficiency measurements.

**Figure 18. Junction Temperature vs. Output Current (SO8) *)**

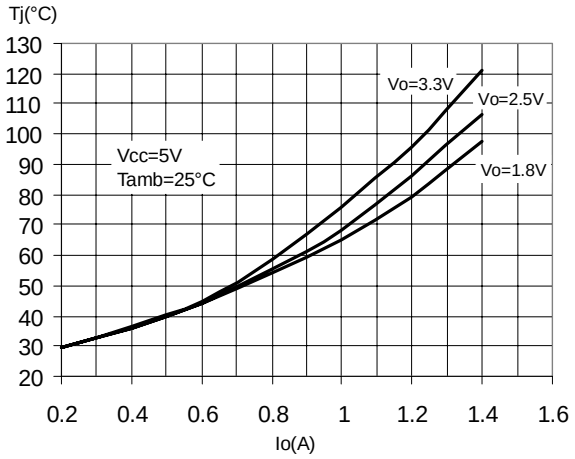



**Figure 19. Junction Temperature vs. Output Current (SO8) *)**

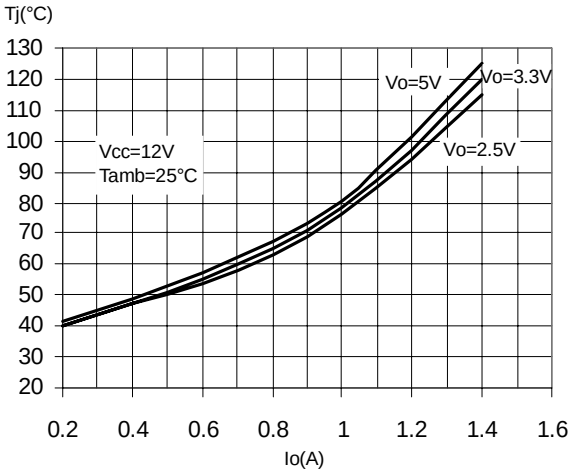



**Figure 20. Junction Temperature vs. Output Current (SO8) *)**

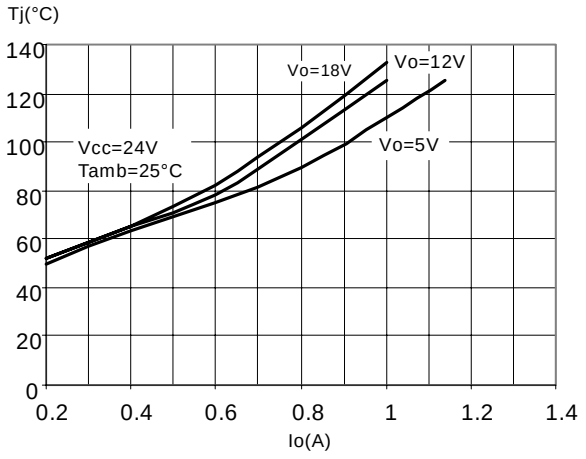



**Figure 21. Efficiency vs. Output Current**

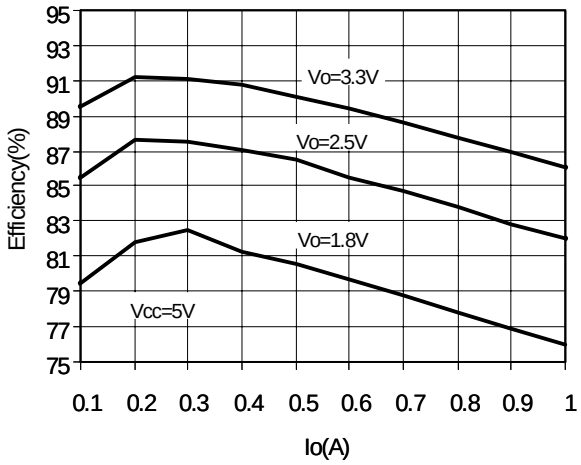
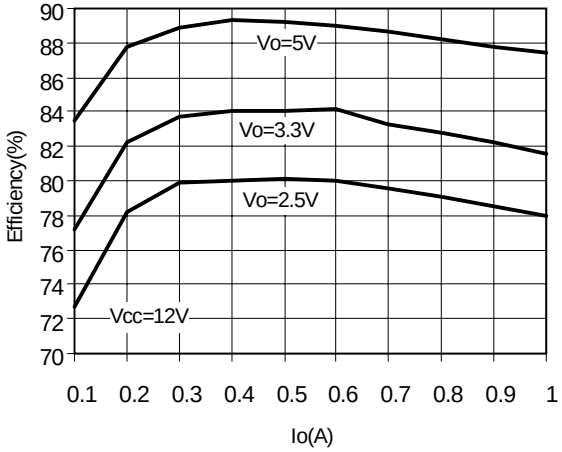



**Figure 22. Efficiency vs. Output Current**




*) Package mounted on demoboard

## APPLICATION IDEAS

### POSITIVE BUCK-BOOST REGULATOR

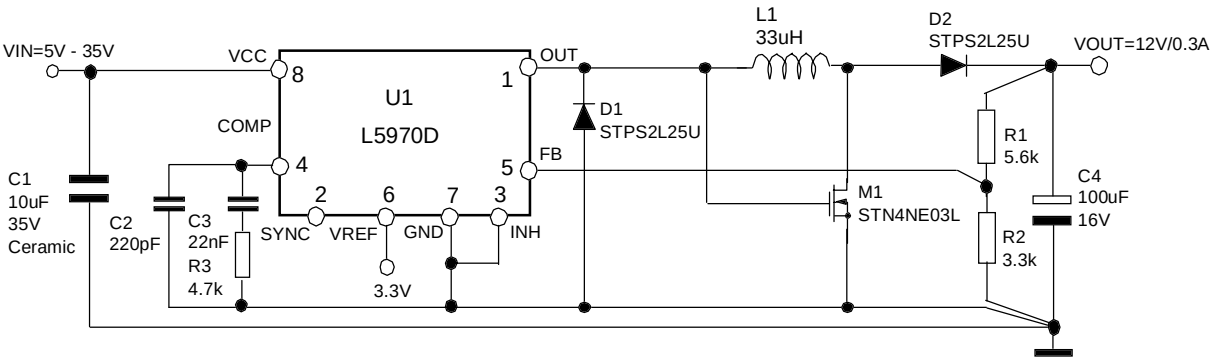
The device can be used to realize an Up-Down converter with a positive output voltage. In figure is shown the schematic circuit of this topology for an output voltage of 12V.

The input voltage can range from 5V and 35V.

The output voltage is given by Vo=Vin · D/(1-D), where D is duty cycle.

The maximum output current is given by Iout=1× (1-D). The current capability is reduced by the term (1-D) and so, for example, with a duty cycle of 0.5, the maximum output current deliverable to the load is 0.5A. This is due to the fact that the current flowing trough the internal power switch is delivered to the output only during the OFF phase.

**Figure 23. Positive Buck-Boost regulator**




### BUCK-BOOST REGULATOR

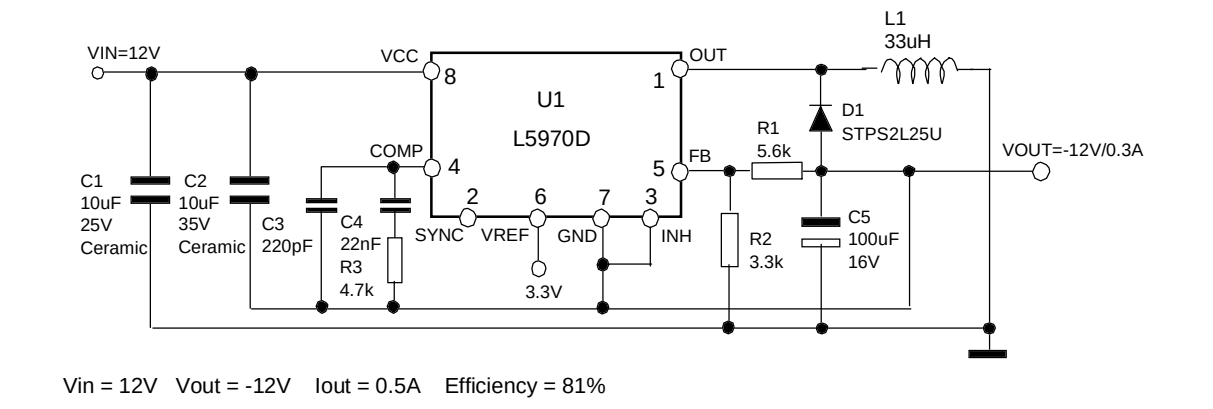
In Figure 24 is shown the schematic circuit to realize a standard Buck-Boost topology.

The output voltage is given by Vo=-Vin · D/(1-D).

The maximum output current is equal to Iout=1 · (1-D), for the same reason of the Up-Down converter.

An important thing to take in account is that the Gnd pin of the device is connected to the negative output voltage. So, the device undergoes a voltage equal to Vin-Vo, that has to be lower than 36V (maximum operating input voltage).

**Figure 24. Buck-Boost regulator**



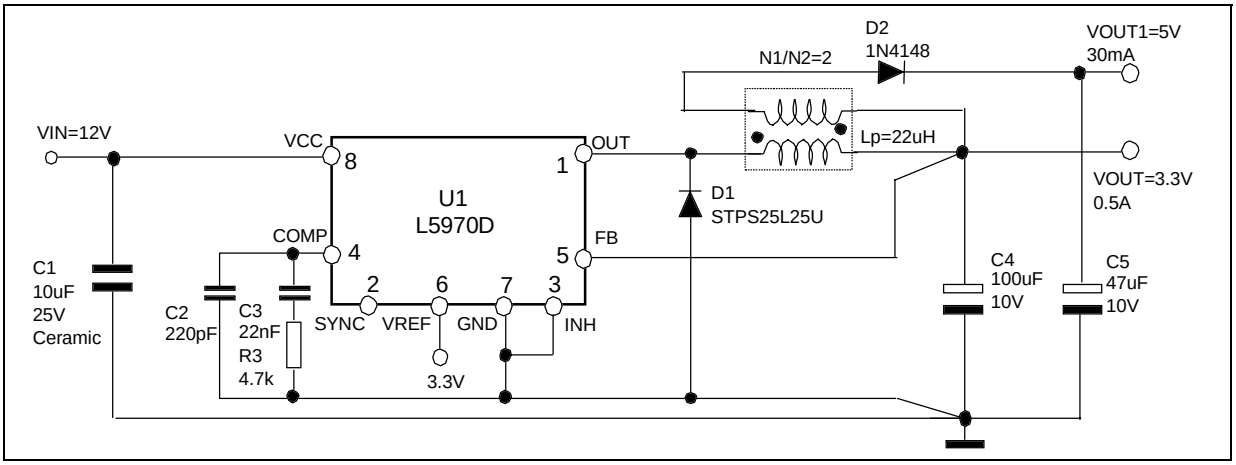
### DUAL OUTPUT VOLTAGE WITH AUXILIARY WINDING

When two output voltages are required, it is possible to realize a dual output voltage converter by using a coupled inductor.

During the ON phase the current is delivered to Vout while D2 is reverse biased.

During the OFF phase the current is delivered, through the auxiliary winding, to the output voltage Vout1. This is possible only if the magnetic core has stored a sufficient energy. So, to be sure that the application is working properly, the load related to the second output Vout1 should be much lower than the load related to Vout.

**Figure 25. Dual output voltage with auxiliary winding**

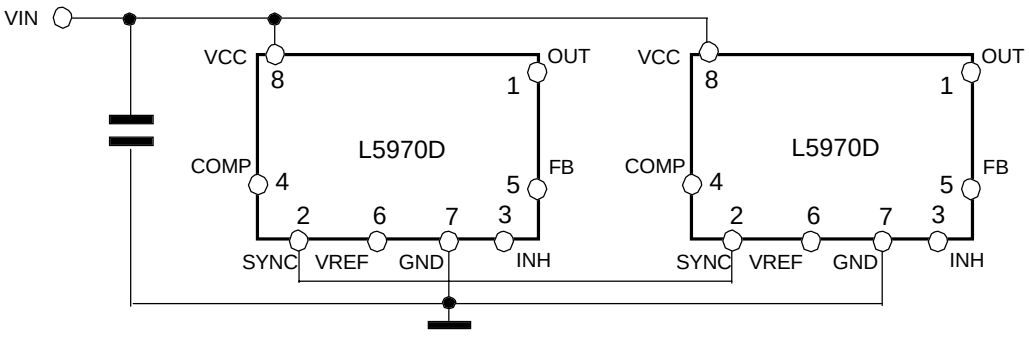



### SYNCHRONIZATION EXAMPLE

Two or more devices (up to 6) can be synchronized just connecting together the synchronization pin. In this case, the device with an slightly higher switching frequency value will work as master and the ones with a slightly lower switching frequency value will work as a slave.

The device can also be synchronized from an external source. In this case the logic signal (see synchronization section) must have a frequency higher than the internal switching frequency of the device (250KHz).

**Figure 26. Synchronization example**



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