



Porting an application from the ST10F168 to the ST10F269

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1 - INTRODUCTION

The ST10F269 is a new derivative of the STMicroelectronics ST10 family of 16-bit single-chip CMOS micro-controllers. It is upward compatible with the ST10F168.

The goal of this document is to enlighten the differences between the ST10F269 and ST10F168 and is intended for hardware or software designers who are adapting an existing application based on the ST10F168 to the ST10F269.

This document will present the modified functionalities of the ST10F269, then the new ones before looking at the modified and the new registers. For each part, the differences with the ST10F168 that may be impacting will be stressed and some advice on the way they can be handled will be given.

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2 - MODIFIED FUNCTIONALITIES

2.1 - Pin Out

2.1.1 - Pin 84

This pin was named Vpp/RPD on the ST10F168 and was the 12V input pin for Flash programming. In the ST10F269, it is now only used as RPD as the Flash is a single voltage one.

2.1.1.1 - Hardware Impact

This pin is no longer designed to accept 12V inputs. Its ratings are the same as any other pin: -0.5V to VDD +0.5V.

2.1.1.2 - Software Impact

None.

Note: Some applications might be using the Vpp pin as a protection for Flash programming by software controlling the 12V charge pump. The ST10F269 being now a single voltage Flash, Vpp will appear as permanently "ON" and thus such a protection can not be reproduced with the ST10F269.

2.1.2 - Pins 17 and 56

For the ST10F168, these are V_{DD} pins connected to 5Volts.

For the ST10F269, these pins 17 and 56 are de-coupling pins for the 3,3V and respectively named DC2 and DC1. A de-coupling capacitor must be connected to these pins and the nearest V_{SS}.

2.1.2.1 - Hardware Impact

The application board should be re-designed in order to introduce the decoupling capacitors.

2.1.2.2 - Software Impact

None.

2.2 - XRAM

The ST10F168 has only 6KBytes of extension RAM while the ST10F269 has 10KBytes.

The XRAM address range in the ST10F168 is 00'D000h - 00'E7FFh and is enabled if XPEN (bit 2 of SYSCON register) is set.

The XRAM of the ST10F269 is divided into 2 ranges named XRAM1 of 2KBytes and XRAM2 of 8KBytes:

- The **XRAM1** address range is 00'E000h - 00'E7FFh if enabled (XPEN set -bit 2 of SYSCON register- **AND** XRAM1EN set - bit 2 of XPERCON register-).
- The **XRAM2** address range is 00'C000h - 00'DFFFh if enabled (XPEN set -bit 2 of SYSCON register- **AND** XRAM2EN set - bit 3 of XPERCON register-).

2.2.1 - Hardware Impact

None.

2.2.2 - Software Impacts

The memory mapping of the application may be impacted by the difference in XRAM size or by the separation in 2 ranges independently selectable.

In the ST10F168, setting XPEN bit in SYSCON register enables the XRAM.

In the ST10F269, setting XPEN bit in SYSCON register enables the XRAM1 only (default reset configuration of the new XPERCON register). Thus accesses to the range 00'D000h - 00'DFFFh that was part of the ST10F168 XRAM will be redirected to external memory.

Three configurations may be seen:

1. Configuration 1: no external memory in address range 00'C000h - 00'CFFFh.

Impact: one register to configure.

Work-around: Set the bit XRAM2EN of XPERCON new register. It enables the second XRAM range. The total XRAM range is then 00'C000h - 00'E7FFh which includes the ST10F168 range.

2. Configuration 2: external memory exists in page 3 and is below 2K Byte size.

Impact: one register to configure, the external memory has to be remapped within page 3.

Work-around: Set the bit XRAM2EN and clear the bit XRAM1EN of XPERCON new register. Then remap your variables to uses the XRAM2 range as your XRAM (bigger than the ST10F168 so no issue) and remap your 2K Byte range of external memory at the XRAM1 location. This way you keep everything within page 3.

3. Configuration 3: external memory exists in page 3 and is above 2K Byte size.

Impact: one register to configure, the external memory to be remapped in another page.

Work-around: Set the bit XRAM2EN of the XPERCON new register and relocate your external memory in page 2 (address range 0x8000 - 0xBFFF) if possible. Then change the link directives according to the new mapping.

Note: The setting of the bits in XPERCON must be done **before** enabling the XBus Peripherals by the XPEN bit of SYSCON.

2.3 - Flash EEPROM

The ST10F168 and the ST10F269 don't have the same Flash memories. The embedded Flash of the ST10F269 has a technology really similar to the stand-alone Flash memories of STMicroelectronics.

Table 1 : Flash Memories Key Characteristics

	ST10F168	ST10F269
Flash Size	256K Bytes	256K Bytes
Flash Organization	4 banks	7 blocks
Programming voltage	12 Volts	5 Volts
Programming method	STEAK™	Write/Erase Controller
Program/Erase cycles	10 000, 20 years of data retention	100.000, ≥ 10 years of data retention

2.3.1 - Hardware Impacts

The 12 Volts input on pin 84 is no longer needed.

2.3.2 - Software Impacts

The mapping of the application and the programming and erasing routines are impacted.

ST10F168 bank 0: this range is fully compatible with the block 0 of the ST10F269.

ST10F168 bank 1: this range is now covered by the blocks 1, 2 and 3 of the ST10F269. It is not mandatory to re-map Code and Data: these 3 blocks could be considered as a single range.

ST10F168 bank 2 and bank 3: The highest third of bank 2 and the lowest third of bank 3 correspond to the block 5 of the ST10F269. Code and Data have to be remapped to take care of this separation in three ranges of 64K Bytes if these banks were likely to be independently reprogrammed.

The programming-erasing software must also be rewritten as the ST10F269 does not work with the STEAK™ but with a Write/Erase Controller.

Figure 1 : Flash Memories' Mapping

		ST10F168 Flash Mapping		ST10F269 Flash Mapping	
Segment 4	13	04'FFFF	Bank 3: 96K Bytes	04'FFFF	Block 6: 64K Bytes
	12	04'C000		04'C000	
	11	04'8000		04'8000	
	10	04'4000		04'4000	
Segment 3	0F	03'8000	Bank 2: 96K Bytes	03'FFFF	Block 5: 64K Bytes
	0E			03'8000	
	0D	03'7FFF		03'4000	
Segment 2	0C	03'0000	Bank 1H: 32K Bytes	03'0000	Block 4: 64K Bytes
	0B	02'C000		02'FFFF	
	0A	02'8000		02'C000	
	09	02'4000		02'8000	
Segment 1	08	02'0000	Bank 1L ^(*) : 16K Bytes	02'4000	Block 3: 32K Bytes
	07	01'FFFF		02'0000	
	06	01'C000	Bank 0 ^(*) : 16K Bytes	01'FFFF	Block 2 ^(*) : 8K Bytes
		01'8000		01'C000	
		01'7FFF		01'8000	
05	01'4000	Bank 0 ^(*) : 16K Bytes	01'7FFF	Block 1 ^(*) : 8K Bytes	
			01'6000		
Segment 0	04	01'3FFF	Bank 0 ^(*) : 16K Bytes	01'5FFF	Block 0 ^(*) : 16K Bytes
	03	01'0000		01'4000	
		00'FFFF		01'3FFF	
	02	00'8000		00'FFFF	
1	00'7FFF	Bank 1L ^(*) : 16K Bytes	00'8000	Block 2 ^(*) : 8K Bytes	
			00'7FFF		
	00'6000		00'7FFF		
00	00'4000	Bank 0 ^(*) : 16K Bytes	00'5FFF	Block 1 ^(*) : 8K Bytes	
			00'4000		
	00	00'3FFF	Bank 0 ^(*) : 16K Bytes	00'3FFF	Block 0 ^(*) : 16K Bytes
		00'0000		00'0000	

Note: Bank 0 (Block 0) and Bank 1L (Block 1) may be remapped from segment 0 to segment 1 by setting SYSCON-ROMS1 (before EINIT).

2.4 - A/D Converter

The A/D Converter of the ST10F269 is based upon a Resistor-Capacitor circuitry while the ST10F168 one is based upon fully switched capacitors. The ST10F269 does not have the self-calibrated feature, but the guaranteed Total Unadjusted Error is ± 2 LSB.

2.4.1 - Hardware Impacts

The table below lists the differences in the DC characteristics of the two devices.

Table 2 : ADC differences

Parameter	Symbol	Limit values for ST10F168		Limit values for ST10F269		Unit
		Minimum	Maximum	Minimum	Maximum	
Analog Reference voltage	V_{AREF}	4.0	$V_{DD} + 0.1$	4.0	$V_{DD} + 0.1$	V
Analog Input Voltage	V_{AIN}	V_{AGND}	V_{AREF}	V_{AGND}	V_{AREF}	V
ADC Input capacitance	C_{AIN}	-	33	-	10	pF
Not sampling		-	33	-	15	pF
Sample time	t_S	-	$2 t_{SC}$	$2 t_{CC}$	$16 t_{CC}$	
Conversion time	t_C	-	$14 t_{CC} + t_S + 4 TCL$	-	$14 t_{CC} + t_S + 4 TCL$	
Total Unadjusted Error	TUE	-2.0	+2.0	-2.0	+2.0	LSB
Internal resistance of analog source	R_{ASRC}	-	$t_S[ns]/330 - 0.25$		$t_S[ns]/150 - 0.25$	k Ω
Reference supply current running mode	I_{AREF}			-	500	μA
power-down mode				-	1	μA
Differential Nonlinearity	DNL			-0.5	+0.5	LSB
Integral Nonlinearity	INL			-1.5	+1.5	LSB
Offset Error	OFS			-1.0	+1.0	LSB

2.4.2 - Software Impacts

None.

3 - NEW FUNCTIONNALITIES

3.1 - CAN Modules

The ST10F168 has only one CAN module.

The ST10F269 has two CAN modules which are both identical to the one of the ST10F168. By default none of the CAN modules is enabled. The two modules can be independently enabled or disabled during the initialization phase.

3.1.1 - Hardware Impacts

None.

3.1.2 - Software Impacts

None.

3.2 - Real Time Clock

This is a new functionality of the ST10F269.

The Real Time Clock is an independent timer. Its clock is directly derived from the clock oscillator so that it can keep on running even in idle or power down mode (if enabled to).

3.2.1 - Hardware Impacts

None.

3.2.2 - Software Impacts

None. By default this peripheral is disabled.

3.3 - MAC Unit

This Multiply and Accumulate unit is a feature added on the ST10F269. It provides DSP-like instructions that may be valuable for signal processing algorithms.

3.3.1 - Hardware Impacts

None.

3.3.2 - Software Impacts

None.

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4.2 - WDTCON Register

Some bits have been added for the ST10F269.

Each of the different reset sources is indicated in the WDTCON register of the ST10F269. The indicated bits are cleared with the EINIT instruction. It is thus possible to identify the reset during the initialization phase.

ST10F168: WDTCON (FFAEh / D7h) SFR Reset Value: 000Xh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTREL								-	-	-	-	-	-	WDTR	WDTIN
RW														R	RW

ST10F269: WDTCON (FFAEh / D7h) SFR Reset Value: 000Xh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTREL								-	-	PONR	LHWR	SHWR	SWR	WDTR	WDTIN
RW										R	R	R	R	R	RW

Bit	Function	
WDTIN	Watchdog Timer Input Frequency Selection 0 Input frequency is $f_{CPU} / 2$ 1 Input frequency is $f_{CPU} / 128$	
WDTR	Watchdog Timer Reset Indication Flag Set by the watchdog timer on an overflow. Cleared by a hardware reset or by the SRVWDT instruction.	
SWR 1)	Software Reset Indication Flag Set by the SRST execution. Cleared by the EINIT instruction.	New
SHWR 1)	Short Hardware Reset Indication Flag Set by the input RSTIN. Cleared by the EINIT instruction.	New
LHWR 1)	Long Hardware Reset Indication Flag Set by the input RSTIN. Cleared by the EINIT instruction.	New
PONR 1)2)	Power-On (Asynchronous) Reset Indication Flag Set by the input RSTIN if a power-on condition has been detected. Cleared by the EINIT instruction.	New
WDTREL	Watchdog Timer Reload Value (for the high byte)	

Note: More than one reset indication flag may be set. After EINIT, all flags are cleared.
Power-on is detected when the internal voltage rises from 0V to a value > 2.0V is recognized.

4.2.1 - Hardware Impacts

None.

4.2.2 - Software Impacts

None if the ST10F168 software was masking the non-implemented bits.

5.1.1.1 - Hardware Impacts

None.

5.1.1.2 - Software Impacts

The value has to be changed from its default reset one to match XRAM size compatibility. Refer to XRAM section for more details.

5.1.2 - POCOnx Registers

These are new registers of the ST10F269.

The port output control registers POCOnx allow to select the port output driver characteristics of a port. The aim of these selections is to adapt the output drivers to the application's requirements, and to improve the EMI behavior of the device. Two characteristics may be selected:

- **Edge characteristic** defines the rise/fall time for the respective output, i.e. the transition time. Slow edge reduce the peak currents that are sunk/sourced when changing the voltage level of an external capacitive load. For a bus interface or pins that are changing at frequency higher than 1MHz, however, fast edges may still be required.
- **Driver characteristic** defines either the general driving capability of the respective driver, or if the driver strength is reduced after the target output level has been reached or not. Reducing the driver strength increases the output's internal resistance, which attenuates noise that is imported via the output line. For driving LEDs or power transistors, however, a stable high output current may still be required.

POCONx				ESFR				Reset Value: 0000h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PNzDC		PNzEC		PNyDC		PNyEC		PNxEC		PNxEC		PNwEC		PNwEC	
RW		RW		RW		RW		RW		RW		RW		RW	

Table 4 : POCOnx Registers Bits

Bit	Function	Reset value
PNxEC	<p>Port Nibble x Edge Characteristic (rise/fall time)</p> <p>00 Fast edge mode, rise/fall times depend on the driver's dimensioning.</p> <p>01 Slow edge mode, rise/fall times ~60 ns</p> <p>10 Reserved</p> <p>11 Reserved</p>	00
PNxDC	<p>Port Nibble x Driver Characteristic (output current)</p> <p>00 High Current mode: Driver always operates with maximum strength.</p> <p>01 Dynamic Current mode: Driver strength is reduced after the target level has been reached.</p> <p>10 Low Current mode: Driver always operates with reduced strength.</p> <p>11 Reserved</p>	00

The new registers are the following:

- POCOn0L, POCOn0H, POCOn1L, POCOn1H, POCOn2, POCOn3, POCOn4, POCOn5, POCOn6, POCOn7 and POCOn8 dealing with the respective ports,
- POCOn20 dealing with the dedicated pins ALE, RD and WR.

5.1.2.1 - Hardware Impacts

ST10F168 and ST10F269 ports don't have the same behavior in their default reset configuration. The ST10F269 default reset values select the "Fast Edge Mode" and the "High Current Mode", while the ST10F168 is designed for "Fast Edge Mode" and "Dynamic Current Mode".

5.1.2.2 - Software Impacts

To have on the ST10F269 a behavior equivalent to the ST10F168's one, POCONx values must be set to the following:

- 0x0044h for POCON0L, POCON0H, POCON1L, POCON1H, POCON4, POCON5, POCON6, POCON7, POCON8 and POCON20,
- 0x4444h for POCON2 and POCON3.

5.2 - New Registers not Impacting the Application

5.2.1 - ODP4 Register (F1CAh / E5h)

This is a new register of the ST10F269. For CAN configuration support, Port 4 has a new open drain function controlled with this register.

5.2.2 - EXISEL Register (F1DAh / DAh)

This register, standing for External Interrupt Source Selection, has been added in the ST10F269.

The purpose of this new register is to select the interrupt sources of the fast external interrupts among the other peripherals. For example the CANy controller receive signal (CANy_RxD) can be used to interrupt the system (y = 1,2).

6 - ELECTRICAL CHARACTERISTICS

6.1 - DC Characteristics

6.1.1 - Absolute Maximum Ratings

They are the same.

6.1.2 - DC Characteristics

6.1.2.1 - Operating Voltage

The ST10F269 appears like a 5V device externally but operates at a lower internal voltage thanks to a voltage regulator.

Hardware Impacts

The pins 56 and 17 which were used as V_{DD} and GND for the ST10F168. Now for the ST10F269, these pins are named DC1 and DC2, respectively pins 56 and 17, and are used as de-coupling pins for the internal core supply.

Software Impacts

None.

6.1.2.2 - Programming Voltage

The ST10F269 has a single voltage Flash Memory.

Hardware Impacts

The 12V input on the pin 84 is no longer needed.

Software Impacts

None.

6.1.2.3 - Miscellaneous

Table 5 : DC Characteristics Differences

Symbol	Parameter	ST10F168		ST10F269		Unit
		Minimum	Maximum	Minimum	Maximum	
HYS	Input Hysteresis (special threshold)	300	-	400	-	mV
I_{ALEH}	ALE active current	-	600	-	500	μ A
I_{PD}	Power-down mode supply current	-	100	-	500	μ A
I_{PD2}	Power-down mode supply current (Real time clock enabled, oscillator enabled)	-	-	-	5	mA
I_{CC}	Power supply current	-	$20 + 6 \times F_{CPU}$	-	$30 + 4 \times F_{CPU}$	mA
I_{ID}	Idle mode supply current	-	$20 + 3 \times F_{CPU}$	-	$20 + F_{CPU}$	mA

6.2 - AC characteristics at 25MHz

6.2.1 - Hardware Impact

None.

6.2.2 - Software Impact

None.

7 - REFERENCES

The following internal documents were used to write this application note:

- ST10F269 Data sheet.
- ST10F168 Data sheet.

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