AN1302
APPLICATION NOTE

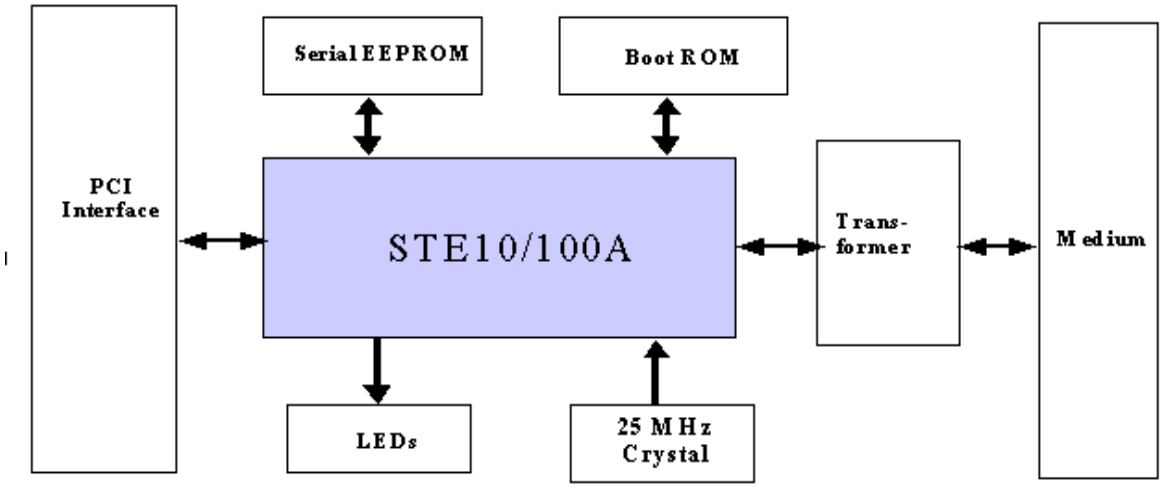
STE10/100A - PCI 10/100 ETHERNET CONTROLLER WITH INTEGRATED PHY

1.0 APPLICATION NOTE OVERVIEW

The STE10/100A is a single chip Ethernet solution for PCI bus adapter applications. Its design is optimized for high throughput, low CPU utilization and low cost. It is optional to program STE10/100A as a MAC mode and bring out the MII interface with the external PHY. This application note is divided into the following topics: General Description, Software Programmer's Guide, Optional MAC Mode and MII Interface Configuration, Print Circuit Board Layout Guidelines, NIC (Network Interface Card) Application Design Schematics and Bill of Materials. This application note should be reviewed with the STE10/100A data sheet.

2.0 GENERAL DESCRIPTION

The STE10/100A is a high performance, low power, 3.3V PCI Fast Ethernet controller with integrated physical layer interface for 10BASE-T and 100BASE-TX application. The system diagram is shown as below.



The STE10/100A provides both half-duplex and full-duplex operation, as well as support for full-duplex flow control. It provides long FIFO buffers for transmission and receiving, and early interrupt mechanism to enhance performance. The STE10/100A also supports ACPI and PCI compliant power management functions. Some key features are listed as follows:

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Support for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- PCI bus interface Rev. 2.2 compliant
- Support PC99 wake on LAN
- Provides two independent long FIFOs with 2k bytes each for transmission and receiving
- Pre-fetch up to two transmit packets to minimize inter frame gap(IFG) to 0.96us
- Retransmits collided packet without reload from host memory within 64 bytes.

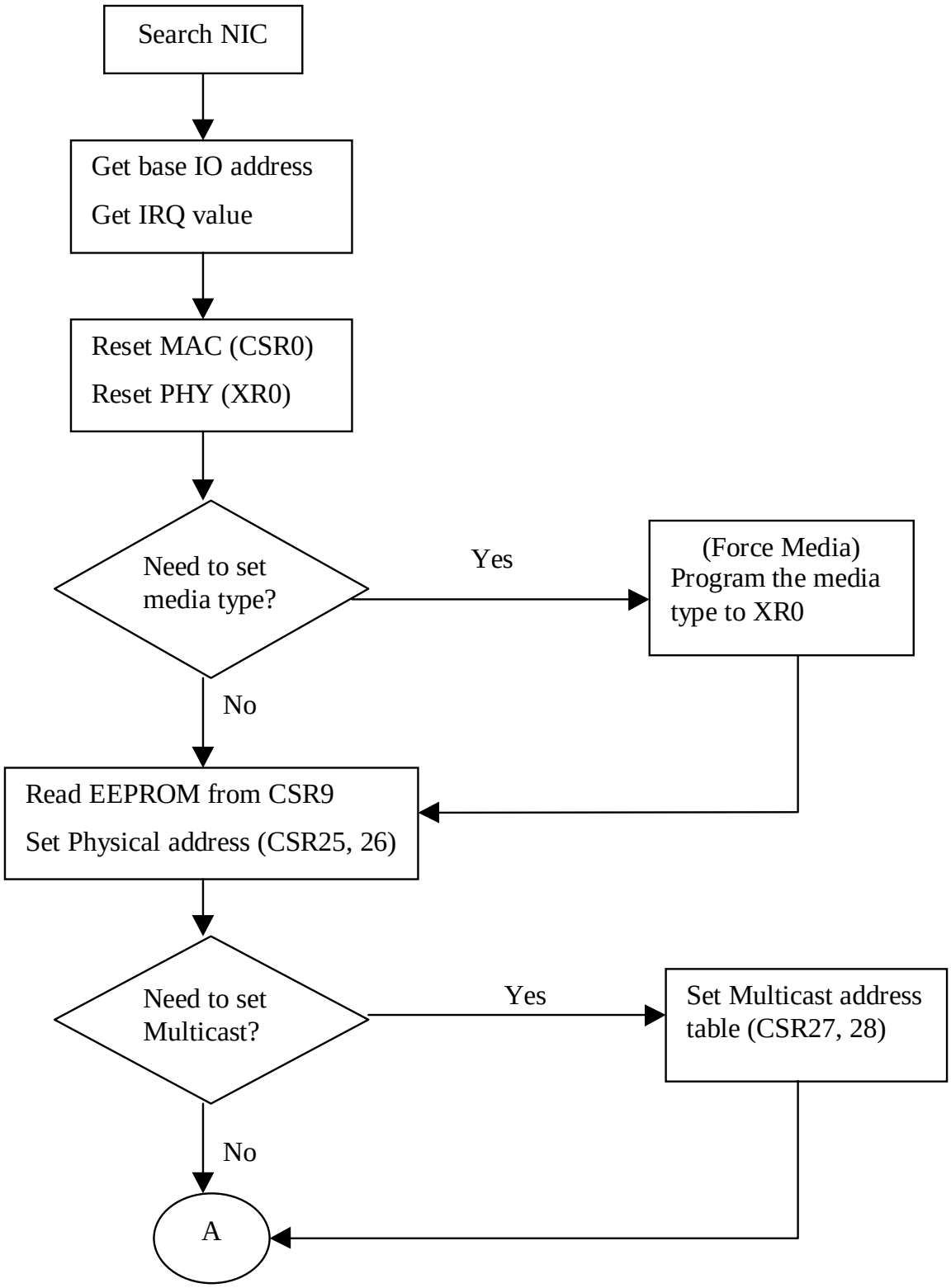
- Provides writable Flash ROM and EPROM as boot ROM with size up to 128kB
- Provides PCI to access boot ROM by byte, word, or double word
- Provides serial interface for read/write 93C46 EEPROM

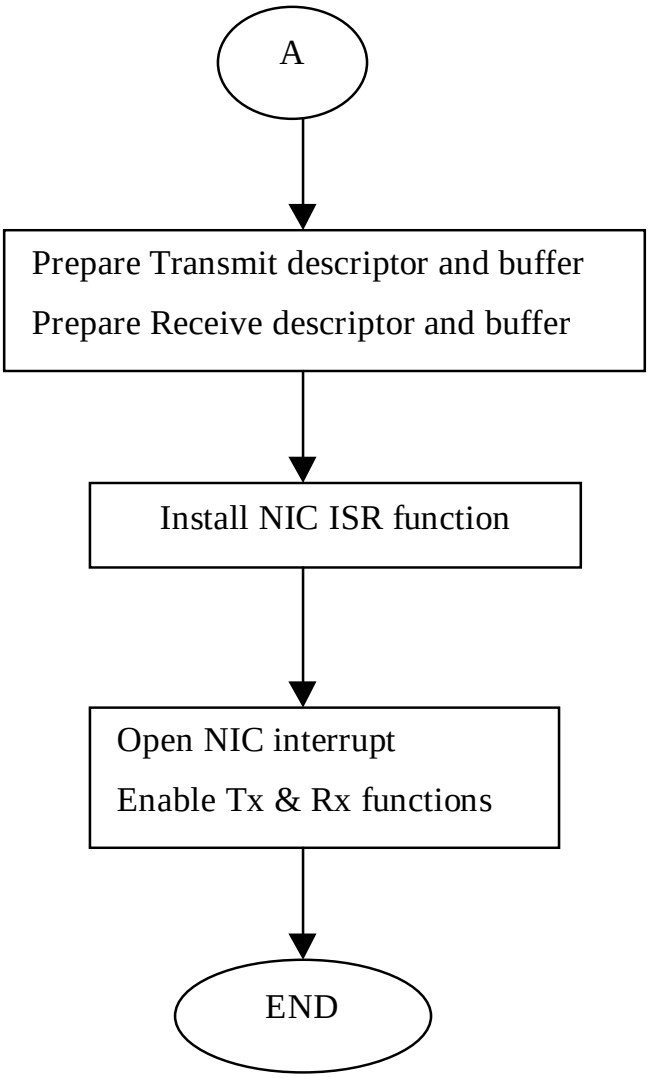
3.0 SOFTWARE PROGRAMMER'S GUIDE

STMicroelectronics supplies the drivers for the STE10/100A NIC for a wide variety of operating systems such as DOS, Win95/98/NT, Unix, Linux, VxWorks, and others. The software programmers guide is designed to help in understanding how the drivers work and/ or aid in the customer software development for the STE10/100A PCI faster Ethernet controller with integrated PHY.

3.1 Initialization Flow

STE10/100A supports the auto-configuration of Plug and Play. It will be automatically configured when placed in any system which supports Plug and Play and configuration management routines. Right after the system starts, Plug and Play will search for the NIC. The driver will query the resident configuration manager to obtain all necessary configuration information such as base IO and IRQ. The driver can obtain the base IO location using methods inherent in the specific driver specification being written to (such as NET.CFG files for ODI and PROTOCOL.INI files for NDIS drivers). Then, reset the MAC (through register CSR0) and PHY (through register XR0). Reset MAC is also called software reset - this ensures that all registers are initialized to their reset values even if a driver was previously run on the NIC. If a media type is need to be set, then force the media type through register XR0, otherwise go directly to read EEPROM, obtain the pre-assigned configuration resources, and set the physical address registers CSR25 and 26. If multicast needs to be set, then go to register CSR27 and 28 to set multicast address table. Otherwise build the transmit and receive descriptors (register CSR 3 and 4) and prepare the corresponding buffers. Then install NICs ISR (interrupt service routine) functions, and finally enable NICs interrupt (write enable bit to CSR17) and open NIC TX and RX functions (CSR6). The flow of initializing STE10/100A is shown as below:


Search NIC
Get base IO address
Get IRQ value
Reset MAC (CSR0)
Reset PHY (XR0)
Need to set media type?
Yes
(Force Media) Program the media type to XR0
No
Read EEPROM from CSR9
Set Physical address (CSR25, 26)
Need to set Multicast?
Yes
Set Multicast address table (CSR27, 28)
No
A

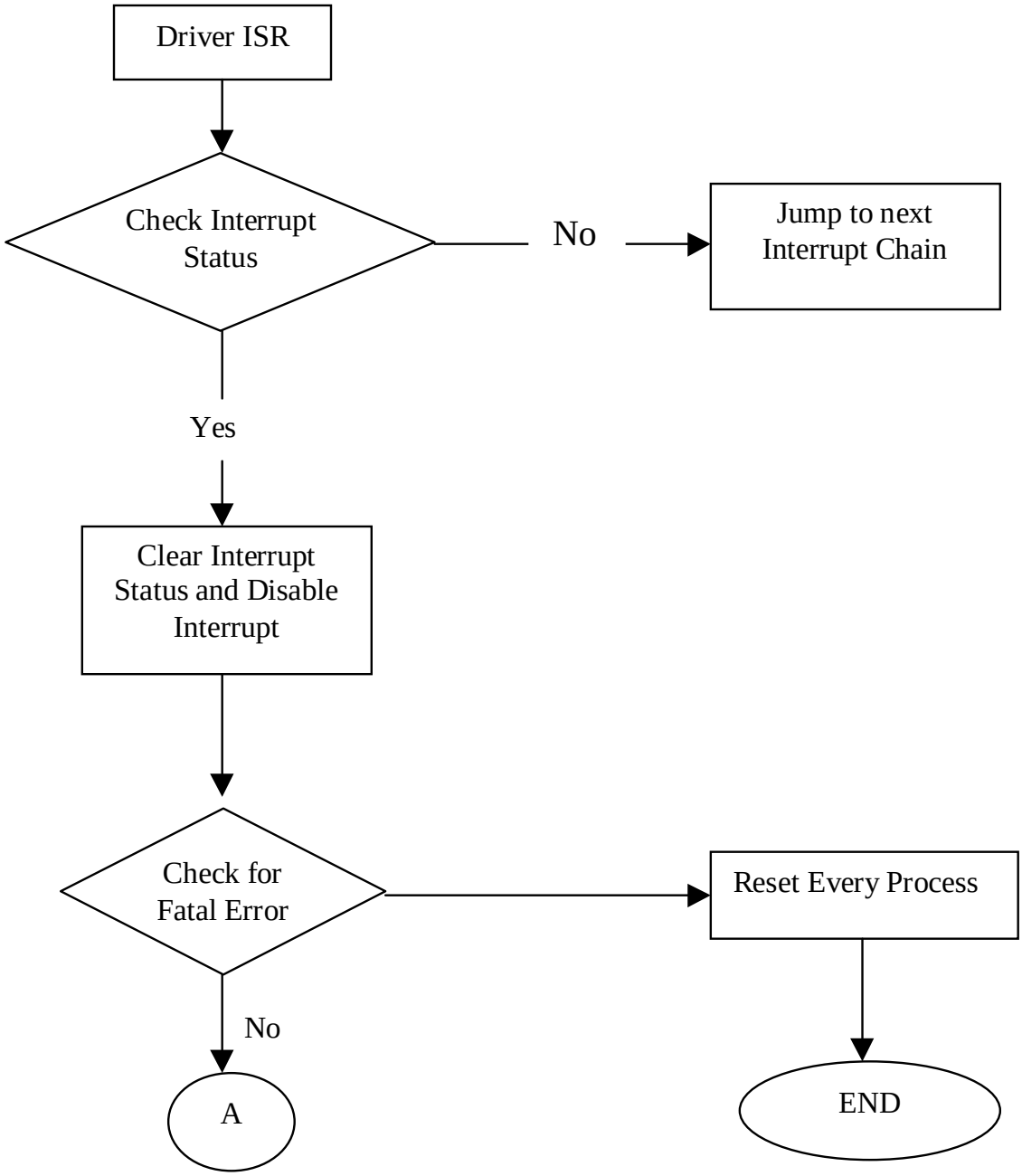


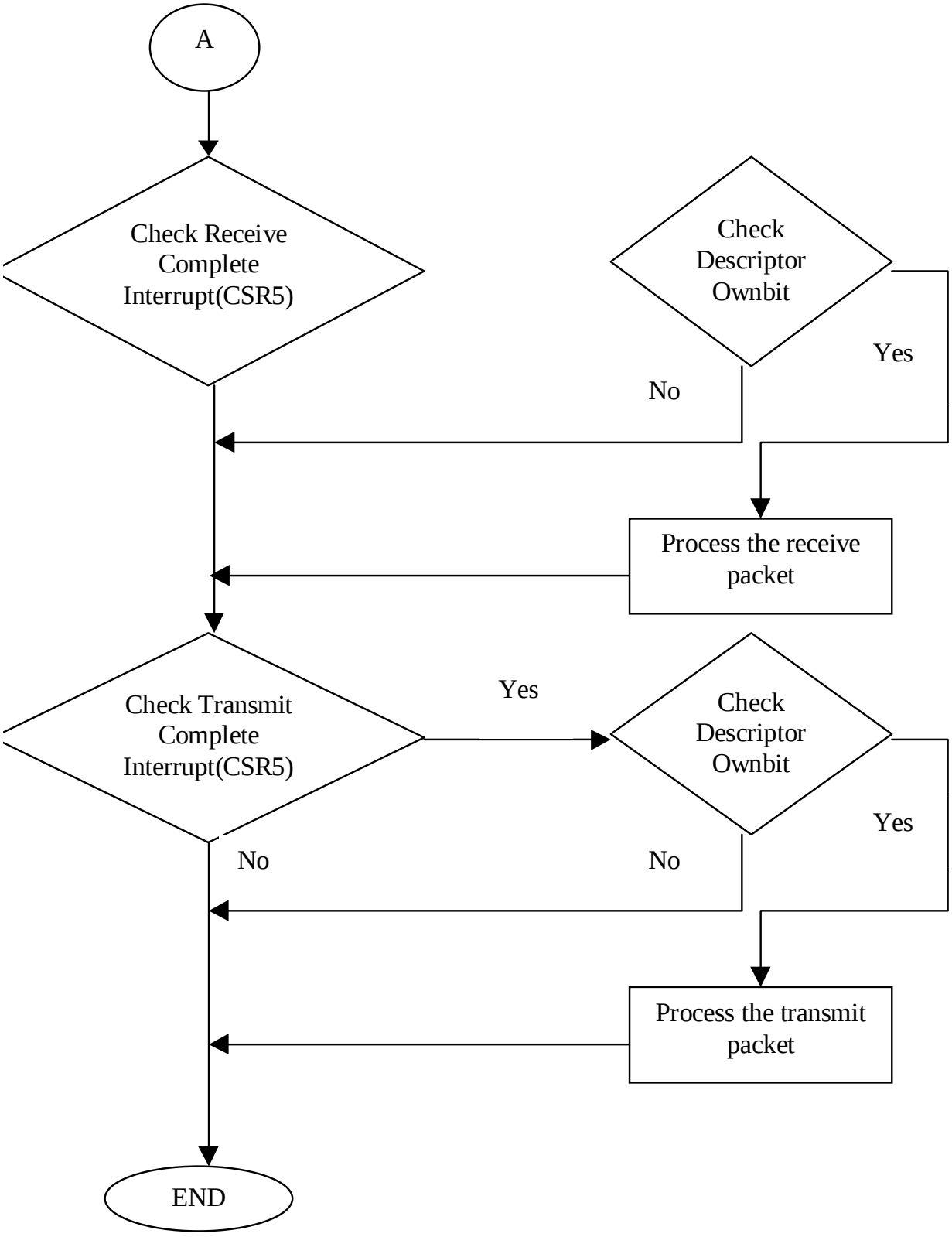
3.2 Interrupt Service Routine

The first thing to do in the interrupt service routine is to check the interrupt status (register CSR5 and CSR16) and confirm the interrupt. Then, disable the interrupt (CSR16) from the further interrupt while in the interrupt service routine. Then check for a fatal error by looking at register CSR5 bit13. If a fatal error occurs, check CSR16 to determine what type of error, and then reset all the processes and end the interrupt service routine. If no fatal error occurs, then go ahead to check receive and transmit complete interrupt (CSR5 bit6 and bit0). If one of the two bits is set, check the ownership bit in the descriptor. If the system owns the descriptor, then process the packet, otherwise, go to end of the interrupt service routine. Before exiting the interrupt service routine, the interrupts must be re-enabled.

For the TX and RX functions within the blocks of "Process the transmit packet" and "Process the receive packet" respectively, the STE10/100A provides an easy to use buffer architecture. As packets are received, they are stored sequentially in the 2 Kbyte receive FIFO. The driver need only perform a series of reads from a particular register to move the packet from the FIFO into system memory. Similarly, the driver needs to only perform a

series of writes to the same register in order to transmit a packet. This simplified buffer architecture enables the driver to implement streamlined data transfer routines. The flow chart of the interrupt service routine is shown as below:




A
Check Receive Complete Interrupt(CSR5)
Check Descriptor Ownbit
Yes
No
Process the receive packet
Check Transmit Complete Interrupt(CSR5)
Yes
Check Descriptor Ownbit
Yes
No
No
Process the transmit packet
END

4.0 MAC MODE AND MII INTERFACE

STE10/100A can be configured to operate in MAC mode and use Flash Boot ROM port as an MII port to control an external PHY device. There are two methods that can be used to program the Boot ROM pins as MII interface pins and put STE10/100A in the MAC mode. One method is from hardware configuration, the other is from software.

- To program the Boot ROM pins as MII interface pins from software, write 0x0024 to the test register "ctestr1" at address 0xfc.

When STE10/100A is configured to run in the MAC mode (Boot ROM pins programmed as MII interface pins), the multiplexed pins are defined as follows:

pin 56 = bra0/Mrxerr	pin 68 = brd1/Mrxd1
pin 57 = bra1/Mcol	pin 69 = brd2/Mrxd2
pin 58 = bra2/Mcrs	pin 70 = brd3/Mrxd3
pin 59 = bra3/Mdio	pin 71 = brd4/Mrxdv
pin 63 = bra6/Mtxd0	pin 78 = broe#/Txclk
pin 64 = bra7/Mtxd1	pin 79 = brwe#/Rxclk
pin 65 = bra8/Mtxd2	pin 80 = bra10/Mtxen
pin 66 = bra9/Mtxd3	pin 81 = bra11/Mdc
pin 67 = brd0/Mrxd0	

The register controlling the MDIO pin of the STE10/100A is CSR9 (offset = 0x48) and is implemented in the following manner:

- CSR9[19]: MII MDIO data in. Used by STE10/100A to read MDIO data from the PHY.
- CSR9[18]: MII MDIO operation mode. When CSR9[18]=1 the PHY is in a read operation mode. When CSR9[18]=0 the PHY is in a write operation mode.
- CSR9[17]: MII MDIO data write. Write MDIO data to PHY by writing 1 or 0 to this bit.
- CSR9[16]: MII data clock is an output signal MDC to the PHY.

5.0 PCB LAYOUT GUIDELINES

The goal of any complex mix-signal system design such as the one which includes both analog and digital functionality is to achieve the most robust system performance possible. Performance aspects such as SNR (signal to noise ratio), BER (bit-error-rate), EMI, and general signal integrity must be considered. The right combination of component placement, signal trace routing practices, and power supply/grounding distribution are part of a robust and reliable system. This section gives the guidelines that should be considered during designing a 10/100 Ethernet NIC when employing STE10/100A in conjunction with the common magnetics and RJ-45 connector.

5.1 Component Placement

Guidelines regarding optimal component placement practices include:

- Keep the distance between STE10/100A and the transformer, as well as the transformer and the RJ-45 connector as short as possible.

- Make sure the crystal device is close to STE10/100A pin x1 and x2, and stay away from the following items:
    - TX+/-, RX+/- differential pairs.
    - PCB edge.
    - Transformer.
    - Any other high frequency items and the associated traces.
- TX pull-up resistors, RX termination resistors and capacitors should be as close to STE10/100A as possible.
- The ferrite beads and decoupling capacitors should be placed as close to STE10/100A as possible, and the traces should be short.

5.2 Controlled Impedance of Signal Traces

It is important to incorporate controlled impedance routing for the signal traces which carry the 125Mbps serial bit stream. Standard micro-strip or strip-line techniques are recommended. It is important to choose an impedance of 50 for each trace that transports the 125Mbps signals between the RJ-45 connector and the transformer, and between the transformer and STE10/100A. This is necessary in order to match the 100 differential impedance of the unshielded twisted pair cable.

5.3 Signal Trace Routing

Some general guidelines regarding the optimal signal trace routing are listed as follows:

- Minimal length controlled impedance signal traces to minimize reflections and decrease noise sensitivities.
- Matched length differential signal traces to minimize jitter.
- Route trace corners at a radius >45 degrees.
- Minimized number of vias for any one given signal trace minimizes radiation.
- All controlled impedance traces routed directly over or under uninterrupted power or ground planes on adjacent layer(s) as this minimizes coupled noise into signal lines.

Some specific guidelines regarding STE10/100A NIC signal trace routing:

TX and RX signal trace routing:

- Avoid right angle on the signal traces. Whenever necessary the round angle or 45 degree angle is recommended.
- The trace width should be at least 2X the minimum unit of the layout program or wider than 8 mils.
- The length of the differential traces TX+ and TX- as well as RX+ and RX- should be equal and the total length of each signal trace should not be longer than 2cm.
- Keep TX and RX traces within the same signal plane and DO NOT use vias.
- The space between the differential traces TX+ and TX- as well as RX+ and RX- should be uniform and as close to each other as possible but not less than 8 mils.
- Keep the distance between the TX and RX differential pairs as far as possible - separate the ground planes underneath TX and RX signal pairs to reduce the cross talk.
- Keep the TX and RX traces away from the clock and power supply traces.
- Whenever possible, always put ground planes around the TX and RX traces.

- The digital signal traces should stay away from the analog signal and power supply traces. If impossible, traces should cross at 90 degrees with the analog signal and power supply routing at the other plane(s).
- Power supply traces should be short and it is always suggested to route them in the format of a plane. Ground should always be routed in the format of a plane.

6.0 NIC SCHEMATICS AND BOM

STMicroelectronics has the STE10/100A demo board available, and the demo board is a PCI bus NIC card. The NIC application design schematics can be found on the website at:

http://www.st.com/stonline/prodpres/dedicate/connect/datacom/ste10/ste10.htm

The corresponding bill of materials are as follows:

BILL OF MATERIALS

ITEM	QUANTITY	REFERENCE	PART
1	25	C1, C2, C3, C4, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C23, C25, C26, C30, C38, C39, C44	0.1UF
2	5	C5,C28,C29,C50,C51	22UF
3	2	C7,C6	22PF
4	2	C36,C37	10PF
5	1	C40	0.001UF
6	2	C42,C41	0.1UF
7	1	C43	1000PF
8	1	C45	0.01UF
9	3	D1,D2,D3	LED
10	1	JP1	HEADER
11	1	J1	RJ45
12	5	L1, L2, L3, L4, L5	BEAD
13	1	OSC	50MHZ
14	1	Q2	NDS352P
15	1	Q3	NDS351N
16	1	Q4	3904
17	1	R1	4.99K
18	3	R2, R3, R4	330
19	3	R5, R22, R40	0
20	1	R6	33
21	2	R9, R14	20K
22	2	R10, R11	5.1K
23	1	R1	2.2K
24	1	R13	4.99K
25	2	R21, R20	50
26	1	R26	100
27	3	R28, R30, R34	49.9
28	2	R33, R32	75
29	1	R36	133K
30	1	R38	4.7K
31	2	R41, R39	10K
32	1	U1	32PIN
33	1	U2	PCISLOT_0
34	1	U3	93C46
35	1	U4	STE10/100A
36	1	U5	LM393M
37	1	U7	HB626-1 (Transpower)
38	1	U8	74VHC123A
39	1	U9	3.3V REG
40	1	X1	25M

7.0 CONCLUSION

STMicroelectronics provides a complete solution with its STE10/100A chipset that comes with reference design hardware/software packages that allow manufacturers to quickly design easy and cost-effective applications. The design package includes:

- Demo Board (PCI bus NIC card)
- NIC applications design schematics
- Gerber files
- Bill of materials
- Detailed datasheet and documentation.

The testing results show that STE10/100A has great performance and all the implemented functions meet or are better than the requirements specified by the IEEE standard draft.

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