AN1266
APPLICATION NOTE

Benchmarking Flash NOR and Flash NAND memories for Code and Data Storage

CONTENTS

INTRODUCTIOM

When choosing a Flash memory for a particular application it is important to know which type of Flash Memory is most suitable. There are now many manufacturers offering a wide range of Flash Memories and users can be daunted by the prospect of selecting the correct product for their application.

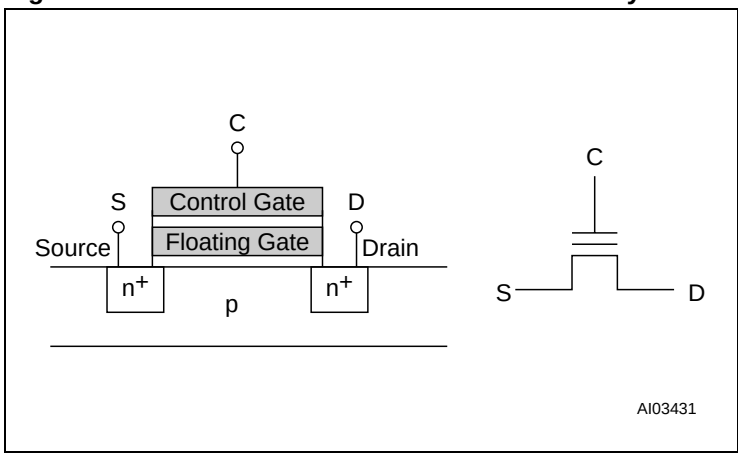
This document aims to give a background on the underlying technologies associated with Flash Memories. It will give the reader a clearer picture of which *type* of Flash Memory to choose for their application. The advantages and disadvantages of each type of memory is discussed along with the underlying principles that govern the properties of the memory.

There are two fundamental Array Architecture that distinguish the type of the Flash Memory, NOR and NAND. Although both these types of memories can store large amounts of data, only the NOR type is suitable for fast random access required for executing code directly from the Flash Memory, saving on shadow RAM costs.

CELL STRUCTURE

The Basic Cell in a Flash Memory is a single MOS transistor built with a Floating Gate between the control gate and the p-substrate. Figure 1 shows a typical cross section of the transistor.

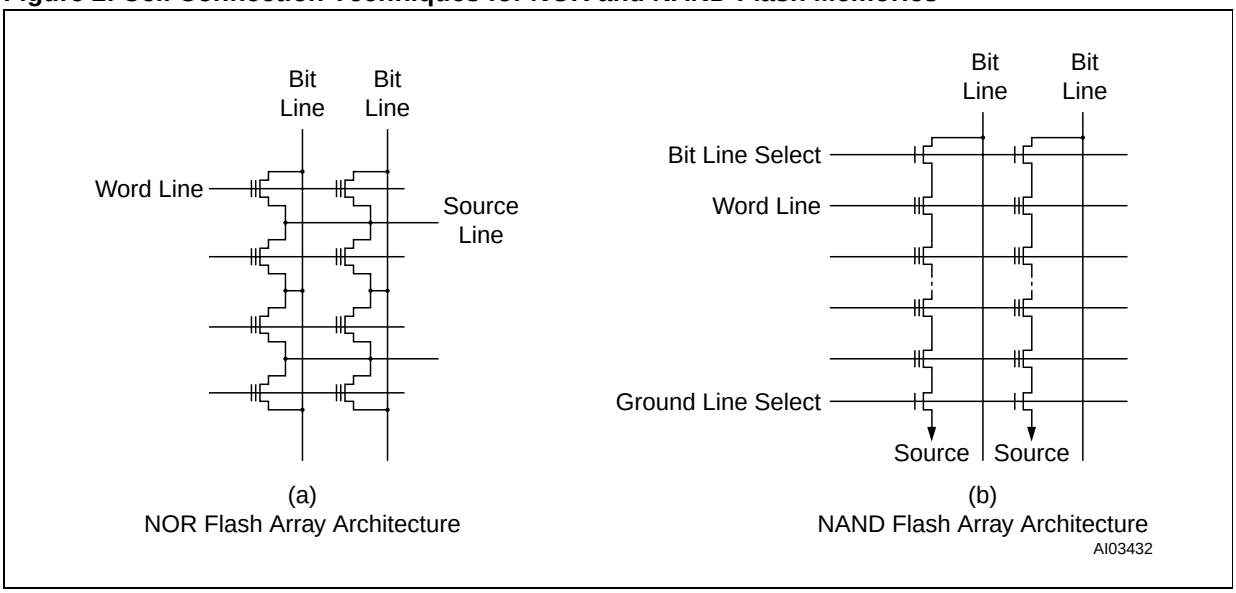
Figure 1. Cross section of the basic Flash Memory Cell



The Floating Gate stores charge (electrons); the amount of charge on the gate determines whether the Flash Memory cell holds a value of '1' or '0'. (In Multi-Bit Cells more than one bit can be stored, this is discussed later). To read the contents of the cell a voltage is placed across CS; the current through DS depends on the charge stored in the Floating Gate. By measuring I_{DS} the charge in the Floating Gate is found.

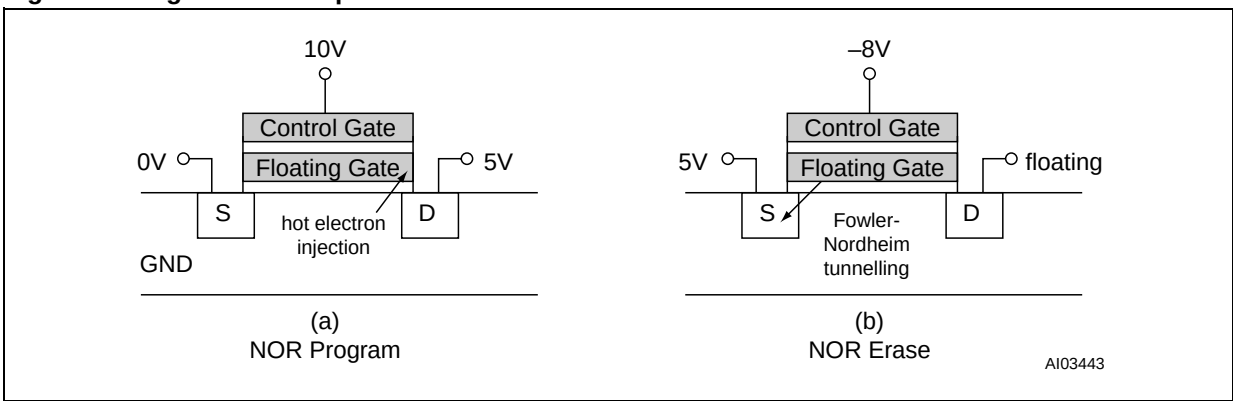
There are various methods of laying out all of the Floating Gate transistors and connecting C, D and S in a Flash Memory array. Figure 2 shows the connection technique for NOR and NAND Flash Memories.

Figure 2. Cell Connection Techniques for NOR and NAND Flash Memories



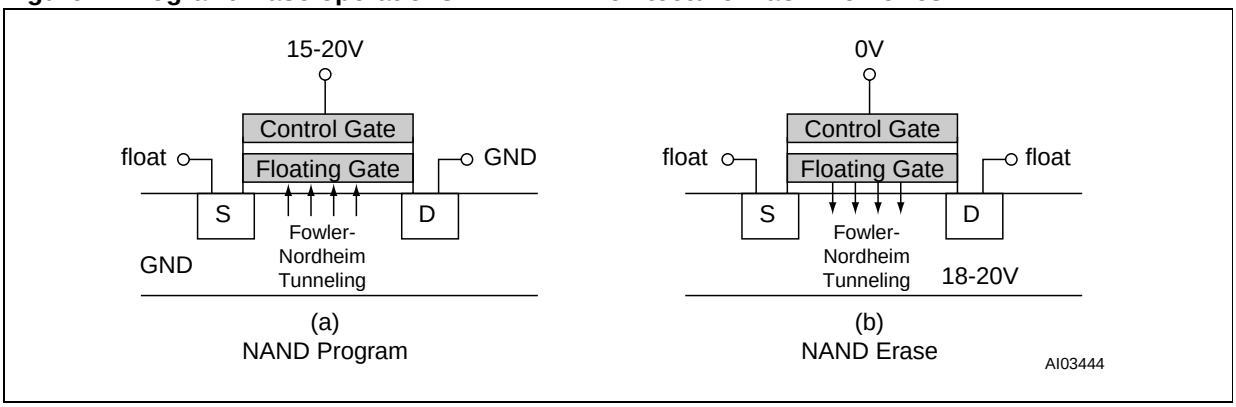
In the NOR architecture a read is performed by connecting the Source Line to ground, raising the voltage level on the Word Line to the sense voltage and connecting the Bit Line to the sense amplifier. If the addressed cell is programmed then no current flows through the Bit Line to the sense amplifier. 8, 16, 32 or more bits are read in parallel depending on the data bus width of the memory. Programming a '0' to the cell is performed by simultaneously pulsing the Bit Line with 5V and the Word Line with 10V; the Program/Erase Controller may have to apply several pulses to program the cell to the correct level. All the cells in a block are erased at the same time; to erase a positive voltage (5V) is put on the Source Line and a negative voltage (-8V) is pulsed on the Word Line; again several pulses may be required to erase all the cells correctly.

Figure 3. Program/Erase operations in NOR Architecture Flash Memories



In the NAND architecture a read is performed by connecting the Source Line to ground, raising the voltage level on the Word Line to the sense voltage, turning on the correct group of cells using the Bit Line Select and connecting the Bit Line to the sense amplifier. The Word Lines of all the other cells in the group are left set to ensure that the cells are in their 'ON' state; only the current in the selected state governs the current in the Bit Line, enabling that cell's contents to be read. Reading a current through a series of several cells and select transistors is a slow operation; the random access time is typically 25µs. To program individual cells the Word Line is driven to a very high voltage (15 to 20V) and the Bit Line is connected to ground (0V); the unselected cells have to pass the programming current without being affected themselves. To erase a sector the Word Lines of the sector are driven to ground (0V) and the p-well of the sector is driven to a very high voltage (15 to 20V).

Figure 4. Program/Erase operations in NAND Architecture Flash Memories

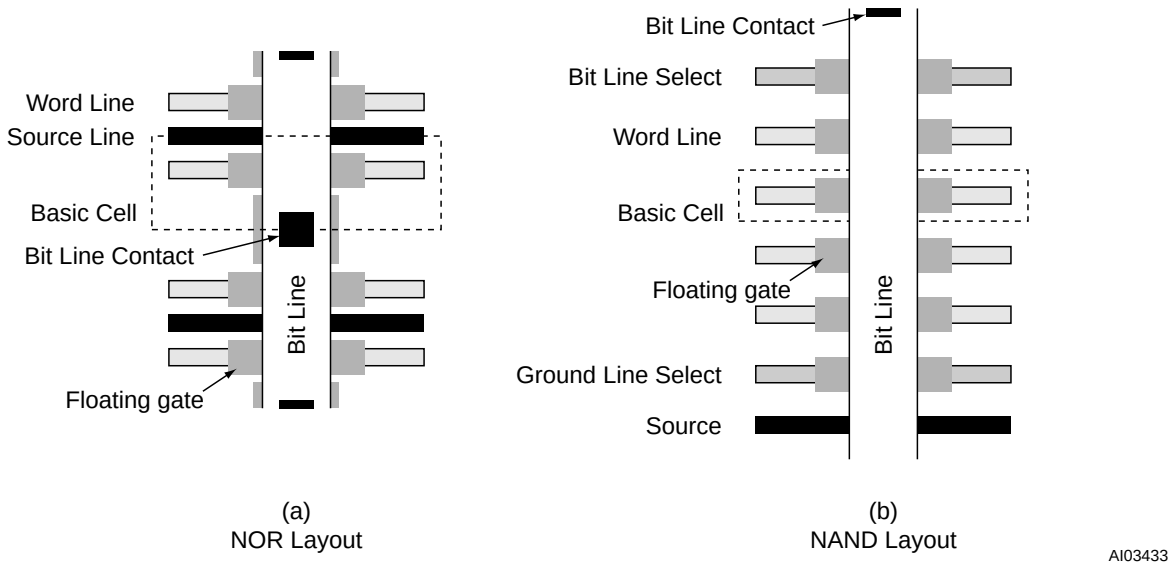


The higher voltage required in the NAND architecture makes the voltage pumps in the silicon more difficult to design. The management, distribution and switching of these higher voltages is also more difficult. With 0.25µ technology this has not been a limiting factor, but as the technology shrinks the electric fields inside the silicon increase, making it more and more difficult to route the signals through NAND devices. Although the Flash Array is smaller in NAND, the voltage pumps and associated electronics are larger.

CELL DIMENSIONS

When the array is laid out on the silicon wafer there are limitations to the size that each cell can be squashed into. Here the NAND architecture has an advantage over NOR. Figure 5 shows typical layouts for NOR and NAND Flash Memories.

Figure 5. Typical Layouts of NOR and NAND Flash Memories

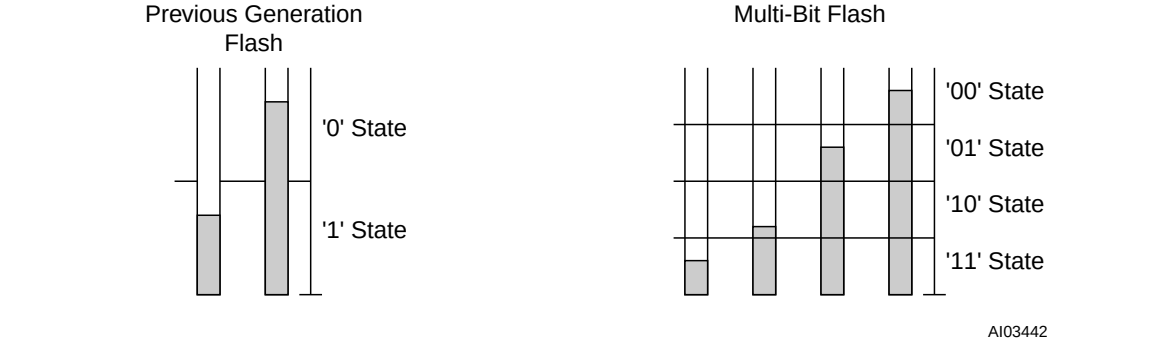


The silicon area required for the Basic Cell in the NOR configuration is $10F^2$ (where F is the feature size, related to the technology used e.g. 0.18µ, 0.15µ etc.); the cell size is limited by the contact to gate distance. The NAND has a smaller configuration, requiring only $6F^2$, thereby allowing a greater theoretical density of cells for a given technology. However, the decoder area for NAND configurations is much larger than that in NOR configurations, as are the charge pumps; when considering the density as number of cells to the overall Flash memory size, the difference between the two types of configuration is not clear cut in favor of NAND (see Reference [1]).

MULTI-BIT CELLS

The Basic Cell in a Flash Memory can hold different charge levels (quantized only by the charge on a single electron), giving rise to the possibility of storing more than one bit of information in each Basic Cell. Figure 6 shows the charge level possibilities for a traditional, previous generation Flash Memory and the levels for a 2-bit per cell Multi-Bit Flash Memory. The amount of charge stored determines I_{DS} when the cell is read.

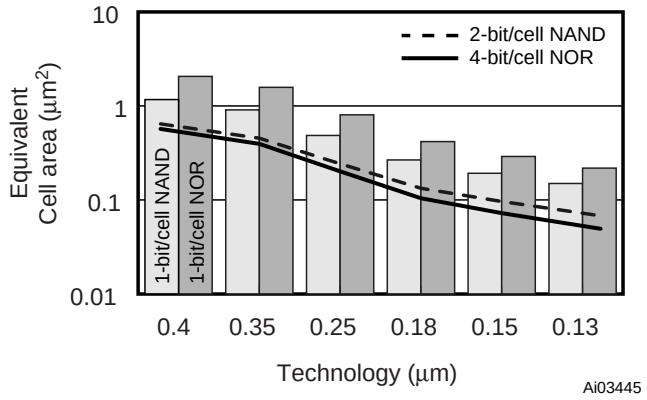
Figure 6. Floating Gate Charge Levels and Output States



NOR architectures have an advantage over NAND in Multi-Bit Cell Flash Memories and are likely to achieve a higher number of bits per cell compared to NAND in the long term. In the NOR architecture the Sense Amplifiers have direct access the each cell. In the NAND architecture the Sense Amplifier's signal is read through several other cells; the charge stored in the "read-through" cells makes small, but significant differences to the value read, decreasing the accuracy. This makes it likely that four bits per cell cannot be achieved in NAND architectures.

Four bits per cell will allow NOR technology to make up the economic difference (in $/Mbyte) lost due to the large cell size. NAND parts with 2-bits per cell are being designed for release towards the end of the year 2000. NOR parts with 2-bits per cell are already being shipped and 4-bits per cell are planned for late in 2001.

Figure 7. NOR/NAND Equivalent Cell Size considering Multi-Bit Cell Technology



OPERATIONAL DIFFERENCES

There are differences in the way that NOR and NAND memories behave at a system level. Table 1 at the end of this section summarizes the operational differences.

Block, Sector and Page Architecture

Flash Memories cannot erase one byte at a time. It is necessary to divide the memory into blocks (or sectors) of cells that can be erased together. If there is some information stored in the block when the block needs to be erased, it must be moved to another block prior to erasing, otherwise it will be lost. NOR memories offer block sizes between 16 Kbytes and 128 Kbytes. NAND memories offer sector sizes between 8 Kbytes and 16 Kbytes. (The meaning of the word block and sector is the same, different suppliers use different terminology).

The page concept is different for NOR and NAND memories. NOR memories with page-mode group up to four addresses in the same page; these four addresses take longer for the first access compared to the subsequent accesses within the same page, often it is referred to as "page-mode".

In NAND memories each sector is sub-divided into pages, usually about 512 bytes long. The read access time inside the page is fast, whereas jumping to another page is slow. Each page should be programmed as a whole too.

Read Access

NOR Flash Memories offer random access. Parts with access times down to 35ns are available. Page-mode memories are available that offer 150ns access for the first page access and 20ns for the subsequent accesses in the page. Burst interfaces allowing bus speeds up to 66Mhz allow NOR memories to be interfaced to a variety of Burst Mode microprocessors.

NAND Flash Memories offer fast access times for sequential reads from within the same page in the memory. The first access to memory in the page typically takes 25µs, with subsequent accesses taking typically 50ns until the end of the page is reached.

Programming

NOR Flash Memories can be programmed in random order, with each program operation taking approximately 10µs per byte or word. Multi-Bit Cell memories take longer to program, but include a Program Buffer that allows parallel programming of many bytes or words, keeping the program rate per word at about 10µs. In the future Multi-Bit Cell NOR Flash Memories will include larger program buffers to reduce the burden on the CPU and decrease the programming time per byte to less than 2µs.

NAND Flash Memories program one page at a time; single byte programming is not possible. A page programs in approximately 200µs and is usually about 512 (or 528) bytes long. The programming rate is about 0.5µs per byte. Multi-Bit Cell NAND Flash Memories take longer to program, approximately 900µs per page or 2µs per byte.

Erase

NOR Flash Memories have block sizes between 16 Kbytes and 128 Kbytes. Typically a 64 Kbyte block takes about 0.7s to erase. The long erase time is due to the need to program each cell in the block to '0' before erasing the cells; this operation is required to guarantee that the charge in all the Floating Gates is the same before the erase operation begins. In modern Flash Memories the Program/Erase Controller manages this process automatically so that the microprocessor can perform other tasks during the erase cycle.

NAND Flash Memories typically have block sizes of 16 Kbytes; these take about 2ms to erase. NAND Flash Memories do not need to preprogram all their Floating Gates to the same level prior to erasing.

Valid Blocks

In NOR Flash Memories 100% of the array is guaranteed to work for a full 100,000 program/erase cycles. After 100,000 cycles the probability of a cell failing is still very small. The benefits of having an array that is 100% guaranteed is:

- Storage Algorithms do not need to store information on "bad blocks", saving space and algorithm development.
- Code can be executed directly from the memory, either for boot purposes (for example in PC systems where the BIOS is in Flash, then is shadowed in RAM) or for both boot and application execution (for example in PDAs where cost and power savings are achieved by executing directly from the Flash and the amount of RAM required is reduced).

In NAND Flash Memories not all of the blocks are guaranteed to work. Typically 98% or more of the Flash Memory is guaranteed. Furthermore it is possible for blocks to fail in service, these too need to be marked as "bad". NAND Flash Memories offer 250,000 program/erase cycles, but these are not guaranteed in the same way as NOR Flash.

Table 1. Operational Difference Summary

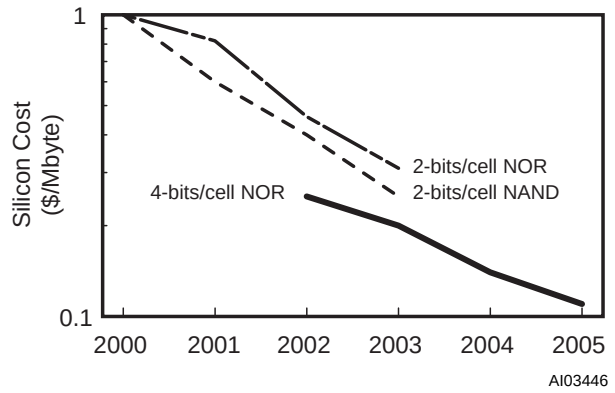
Operation	NOR	NAND	Summary
Random Read	35 to 150ns	25µs	NOR – true random access. NAND – slow page selection Time.
Sequential Read	20 to 150ns	50ns	NOR – true random access. NAND – page read from buffer.
Program Time	5µs/byte random	0.5µs/byte sequential only	NOR – true random programming. NAND – page or sequential partial page programming.
Erase Time	0.7 s/128 Kbyte	2 ms/16 Kbyte	NOR – Internally the Flash has to program all cells first. NAND – Quick erase operations.
Array Good	100%	98%	NOR – All addresses are guaranteed good NAND – Bad Blocks cannot be used to store data
Endurance	100,000 with no cell failures	250,000 with some block failures	NOR – 100% of the array is guaranteed good after 100,00 cycles. NAND – Some additional failures can be expected.

COST TRENDS

Until 4-bit per cell NOR Flash Memory becomes available the basic cost of 2-bit per cell NAND memories is slightly less than that of 2-bit per cell NOR. Figure 8 compares the cost trends for the 2-bit per cell architectures, also shown is the predicted cost of 4-bit per cell NOR technology.

At a system level the cost difference between NOR and NAND is not as wide as the graph suggests. Many applications that make use of NAND devices require additional controller chips, whereas there are NOR Flash Memories that are compatible with most microprocessor buses. Flash Memory has become more common than EPROM for boot devices; only NOR Flash Memory offers boot capability. Furthermore the same Flash part can be used for application storage and execution. Many systems require only one Flash Memory for boot code, application code and user data, vastly reducing system costs.

Figure 8. Cost Trends for Multi-Bit Cell Flash Memories



CONCLUSION

The difference in cell size between NOR and NAND Flash Memories will be compensated for when 4-bits per cell NOR Flash Memories become available, turning NOR technology into the most cost-effective storage solution for all applications. The other advantages of NOR Flash Memories, such as being able to execute code directly from the Flash Memory, further enhance the cost-effectiveness of the technology. Finally, flexible bus interfaces such as Burst Mode, Page Mode, and Multiplexed Buses make NOR Flash Memories the easiest type of memory for all current and future applications.

REFERENCES

[1] P. Cappelletti, C. Golla, P. Olivo and E. Zanoni, “Flash Memories”, Kluwer Academic Publishers, 1999.

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.

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