AN1265
APPLICATION NOTE

Highlighting the Advanced Features of the M58LW064 family of Flash Memories

CONTENTS

INTRODUCTION

The M58LW064 is the first in a new family of leading-edge Flash Memories from ST Microelectronics with many advanced features to suit today's and tomorrow's demanding products. Incorporating new multi-bit cell technology, 32-bit burst bus access and write buffers along side standard Flash Memory features the family represents a new generation in the advance of Flash Memory technology.

This application note is intended for use by design engineers who are already familiar with current Flash Memories and are keen to familiarize themselves with this next advance.

PRODUCT FAMILY DISTINCTIVE CHARACTERISTICS

This new family of Flash Memories combines several key features that distinguish it from previous generation Flash Memories. These features are aimed at reducing cost in future designs by increasing the size of the Flash Memory array and reducing the number of components in a system. A brief overview of each feature is presented here, with more depth being described later on.

Multi-bit Cell Technology. Each cell in the Flash Memory can be programmed to more than two distinct logic levels, giving rise to the concept of multi-bit cells that store more than one bit per cell. A memory that uses this technology can store twice as many bits in the same size array of transistors, in the future four times as many bits are planned. This will halve or quarter the cost of the memory per bit.

32-bit Burst Access. Many microprocessors incorporate burst access busses in order to increase the through-put of data whilst decreasing the power consumption. By providing a Burst Read operation in the Flash Memory it is possible to interface the Flash Memory to microprocessors directly (as apposed to shadowing the contents in SDRAM), decreasing power and maintaining fast access. The amount of SDRAM can be reduced considerably since it is no longer necessary to have as much, thus saving cost in the product. Furthermore, the M58LWxxx family is available with 32-bit bus access, giving even higher bandwidth access compared to previous 8-bit and 16-bit Flash Memories.

Page Mode. For microprocessors without Burst Read operations the memory supports faster access for accesses to ad-

dresses within the same page. The first access to the page results in an access time equivalent to the normal random access time, further accesses to the same page are performed very much faster.

Write Buffers. Up to 16 Words can be submitted at a time for programming (4 Words minimum). This feature both speeds up the programming time in the Flash Memory and frees up the microprocessor to do other work whilst programming.

Code Plus Data Storage. The size of the memory array in the M58LWxxx family will make it one of the first memories that can be used to store both an application's code and data on a single part. Most of today's portable applications require between 2 Mbytes and 4 Mbytes for their application code, with users demanding at least 4 Mbytes of data space (about 30 photo-quality digital pictures). With 8 Mbytes available in the smallest family member there is space for both all the required code (both application and operating system) and user's data.

The development of the M58LWxxx Family will continue over the next few years with sizes doubling each year. With 4 bits per cell expected in 2002/3 the size will quadruple. Table 1 shows the roadmap planned for the product family.

Table 1. M58LWxxx Family Roadmap

Family	M58LW032A/B	M58LW064A/B	M58LW128A/B	M58LW256A/B	M58LW512A/B
Lithography	0.18µ	0.18µ	0.18µ	0.15µ	0.13µ
Density	32 Mbit	64 Mbit	128 Mbit	256 Mbit	512 Mbit / 1 Gbit
Organization	2 Mb x16 1 Mb x32	4 Mb x16 2 Mb x32	8 Mb x16 4 Mb x32	16 Mb x16 8 Mb x32	32 Mb x16 16 Mb x32
Supply Voltage	2.7 to 3.6V	2.7 to 3.6V	2.7 to 3.6V	2.7 to 3.6V	1.8 to 3.6V
Multi-bit Cell	2 bits per cell	2 bits per cell	2 bits per cell	2 bits per cell	2 or 4 bits per cell

APPLICATIONS AND PRODUCTS

The application areas that will benefit the most from this advance in Flash Memory are mainly consumer products that require low power, low cost and large storage. Some of the target products are:

- Digital Set-top Boxes
- Phones incorporating Web Browsers and Email
- Digital Still Cameras
- Hand-help Applications, Personal Digital Assistants (PDAs)

The family fits into very competitive market places where consumers are very conscious of both price, storage capacity and power consumption. The M58LWxxx family makes an exceptional product for this market area since it satisfies and exceeds all of the market requirements. When designed into future systems further savings can be made to power and price by reducing or removing the SDRAM requirements.

Other applications that are very demanding on Flash Memories include GPS, Networking Products, Computer Games and Printers. The M58LWxxx offers a clear advantage over previous generation Flash Memories in each of these areas.

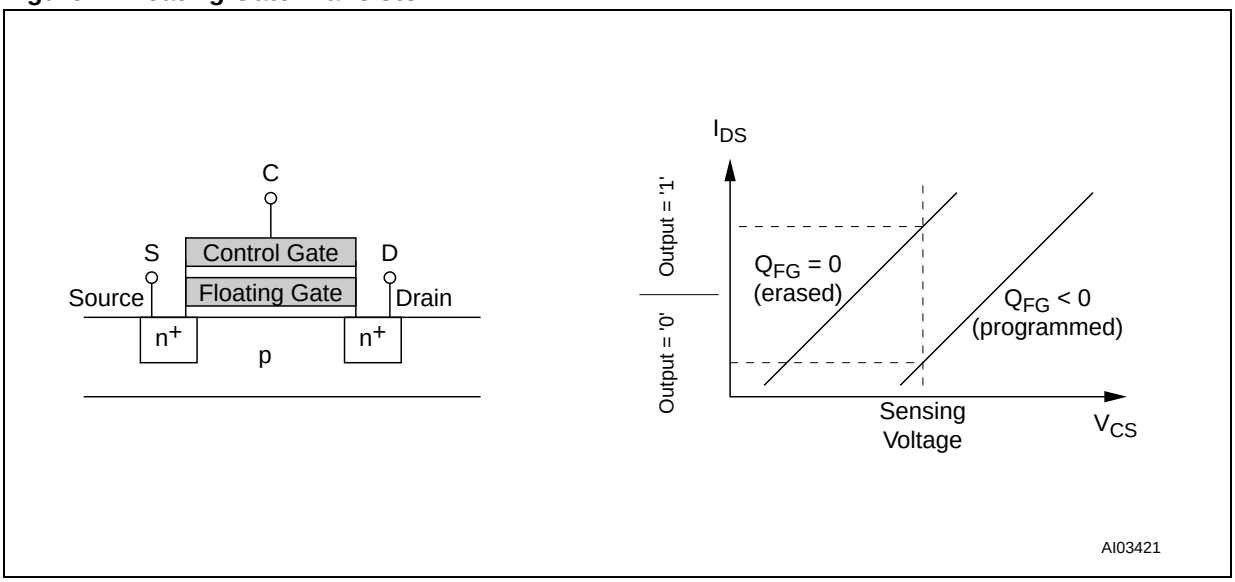
ADVANCED FEATURES

To fully understand the benefits that the advanced features provide it is useful to have an in-depth understanding of the technology and some examples of their use. This next section elaborates on the overview given previously.

Multi-bit Cells Technology

The Floating Gate Transistor that forms the basis of Flash Memories works by storing charge on the Floating Gate. Figure 1 shows an example of the Floating Gate Transistor. The amount of charge stored in the Floating Gate affects the current in the transistor for a given Control Gate voltage. When the Floating Gate is programmed and the Control Gate voltage is set to the Sensing Voltage only a small amount of current flows through the transistor; when the Floating Gate is erased a higher current flows through the transistor.

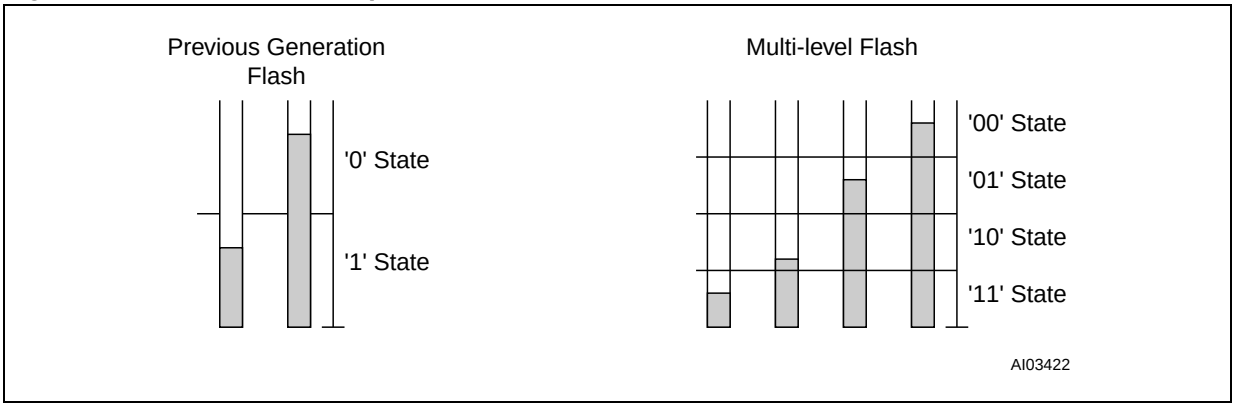
Figure 1. Floating Gate Transistor



It follows that by partially programming the Floating Gate with a different charge level it is possible to store more than just two states. If 4 distinct levels can be programmed then each transistor cell can store 2 bits; if 16 distinct levels can be programmed then each transistor cell can store 4 bits. Figure 2 shows examples for one and two bits per cell.

The state of each cell is determined by comparing the output current level with proper thresholds to see which band the level is in. The more bits that are stored in each cell, the more thresholds are needed and the more accurate the comparison needs to be.

Figure 2. Cell Levels and Output States



Programming Multi-bit Cells requires more accuracy than programming previous generation Flash since care must be taken to ensure that the Floating Gate contains the correct number of electrons for the intended state. The injection of electrons into the Floating Gate is finely tuned by applying a large number of small pulses on the gate of the cell (up to 20 for a 2-bit cell). Consequently the programming time for Multi-bit Cells is considerably longer. To achieve comparable programming speeds to previous generation Flash several words can be programmed simultaneously through the Write Buffer, resulting in a programming time typically under 200µs for 16 Words (equivalent to about 12µs per Word).

32-Bit Burst Access

The M58LWxxx family Burst Read operations support high synchronous data transfer rates, automatic internal address increment, microprocessor controlled Burst Lengths and are compatible with Burst Mode microprocessors. A Burst Read operation involves specifying a start address and then clocking the data from successive addresses with a synchronous clock; special addressing schemes also exist to interleave the addresses as required by some microprocessors. Burst Read operations allow faster access to sequential memory contents than random access operations. For example, using the M58LW064 with a 33MHz clock the first data read during a Burst Read operation appears at least 7 clock cycles after the beginning of the Burst Read operation and subsequent data can be read one every following clock cycle (30ns).

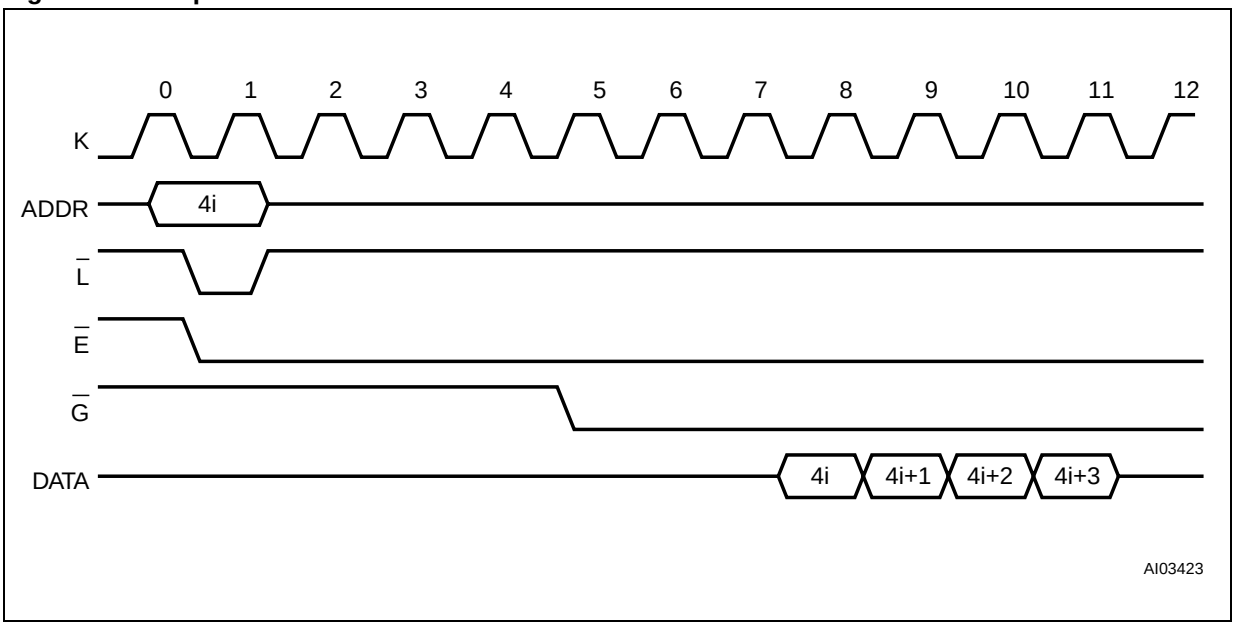
Registers inside the Flash can be used to configure various parameters about the Burst Read operation. On reset the memory reverts to its asynchronous mode and, until the registers are set, Burst Read operations cannot be performed. The microprocessor may boot from the Flash Memory, but only in asynchronous mode. The registers in the Flash configure the Burst Length, Burst Type and Burst Latency.

The Burst Length is the number of data reads (either 16 or 32 bits) that can be read; lengths of 1, 2 and 4 (and 8 for 16 bit data busses) can be selected, or continuous burst reads may be used. When a Burst Length is selected (opposed to continuous) the memory will cycle the address through the page containing the start address. For example if a start address of 3 is specified and the Burst Length is 2 then continuous reads will read addresses 3, 4, 3, 4... until a new start address is specified by a new Burst Read operation. In continuous mode the whole memory can be read and the address will wrap from the top address to the bottom address.

The Burst Type defines whether the addresses are read sequentially or are interleaved. Some microprocessors require interleaved read sequences and the memory can be fully configured to support these microprocessors.

The Burst Latency configures the number of clock cycles before the memory will make the first and subsequent data available on the data bus. Both the microprocessor and the memory need to be configured to have the same Burst Latency, otherwise the data will be read from the wrong addresses. The Burst Latency is specified as X.Y.Y.Y where X is the initial number of clock cycles before the first data can be read and Y is the number of clock cycles before subsequent data can be read. Burst Latency X can be configured from 7 to 16 and Y can be configured to either 1 or 2. (Zero wait-state would be represented by 2.1.1.1). For each clock speed the Burst Performance Table in the Data Sheet specifies the fastest configuration that can be achieved and either this or slower configurations must be used.

Figure 3. Example of 8-1-1-1 Burst Transfer

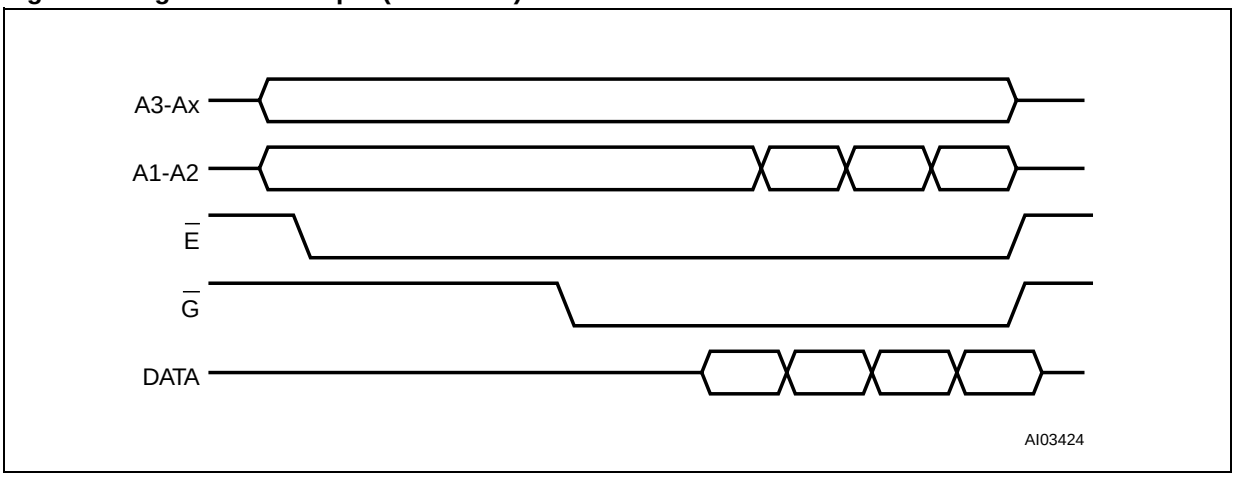


Page Read

Microprocessors that do not support Burst Read operations may still be able to take advantage of fast access by using the Page Read feature of the M58LWxxx family. In a Page Read operation the first Bus Read operation in the page takes the full access time, subsequent Bus Read operations from the same page take considerably less time. For the M58LWxxx family a page is 4 Words in x16 mode or 2 Double Words in x32 mode, i.e. all of the Address Bits from A3 upwards must remain constant, only A2 (and A1 in x16 mode) may change.

Figure 4 shows an example of a Page Read operation. The first address takes longer to reach the Data Bus than the subsequent Page Read operations.

Figure 4. Page Read Example (x16 mode)



Write Buffer

The Write Buffer allows the microprocessor to program from 4 to 16 Words (or from 2 to 8 Double Words) in parallel, both speeding up the programming and freeing up the microprocessor to perform other work.

The minimum buffer size for a program operation is a 4 Word (or 2 Double Word) page. Inside the page the 4 Words are selected by addresses A2 and A1. Any attempt to program a single word (or Double Word) inside the page of a previously erased block will result in the programming of the Word, however all other Words inside the page will be set to FFFFh.

For any page, only one Write to Buffer and Program Command can be issued inside a previously erased block. Any further program operations on that page must be preceeded by an erase operation on the respective block.

As already discussed, each Multi-bit Cell takes longer to program than traditional single bit cells. Using the Write Buffer 16 Words can be programmed concurrently, without intervention from the microprocessor. Internal algorithms for parallel programming result in a speed increase of about 20 times, giving a programming time per Word of about 12µs, similar to one bit per cell Flash.

The additional benefit of the Word Buffer is it allows the microprocessor to perform other work in between servicing the Flash Memory. In order to service the Flash Memory every 10µs the microprocessor is unable to perform very many other functions. Context switches where the microprocessor changes from one task to the next generally take about 2 to 5µs and a CPU attempting to schedule fast flash programming will spend most of its time performing context switches and not getting any work done. With the Write Buffer the Flash only needs servicing approximately every 200µs. While this is still fast, it is well within the reach of most microprocessors and allows far more CPU time to be dedicated to other tasks, leaving the programming of the Flash Memory as a background task.

STANDARD FEATURES

Along with the Advanced Features introduced with this Flash Family are the Standard Features that users have come to expect with modern Flash Memories. For example, the part includes the Common Flash Interface, Software Read-while-Write and Block Protection. The Flash is based on the highly efficient and reliable NOR technology. Many of the Standard Features are highlighted in the Benchmarking section, the more advanced ones are described in detail here.

Common Flash Interface (CFI). Software standards are needed to make Flash Memories interchangeable and to encourage adoption of new flash technologies. Toward this end, Intel, AMD, Fujitsu, Sharp and other leading Corporations promote the idea that a more flexible method of identifying Flash Memory sizes and configurations is needed. From this need, the Common Flash Interface (CFI) specification has emerged, allowing all necessary Flash parameters to be stored directly on the memory - like a data book on a chip. The Common Flash Interface (CFI) is a major breakthrough in flash identification. It allows one set of software drivers to identify and use a variety of different current, and future, Flash products. This is possible because all identifying information for the memory is stored directly on the chip. Information such as the memory size, byte/word configuration, block configuration, necessary voltages and timing information reside on the chip for use by the system software. The Common Flash Interface (CFI) allows systems to accept and use most SIMMs (single in-line memory modules) and memory cards manufactured today and tomorrow without revising the software.

Software Read-while-Write. With current computer systems relying more and more on multi-tasking environments to provide real-time applications it is critical that the software has access to all of its data in deterministic times. The M58LWxxx family of Flash Memories solves this problem by providing fast program/erase suspend instructions, allowing access to valid regions of the Flash at any moment.

Typically a program or erase operation can be suspended in 10µs or less. Once suspended, Blocks of the Flash Memory that are not being affected may be read as normal, giving access to both code and data in the Flash Memory at very short notice.

Flexible Block Locking. Blocks can be locked to prevent accidental, unwanted Program or Erase operations from changing the data. Applications often protect the Boot Blocks as accidental Program or Erase operations to these Blocks can render the system unrecoverable. Critical data and application code are also often protected.

The Flexible Block Locking schemes allow any combination of Blocks to be locked. Like Program and Erase operations individual Block Locking is performed by an embedded algorithm so the user does not need to worry about the internal workings of the Flash Memory. All Blocks can be temporarily unlocked to allow changes using to the memory before re-locking and securing the data.

NOR Technology. The M58LWxxx family is based on reliable NOR technology. NOR based Flash guarantees 100,000 program/erase cycles and guarantees 10 to 20 year data retention. Random access to all memory locations, in any order, are possible. This allows code execution directly from the memory. In-system programming capability is possible for flexible manufacturing systems.

BENCHMARKING AGAINST INTEL STRATAFLASH™

Intel also offer Multi-bit Flash Technology in their StrataFlash memory family. The Advanced features of the M58LWxxx family make it more suitable for a variety of applications. The following tables give indications as to which applications will benefit the most from each of the features of each memory.

Table 2. Benchmarking against Intel StrataFlash(1)

Parameter/Function	M58LW064A/B M58LW128A/B	28F640J3A 28F128J3A	M58LWxxx Family Advantages
Read Voltage	V_{DD} = 2.7 to 3.6V V_{DDQ} = 1.8 to 3.6V	V_{CC} = 2.7 to 3.6V V_{CCQ} = 2.7 to 3.6V or 5V	Connection to low voltage MCUs simpler for low power applications.
Program/Erase Voltage	V_{DD} = 2.7V to 3.6V	V_{CC} = 2.7 to 3.6V	Low Power Program/Erase
Program/Erase Enable	Logic level Program Enable pin, V_{PP}	Logic level Program Enable pin, V_{PEN}	Easy software or hardware program and erase protection
Bus Width	x16 or x32	x8 or x16	High Bus Width for high bandwidth, direct code execution, integration with advanced microprocessors
Block Organization	Equal 64 Kword	Equal 64 Kword	All Blocks equal simplifies Data Storage algorithms.
Random Access	150ns (V_{CC} = 2.7V)	120ns (V_{CC} = 2.7V)	150ns with 32-bit bus for high data transfers
Burst Mode	Yes	No	Fast access for high speed synchronous transfers to MCU
Page Mode	Yes	Yes	Fast access for non-burst mode MCUs
Read Current	30mA	55mA	Low power for long battery life even during code execution from memory
Standby Current	40µA	100µA	Exceptionally low power for long battery life.
Power Down Current	1µA	50µA	Exceptionally low power for long battery life.
Command Set	All Compatible except programming, where: M58LWxxx provides a 16 Word Buffer and StrataFlash provides an 8 Word Buffer		The Command Set offers very powerful programming instructions and clear identification modes

Parameter/Function	M58LW064A/B M58LW128A/B	28F640J3A 28F128J3A	M58LWxxx Family Advantages
Program Operations(2)	Program 4 to 16 Words or 2 to 8 Double Words	byte/word program with 32 byte program buffer	Write Buffer decreases CPU load and increases programming speed.
Typical Programming Time (Average Word)	12µs	12µs	Fast Word Programming time for efficient data updates
Program Time	0.85s per Block	0.8s per Block	
Program Suspend Latency	3µs (typ)	25µs (typ)	Very fast access to data in other blocks when programming.
Erase Operations	One Block at a Time	One Block at a Time	
Erase Time	1s	0.7s	
Erase Suspend Latency	10µs (typ)	26µs (typ)	Very fast access to data in other blocks when erasing.
Error Code Correction	Yes	No	Enhanced Data Integrity for Code Storage
CFI	Yes	Yes	Software readable Data Book for transparent future upgrade
Endurance	100,000 Program/Erase Cycles per Block	100,000 Program/Erase Cycles per Block	Long life
Packages (x16)	TSOP56 TBGA64	TSOP56 EasyBGA	Die-sized packages for sub-miniature applications.
Packages (x16/x32)	TBGA80	N/A	Die-sized packages for sub-miniature applications.

Note: 1. The benchmarking done in this table is an ST evaluation based on the Intel document 290667-005, March 2000.
2. For the M58LWXXX family the minimum Buffer Size of a "Write to Buffer and Program" command is 4 Words or 2 Double Words.

Connecting the M58LWxxx family to CPUs is similar to connecting the Intel StrataFlash. Both parts use Write Enable and Output Enable control signals; Chip Select for single Flash memory systems are the same; Page Mode is supported on both memories and the pin connections have been made as similar as possible. Burst systems will not be able to support Intel's family without extra logic; the burst signals are one of the main differences between the M58LWxxx family and the StrataFlash family. The M58LWxxx family offers designers to opportunity to interface to 32-bit data buses using a single Flash memory part, whereas the StrataFlash family is only available in bus widths up to 16-bits. Two StrataFlash memories are required in parallel to interface to 32-bit CPUs at the full bus width.

Figure 5 shows the connections between a typical CPU and the two Flash memory families. For applications requiring 32-bit data buses, using one Flash memory rather than two simplifies the circuit and the PCB layout. For 16-bit applications the M58LWxxx family can be used in word mode. The burst control pins of the M58LW064B are not shown in the diagram.

Figure 6 gives a comparison between the pin-connections of the StrataFlash family and the M58LWxxx family for the TSOP56 package. This highlights that, with careful design, it is possible to make a PCB that can take either part. The pins that have specific differences are given in Table 3.

Table 3. Description of the Pin Differences between the M58LWxxx Family and StrataFlash Family

M58LWxxx	StrataFlash	Comments
R	CE1	The Valid Data Ready output, R, in the M58LWxxx family is an open drain output. CE1 in the StrataFlash family is a Chip Enable input. Many designs can ground this pin since, in both cases, no harm will come to either memory.
$\overline{L}$	CE2	The Latch Enable input, $\overline{L}$, in the M58LWxxx family is used to latch the address for multiplexed address/data bus systems. The input is not required until bit M3 in the Burst Configuration Register has been set. The pin can be grounded for successful operation of both memories in the same socket.
K	BYTE#	The Burst Clock input, K, in the M58LWxxx family is used to perform synchronous burst operations. BYTE# controls whether the StrataFlash is in byte-wide or word-wide mode. The pin should be tied to V_{DDQ} for correct operation of both parts in the same socket.
$\overline{B}$	A0	The Burst Address Advance input, $\overline{B}$, is used to advance the address during burst operations. A0 is not used when the StrataFlash is in word-wide mode. The pin can be tied to V_{SS} or V_{DDQ} for correct operation of both parts in the same socket.
V_{DDQ}	V_{CCQ}	The M58LWxxx family output drivers operate in the range 1.8V to 3.6V, whereas the StrataFlash family work from 2.7V to 3.6V and at 5V ±10%. The range of operation for both parts to work in the same socket is 2.7V to 3.6V.
R$\overline{B}$	STS	The Status output, STS, in the StrataFlash family is configured to behave the same as the Ready/Busy output, R$\overline{B}$, on power-up and on reset. Unless the configuration of the StrataFlash is changed the two parts will behave the same.

CONCLUSIONS

The M58LW064 is the first in a new series of Advanced, Next Generation Flash Memories from ST Microelectronics. The family includes many features to simplify and cost-reduce the products of today and tomorrow.

Figure 5. Comparison of M58LW064B and 28F032J3A connections to 32-bit CPU

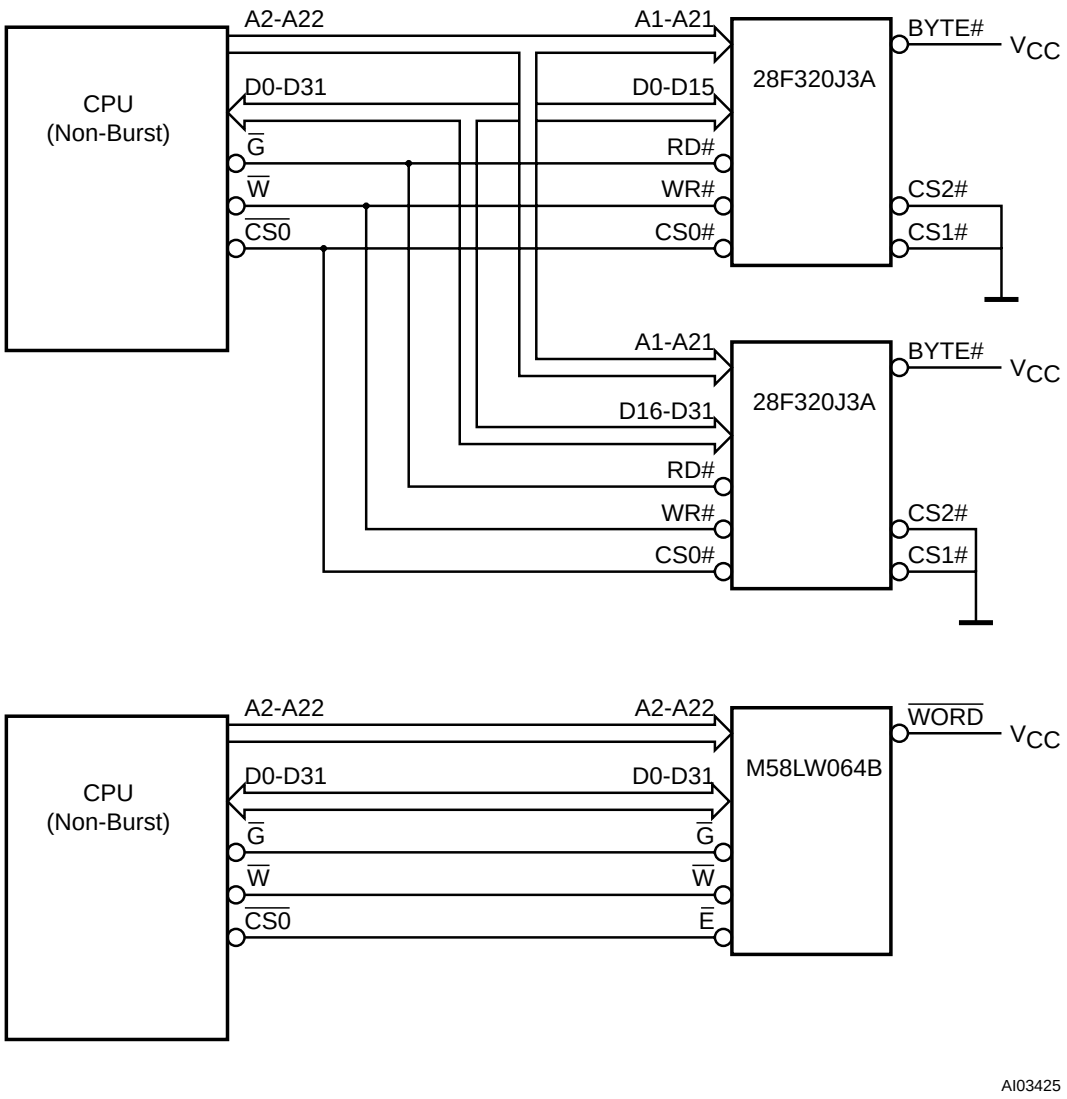
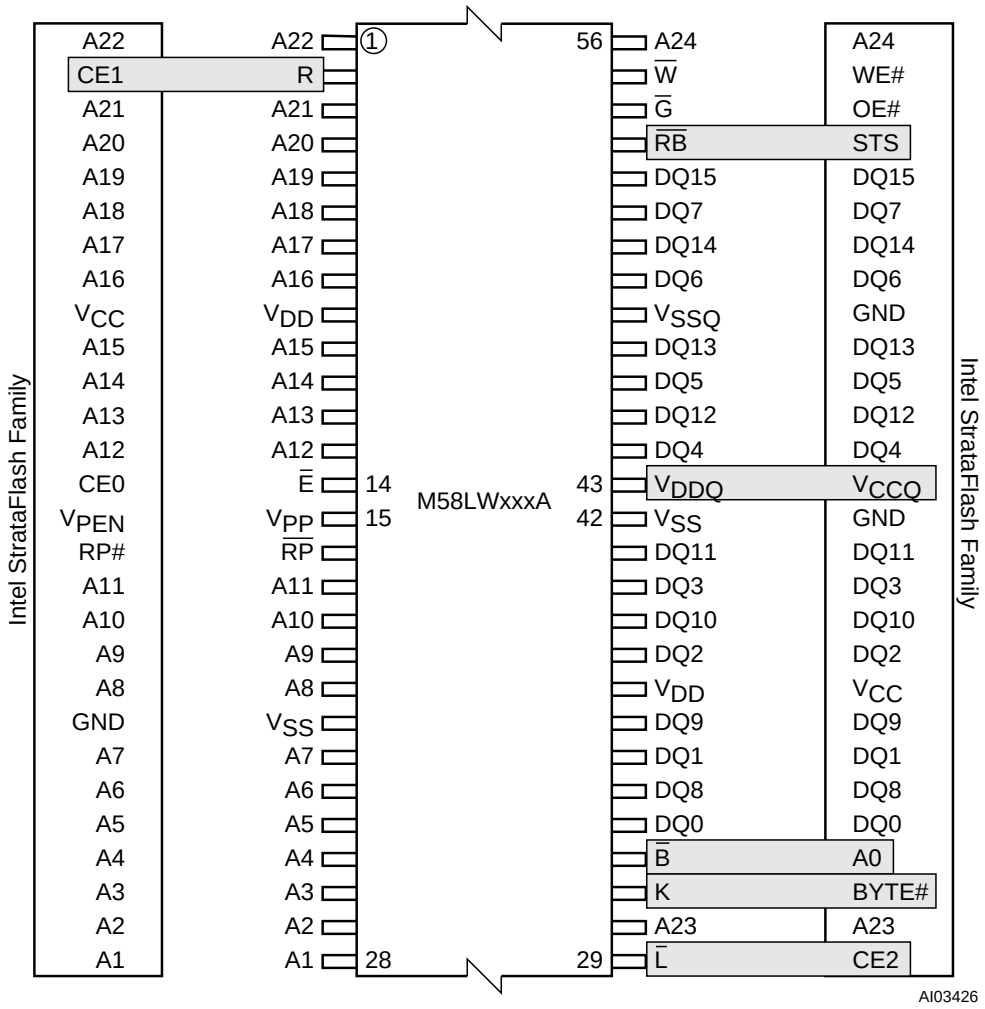


Figure 6. TSOP56 Connection Differences



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