APPLICATION NOTE

THE NEW ACS™ SERIES: A BREAKTHROUGH IN RUGGEDNESS & DRIVE FOR HOME APPLIANCES

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INTRODUCTION

Home appliances such as washing machines, refrigerators and dishwashers use a lot of low power loads such as valves, door lock systems, dispensers or drain pumps. Since these loads are powered by the mains in ON / OFF mode, they were initially controlled by relays. Recently, relays have been replaced by triacs, due to their smaller size and lower driving energy. Nevertheless triacs don't fulfill alone the new requirements that users now need and are used with others components.

Power switches must now be directly driven by a microcontroller unit (MCU) and must be robust to withstand the a.c. line transients so that systems may fall into line with new European electromagnetic compatibility (EMC) standards. ACSs (for Alternative Current Switches) have been designed with this goal mind, i.e. to offer logic level and more robust semiconductor devices.

On the other hand, ACSs have been developed adopting a functional integration approach. They can be used directly between a MCU and the load. An external protection or buffer circuit are not required since these are already integrated on the die. This considerably reduces the overall electronic board size. Moreover, the array of ACSs allows one device to control the various loads typically required in a washer appliance.

Table 1 gives the RMS current of loads that can be controlled by ACS402-5SB4 or ACS108-5SA/N, in ON / OFF control mode.

Table. 1: ACS108 and ACS402 targeted loads.

LOAD	IRMS (A)	POWER FACTOR	(dIout/dt)c (A/ms)	(dVout/dt)c (V/µs)	TURN-OFF DELAY (ms)
Door Lock Lamp	< 0.3	1	0.15	0.15	< 10
	< 0.8	1	0.4	0.15	< 20
Relay Valve Dispenser Miro-motor	< 0.1	> 0.7	< 0.05	< 2	< 10
Pump Fan	<0.2	> 0.2	< 0.1	< 10	< 10
	< 0.6	> 0.2	< 0.3	< 10	< 20

ACS TRIGGERING MODE

1: Negative gate current.

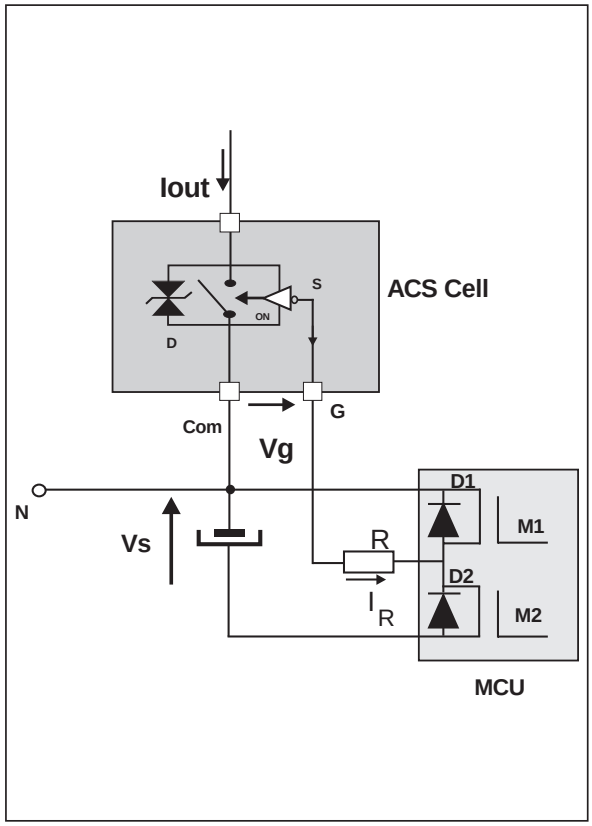
The ACS silicon structure is different from the triac one. For instance, the gate embeds a diode junction. Then the gate current can only circulate in one direction, from the COM pin to the Gate one. A peak reverse voltage (V_{GM}) of this junction is also defined in the ACS data sheet.

In order to sink a current from the gate by a microcontroller output port, the supply voltage positive terminal must be connected to the drive reference, i.e. the COM pin of ACSs (cf. figure 1).

An interesting benefit of such a connection is that the ACS is not fired when the MCU is at reset state. Indeed, in this case, all the MCU port pins are at high level. This means that the gate resistors are all connected to the COM terminal (for I/O port in Push/Pull configuration). No spurious triggering can then occur.

It should be noticed that for a direct switch / MCU connection, the MCU current capability is not the only point to check to decide if the buffer circuit can be removed. Actually, the transistor, used to amplify the MCU current in order to control the gate, also play an overvoltage protection role. Annex B gives the gate voltage limits between which the MCU output port will be not stressed. It is also shown that with ACSs, the gate voltage remains inside these limits even with worst cases of dI/dt gradients at turn-on.

Fig. 1: Gate / MCU connection.



2: New layout possibilities.

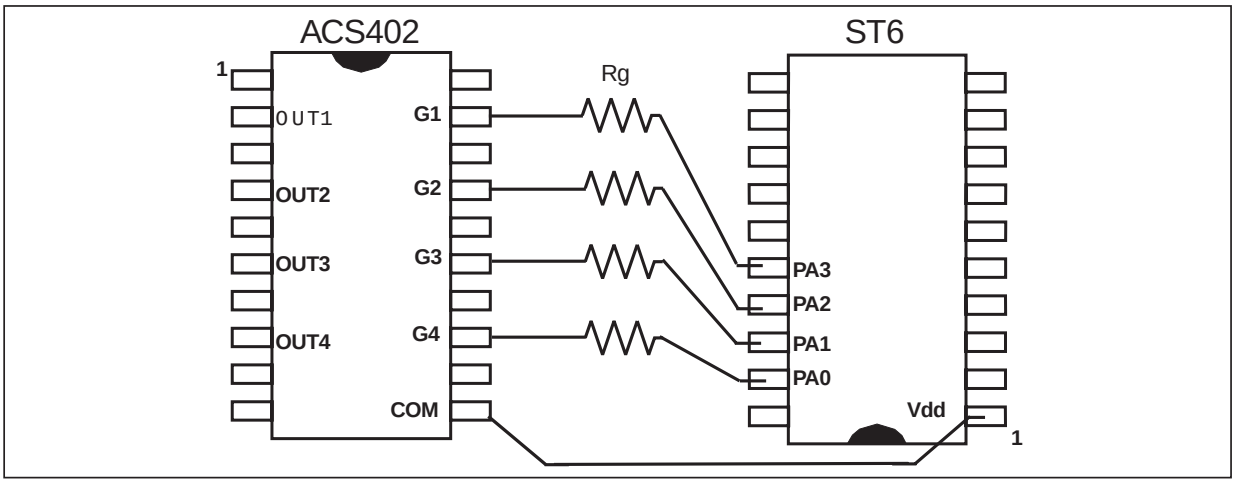
It has already been said that ACS silicon structure is different from the triac, according to the gate operation. A second difference is that ACS have been developed in an integration goal.

To allow different cells to be associated in one single package or controlled by one single drive die, the common drive reference voltage must be connected to the back of the die. Indeed, each die bottom is electrically linked to the other ones by the frame. This is achieved by the ACS silicon structure, where an integrated level shifter allows both thyristors to be controlled by means of a gate voltage referenced at the back of the die (COM pin) [1].

Thanks to ACSs arrays, the copper tracks count is reduced since the different COM pins are connected together inside the package. This also allows smaller gate / MCU copper tracks loop areas, and so increases the EMI immunity of the overall electronic board.

Figure 2 (on page 3) shows an example of connection between an ACS402-5SB4 and a ST62xx, both in DIL20 packages.

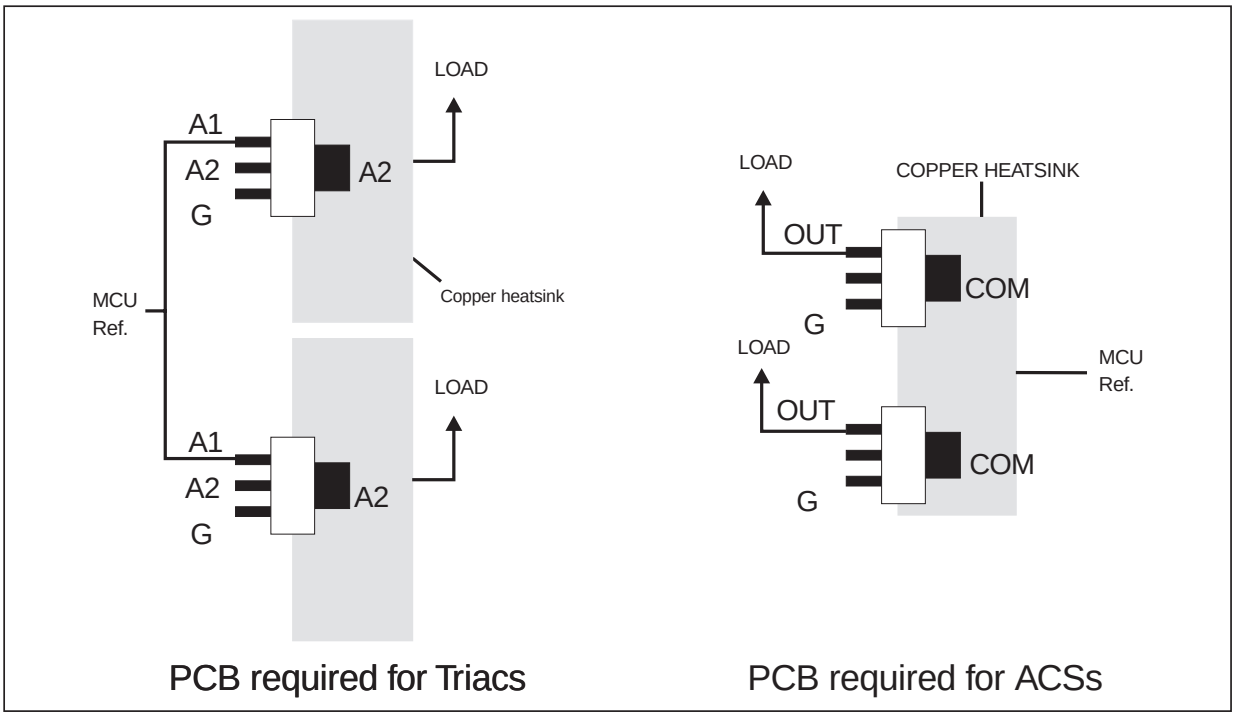
Fig. 2: Reduction of gate / MCU loop areas.



A particular benefit of such a pin out appears with Surface Mount Devices (SMD). In this case, the tab pin is the COM one. The copper surface used to perform a heat-sink can then be used as a supply voltage bus. It allows new layout possibilities and, above all, a miniaturization of the Printed Circuit Board (PCB).

Indeed, unlike triacs, the heat-sink areas are at the same voltage and so can be regrouped (cf. figure 3). The heatsink area therefore depends on the maximum amount of dissipated power at the same time, by all the switches put on it. So, the number of switches which will conduct at the same time and their conduction time should be known.

Fig. 3: Printed circuit area reduction thanks to ACSs in SOT223 packages.



INDUCTIVE LOADS ON / OFF CONTROL

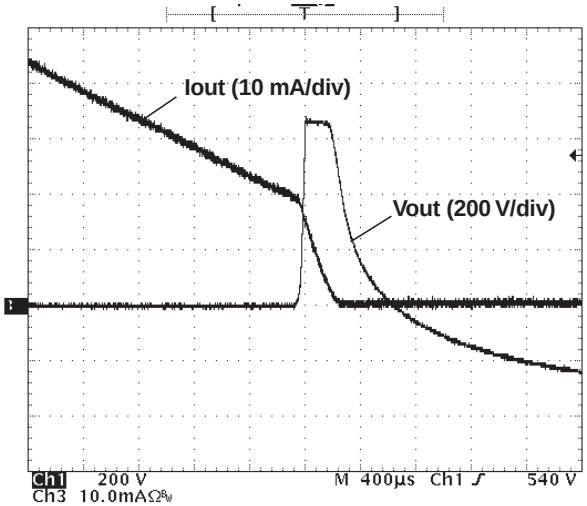
1: Valves and relays

1-1: Turn-off overvoltage are clamped by ACSs.

Valves and relays are both electromagnetic systems. In the case of AC high voltage operation, their windings present a high series resistance (a few kOhm) and a high series inductance (tens of Henry). Hence, they absorb a low RMS current (typically, 10 to 50 mA). In this case, the current rate of decrease is low and an automatic switch turn-off may result, when its current becomes lower than the holding level [2]. There may be an over-voltage due to the fact that there is still some current through the inductive load. The inductive energy thus creates a back electromotive voltage which tends to force the switch to conduct. If this over-voltage is not clamped, it can exceed the device breakdown level and damage it.

ACSs are over-voltage self-protected. They can sustain their holding current in such an operating mode, as shown in figure 4.

Fig. 4: ACS voltage & current waveforms at turn-off (230V, 35mA RMS valve).



During clamping periods, the inductive energy is dissipated both in the silicon die and the series resistance of the load. The worst case appears when the load inductance is the highest, i.e. for electromagnet loads.

In annex C, a theoretical analysis is performed with a 0.1 power factor load and an RMS current lower than 40 mA (value which never appears in practice where, for such RMS currents, the power factor is always higher than 0.7). Then, it is demonstrated that, even in this worst case scenario, the transient junction temperature remains below 160°C. And the clamping period time (t_{cl}) always lasts less than 1 ms. Such thermal stress is suitable for ACSs dies thanks to their reliable planar technology.

2 : Maximum switching frequency.

As far as thermal management involving clamping phases is concerned, a maximum load commutation frequency must be defined to avoid excessive device heating.

Figure 5 gives the maximum supplementary temperature rise due to recurrent clampings, versus the ACS switching period (see annex C). This figure is given for a 230 V - 50 Hz mains voltage (110 V mains is less stressing), for the worst case of load (power factor = 0.1, peak load current = i_{Hmax}) and for the maximum V_{CL} and i_H values (800 V and 60 mA respectively). In this case, the energy absorbed by the die equals 25 mJ.

The chosen package is the TO92 one (ACS108-5SA device) because it presents the highest Rth value, among ACS packages on offer (DIL20, TO92, SOT223).

It can be seen that this temperature elevation can be neglected (< 4°C) as long as the control frequency is less than one Hertz. Such a value is suitable for most appliance applications where loads are at most controlled once per second. For that reason, in ACS data-sheets, the maximum allowed current is given for a 1 Hertz maximum frequency 0.1 minimum load power factor. Turn-off dissipated power is then reviewed for a wide range of application needs.

This enables us to conclude that no varistor is needed across ACSs to clamp the loads inductive energy at turn-off, even with electromagnets which are the highest inductive loads in Appliances.

2: Pumps and Fans ON / OFF control.

2-1: Application (dI/dt)c & (dV/dt)c needs.

There is a higher risk that a triac or an ACS will fail to turn-off when both the load current rate of decrease and the reapplied voltage rate across the device are steep [3]. This risk increases as the junction temperature increases. The maximum current decreasing rate that ACS can switch off, called (dI/dt)c is defined for a maximum reapplied voltage rate, called (dV/dt)c, and for its maximum T_j.

Pumps and Fans are, for the most part, induction or permanent magnet motors. Their series inductance is in the range of one Henry, and their winding resistance equals a few hundred Ohm. Their power factor is low. Hence, after switch turn-off, the reapplied voltage across it is high and appears with a high rate of increase (as described in the equation 1 here-after where L and cosφ are the inductance and power factor of the load, V the mains RMS voltage and C is the ACS capacitance value):

Equation 1:

$$(dV/dt)c_{(V/\mu s)} \cong V_{(V)}\sqrt{2}\sin\varphi / \sqrt{L_{(H)} x C_{(F)}}\; x10^{-6}$$

Figure 6 shows that the (dV/dt)c rate for an ACS402 die without any snubber, controlling a 230 V 220 mA pump, is lower than 10 V/µs. The measure will be similar with an ACS108 die because it presents the same capacitance value as an ACS402.

The next equation (2) shows that the current rate of decrease is almost half the RMS current (0.44 ratio for a 50 Hz mains frequency and 0.53 for 60 Hz):

Equation 2:

$$(dI/dt)c_{(A/ms)} = \sqrt{2}\, x\, I_{rms(A)}\; x\; 2\pi\, x\, f_{(Hz)}\; x\; 10^{-3}$$

To summarize, it can be said that the worst commutation case appears with pumps or fans. In this case, the stress that ACSs must withstand is:

Equation 3:

$$\begin{cases} (dI/dt)c_{(A/ms)} = \dfrac{1}{2}\, I_{RMS(A)} \\ (dV/dt)c < 10V/\mu s \end{cases}$$

Fig. 5: Supplementary temperature elevation due to repetitive clampings (@ clamping energy = 25mJ, package: TO92).

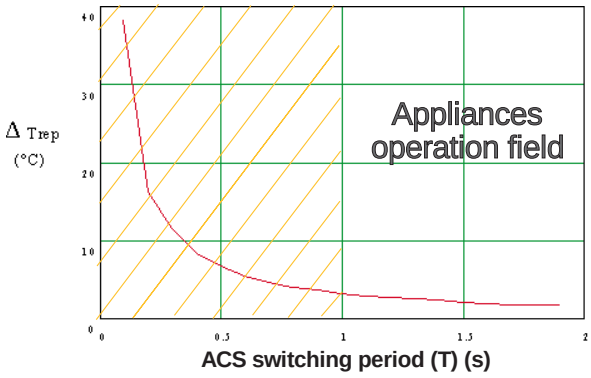
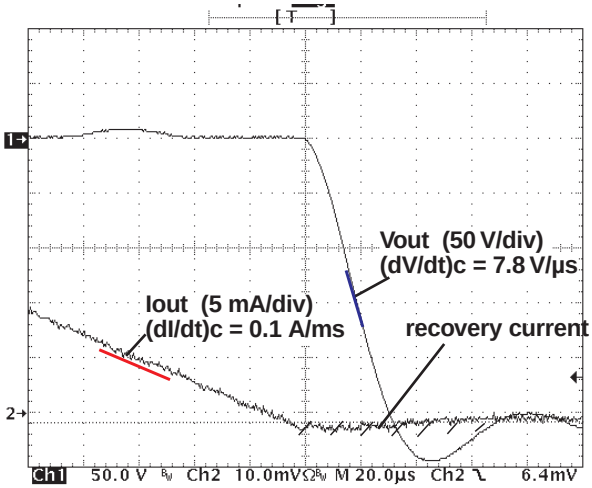


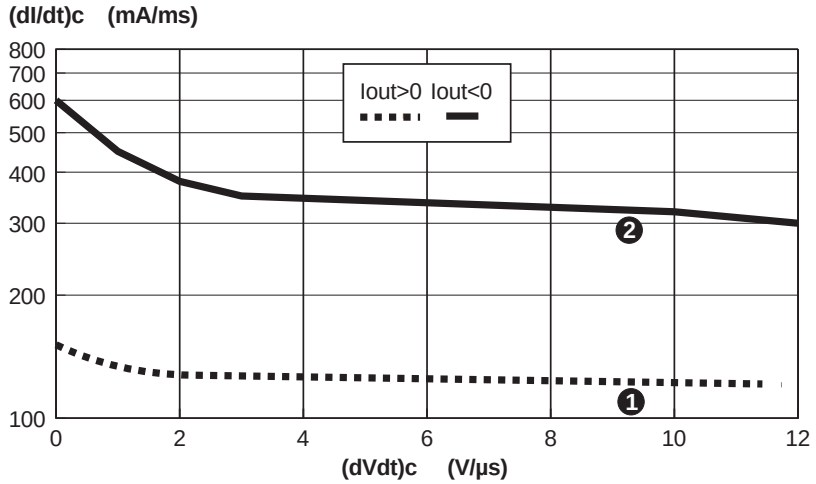
Fig. 6: 230V 220mA RMS pump switch-off.



2-2: ACS asymmetrical turn-off behavior

As shown in Figure 7, ACSs behave differently depending on the current direction before switch-off.

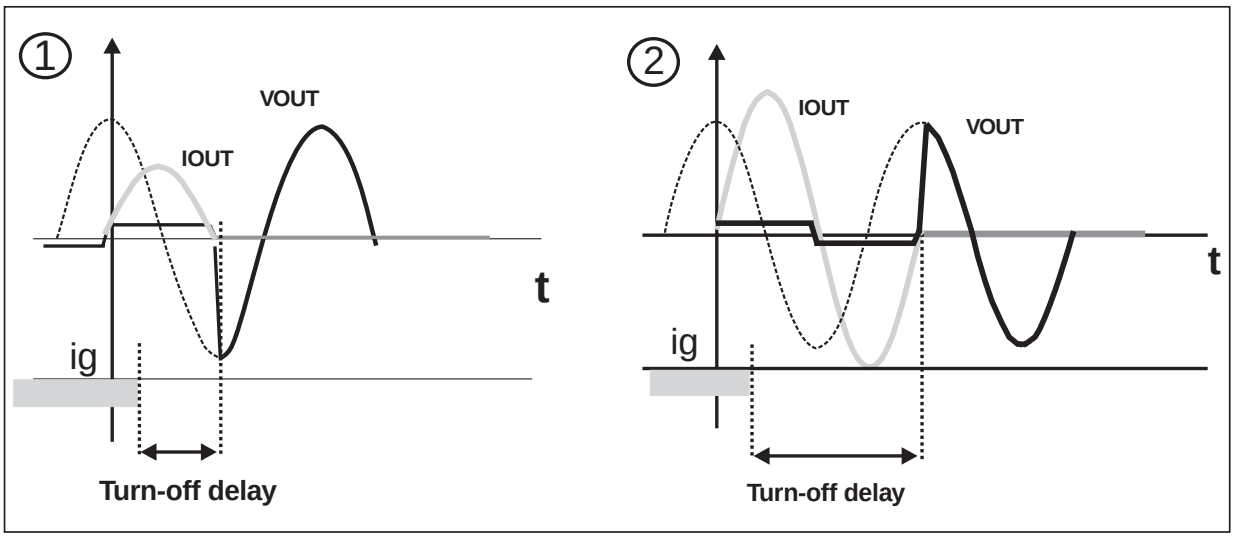
Fig. 7: ACS402 & ACS108 (dI/dt)c typical ability versus reapplied (dv/dt)c rate @Tj = 110°C.



For 200 mA RMS maximum current pump (see case 1 in Figure 7), the turn-off will be performed whatever the current sign is. The maximum turn-off delay is then one half cycle (10 ms for 50 Hz mains).

On the other hand, for a 200 - 600 mA RMS pump (see case 2 in Figure 7) and 110°C junction temperature, the switch-off will only be achieved when the current reaches zero with a negative sign. Therefore, in this case, the turn-off delay time can reach up to 20 ms for 50 Hz line frequency (cf. Figure 8).

Fig. 8: Turn-off delay for different pump or fan RMS currents.



RESISTIVE LOADS ON/OFF CONTROL

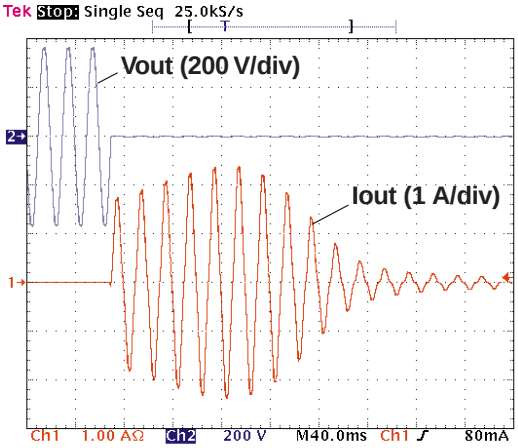
1- Inrush current.

In most systems, resistive loads are thermal effective. For example, light bulbs emit light when their filament is hot enough. New types of door-lock actuators have emerged in which the bolt move is due to a thermal expansion of a metallic part or a wax.

All these loads can be characterized by a very low resistance value in cold state. Consequently, when the switch is turned on, there is a high inrush current. For low power light bulbs, the inrush current lasts on average 10 ms. The worst scenario is in the case of thermal door-locks.

Figure 9 shows a typical inrush current in such loads.

Fig. 9: Inrush current in a 230V thermal effective door-lock.



2- Transient junction temperature.

With such current shapes at turn-on, thermal calculation must be carried out in order to choose the right package or heat-sink so as to avoid exceeding the maximal junction temperature (110°C).

To perform the calculus, the current shape must be simplified. Let us work on the hypothesis that the current average waveform of figure 9 is similar to a 2 A peak 0.18 s time long sinus shape.

Then, the average conduction and gate current losses in the ACS are given by the following relationship:

Equation 4:

$$P_{av} = r_d \times I^2_{RMS} + V_{t0} \times I_{RMS} \frac{2\sqrt{2}}{\pi} + V_{gt} \times I_g$$

Then, according to ACS108 or ACS402 specifications, we find: P_{av} = 1.766 W.

Equation 5:

$$T_{j\,peak} = T_{jo} + Zth(t_p) \times P_{av}$$

For a t_p long dissipated power pulse, the peak junction temperature ($T_{j\,peak}$) is given by the here-above equation, where T_{jo} is the initial T_j value.

Since the thermal impedance values at 0.18 s for TO92 and DIL20 packages are 22.5 and 8 °C/W respectively, it can be said that the junction temperature elevation, at the end of the inrush current period, is 40 °C for a TO92 package and 14 °C for a DIL20 package.

So, the maximal junction temperature before door lock switch-on should be at most 96°C for ACS402-5SB4 (DIL20) and 70°C for ACS108-5SA (TO92), in order to keep $T_{j\,peak}$ below $T_{j\,max}$ (110 °C).

For washing systems, as the door lock start may appear at the beginning of a washing cycle, we suppose that T_{jo} equals at worst the maximal ambient temperature, i.e. 70 °C.

So, in this respect, both ACS devices are convenient for door lock operation.

3- Light bulb flashover.

Another point should be highlighted when driving a light bulb with a silicon switch. Indeed, at the lamp life time end, the filament breaks itself. This result on a flashover across the gas, included in the bulb. Then, the overall filament can be short circuited by the flashover, and the load current is not more limited.

Figure 10 gives the typical overcurrent measured when a 25 W lamp fails. This current can exceed the i^2t capability of the ACS and destroy it.

To avoid to destroy the ACSs at each lamp flashover, a power resistor can be added in series with the light.

This resistor (R) is rated in order to limit the ACS current to its I_{TSM} value (10 for a 10 ms half sinus conduction). R is calculated as following:

Equation 6:

$$R = \frac{230 \times \sqrt{2}}{10} = 33\Omega$$

The power resistor depend on the RMS current of the load:

Equation 7:

$$P = R \times \left(P_L / V\right)^2 = 33 \times 25^2 / 230 = 0.39W$$

A 33 Ohm 1/2 W resistor is so sufficient.

Figure 11 gives the overcurrent measured with such a resistor, during the flashover of a 25 W light bulb.

Fig. 10: 25W light bulb flashover current.

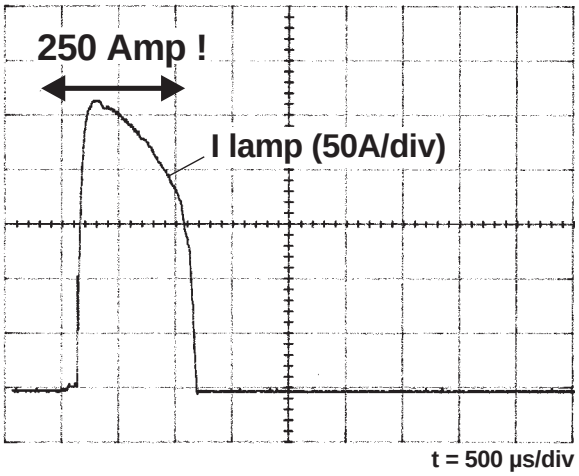
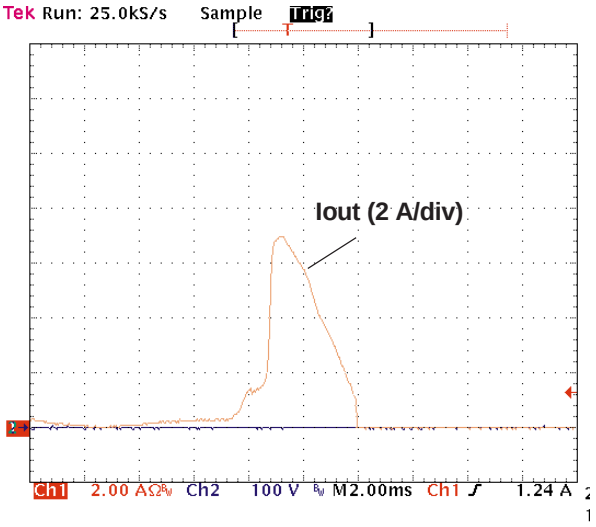


Fig. 11: Flashover current limited by a 33Ohm 1/2W resistor.



ELECTROMAGNETIC COMPATIBILITY STANDARDS

1- IEC 1000-4-5 standard.

1-1 Standard requirements.

The IEC1000-4-5 standard has been established to check if systems can always work after there has been a voltage surge super-imposed to the mains. A standard voltage waveform has been chosen which embodies typical over-voltages due to thunder or disconnection of running inductive loads from the line.

Two kind of surges must be applied:

1) **Line to Ground surge**: in this case the maximum voltage surge is 4 kV (for aerial power network), but the energy is absorbed by the Y2 capacitors (connected between lines and ground) of the mains filter.

2) **Line to Neutral surge**: in this case the maximum voltage surge is 2 kV (for aerial power network), and is applied across the power device and the load controlled by this one.

N.B: *1 kV is required for public power network*

A Line to Neutral over-voltage is then:

1) entirely absorbed by the load if the power switch is ON;

2) entirely held by the semiconductor device if it appears while the switch is at off-state.

As the Line to Neutral surge can appear at peak mains voltage, the overall amount of voltage can reach 2.4 kV. This will be higher than the break-down level of the silicon devices used in appliances. Then, in order to prevent components destruction, designers use a varistor connected across silicon devices. The overvoltage is limited below the breakdown level of the power semiconductor and the surge energy is absorbed by the Metal-Oxyde component.

1-2: ACS behavior during IEC 1000-4-5 test.

When a surge appears when an ACS is OFF, the mains over-voltage is first clamped by the device. But an excessive energy surge can raise the ACS current above its breakover level. Then, the switch turns on in break over mode. Such an event is particularly stressful on the semiconductor especially so if the current and its rate of increase are both high. The worst case occurs for ACS driving low resistance, non inductive loads.

For example, figures 12 and 13 have been recorded with a thermal active door lock system at low temperature. The 2 kV surge is super-imposed to the 230 V - 50 Hz mains and synchronized with its peak value, as shown on Figure 12.

Figure 13 zooms the device turn-on in this mode. As the load was previously off, its resistance is cold and equals 150 Ohm. In this case, the current rises at a rate of 100 A/µs and reaches 15 A. Such transient surges would damage triacs, but not ACSs which are designed to turn-on in breakover mode. No more varistor is then needed in parallel across ACSs unlike triacs. The difference between ACS and Triac + Varistor is that, with the ACS, the load is switched on during a half or one mains cycle. This can be accepted as such events happen a few times in the system's life.

Reliability tests are carried out on production batches to check the ACS robustness towards IEC1000-4-5. A standard surge generator is used directly across a load and an ACS. The load is a 150 Ohm resistor, including a 3 µH parasitic inductance, to simulate a cold door-lock. The applied surge is fixed at +/- 2,4 kV in order to be equivalent to a 2 kV over-voltage applied at the peak mains voltage, with the same bias.

Fig. 12: 2kV surge on the mains (IEC 1000-4-5 test).

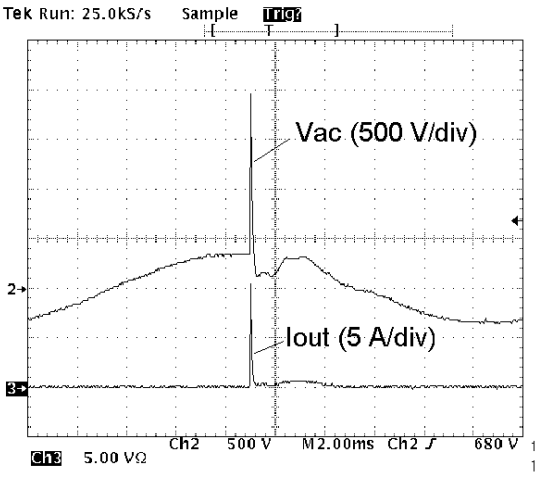
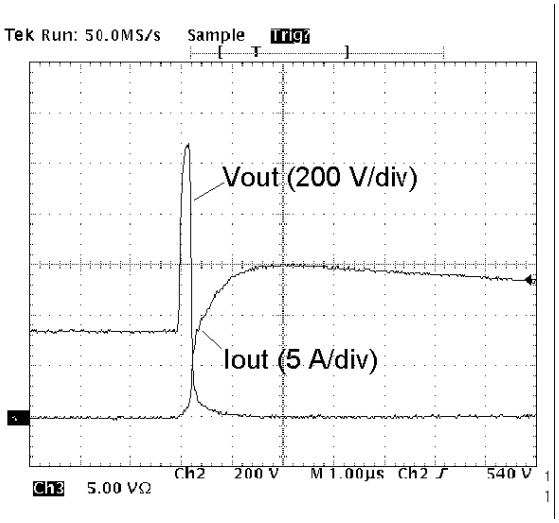


Fig. 13: ACS breakdown zoom (IEC 1000-4-5 test).



2-1: Standard requirements.

For IEC1000-4-4 tests, two different stressing ways are demanded. One is to apply the bursts to the Line, Neutral or Ground through 33 nF capacitors. In this case, the bursts are entirely absorbed by the mains filter, which is often present at the input of electronic systems. The second IEC1000-4-4 stressing mode is to apply the bursts through a typical 100 pF capacitor (realized by an aluminum sheet), directly to the I/O ports of the system.

The I/O port test is in fact required for systems where there are control wires, as for computers (wires between keyboard and central unit). But appliance manufacturers apply similar test to check if their products can withstand fast voltage transients.

The standard requires that for burst voltages up to 2 kV, the system must operate without problem. However, triacs can then turn-on due to high dV/dt rates. In this case, a snubber must be added to smooth these rates. Designers must then manage with the following trade-off:

1) **Reduce dV/dt rates**: the snubber capacitance must be high and the snubber resistance must be low;

2) **Reduce the dI/dt rate at turn-on**: the snubber capacitance must be low and the snubber resistance must be high.

2-2: Snubber removal thanks to ACSs.

I/O tests have been carried out on an electronic board including an ACS402, where the gate is short-circuited to the COM in order to avoid parasitic turn-on due to MCU bad operations. The system under test is embodied by this board. The I/O wires are then the OUT pins of each ACS cell (which are connected to the loads), plus the Line and Neutral wires. The trial diagram is shown in Figure 14,on the next page.

Fig. 14: IEC1000-4-4 test synopsis.

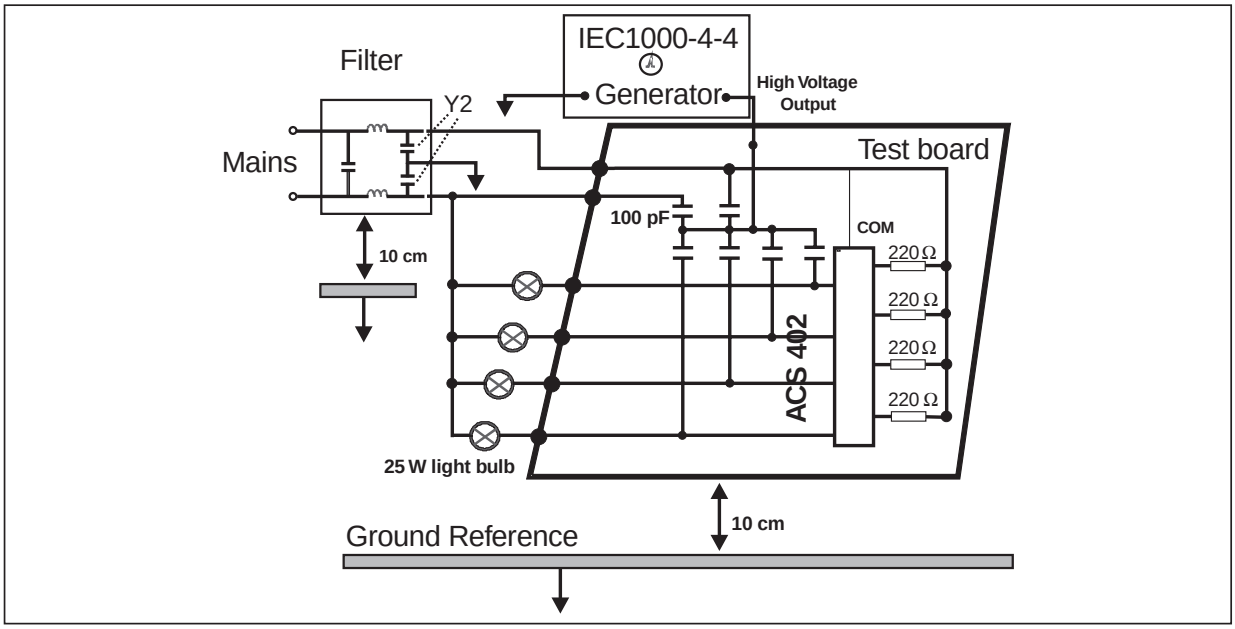
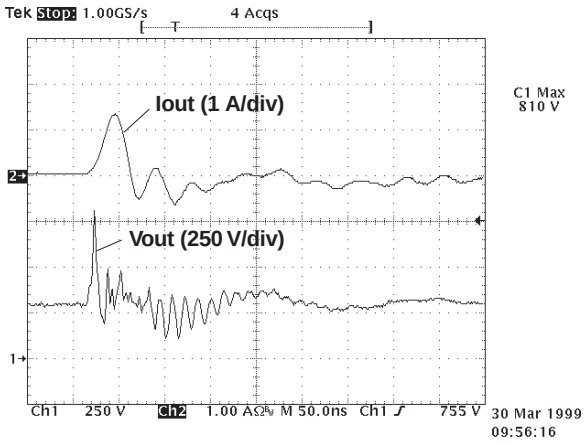


Figure 15 shows the OUT-COM voltage measured during a 2 kV IEC1000-4-4 test (N.B.: 1 kV is required for public power network). We see that in spite of capacitive current due to high dV/dt rates, the ACS does not turn-on. The semiconductor switch withstanding to IEC1000-4-4 depends on its dV/dt capability. ACS devices present dV/dt characteristics ten times greater than both same current and sensibility ratings triacs. For example, a 0.2 Amp - 10 mA maximum i_{gt} ACS has a minimum dV/dt capability of 500 V/µs (@ T_j = 110 °C).

It can also be seen that the ACS voltage overflows its breakdown value given for a 50 Hz sine wave (810 V is reached in spite of 650 V breakdown value). In fact, the voltage rate of increase is so high that the silicon device has not enough time to begin to clamp. A higher value than its V_{CL} value can then be reached.

To sum up, it can be said that ACSs, thanks to their high dV/dt capability, improve the overall electronic board robustness towards fast line transients without any snubber. But it must be kept in mind that the mains filter Y2 capacitors play also a role in sustaining IEC1000-4-4 tests, by derivating some part of the bursts energy. Typical value for these capacitors are 2.2 nF.

Fig. 15: IEC1000-4-4 test on ACS402 cell for 2kV burst.



CONCLUSION

ACS retains the well-known advantages of the triac (high AC voltage blocking capability, current bidirectionality) and adds high over-voltage ruggedness and the increased reliability and compactness that appliance manufacturers now need.

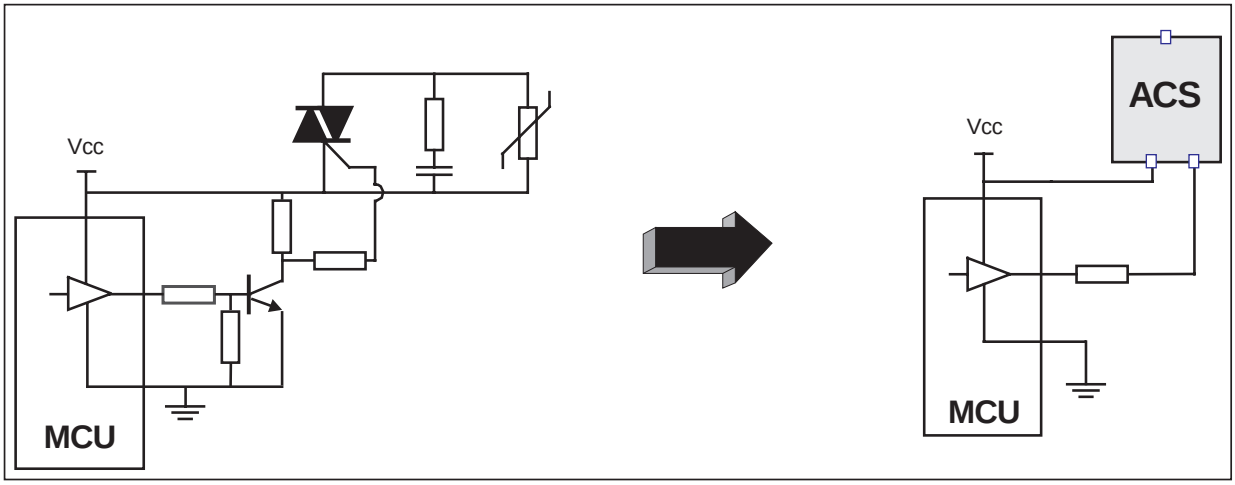
Thanks to the clamping capability and robust break-over characteristics of the ACS structure, the protection circuits that are usually connected in parallel with the triacs, are no longer required. The varistor removal increases automatically the reliability of the electronic board. And the snubber removal allows designers to be free with the dV/dt at off state and dI/dt at turn-on trade-off when choosing an R-C circuit.

In addition, the triac gate-drive transistor and its associated resistors are also redundant because ACS devices have built-in logic level drive circuits that allow the power switch to be safely driven from any MCU output pin capable of sinking 20 mA without over-stressing the micro-controller output.

Hence, the typical component count falls from eight with triacs, down to two with ACSs (cf. figure 16).

The new ACS devices represent a real breakthrough in the design of power switches for home appliances. The enhanced performance, for example their robust off-state and logic level drive, allied to their inherent compactness will open new perspectives in the design of compact and reliable electronic power controllers.

Fig. 16: Component count reduction thanks to ACS.



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ANNEX A: ACS402 demonstration Board

Figure A.1 shows the electronic diagram of a demonstration board used to illustrate ACS402 / ST6 compatibility. Note that the reset, power supply and oscillator circuits are given as examples. Other solutions are also possible. For instance, ST6 and ST7 microcontrollers with integrated reset circuits can be used.

The main features are:

-V_{DD} connected to the Neutral;

-V_{DD} is the reference voltage of each ACS402 cell, which are all connected together in the DIL20 package;

Fig. A-1: Demonstration board diagram.

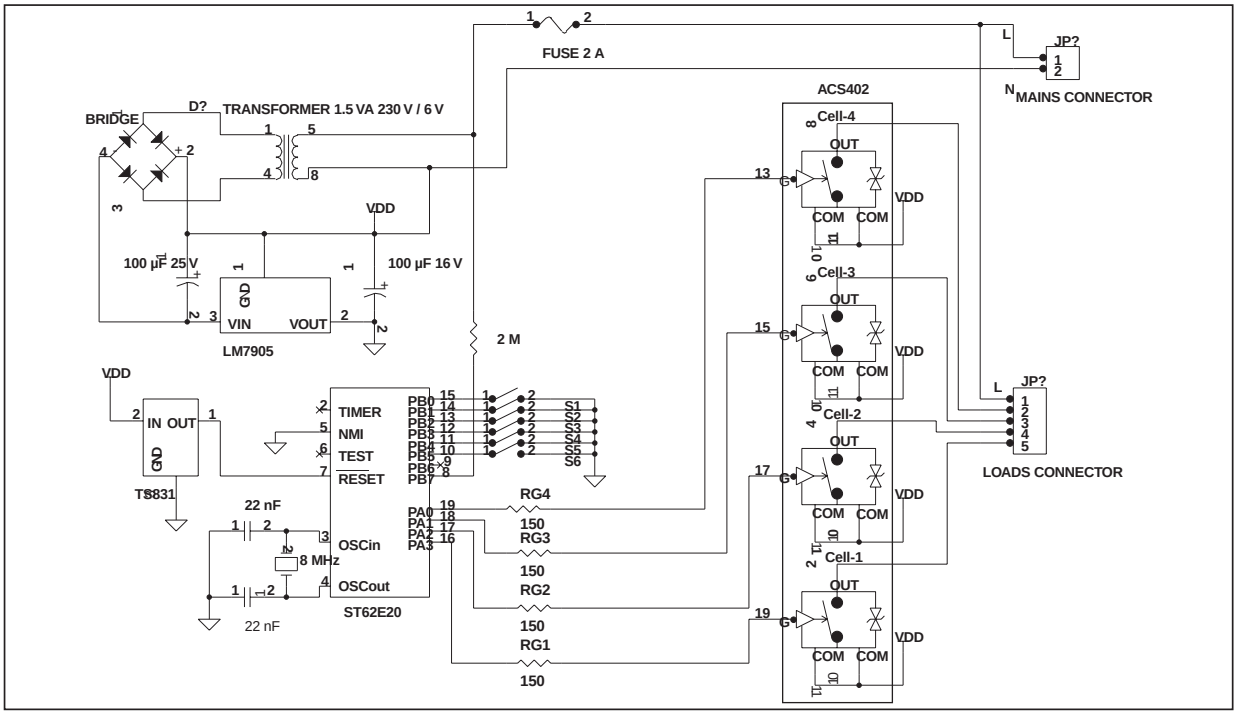
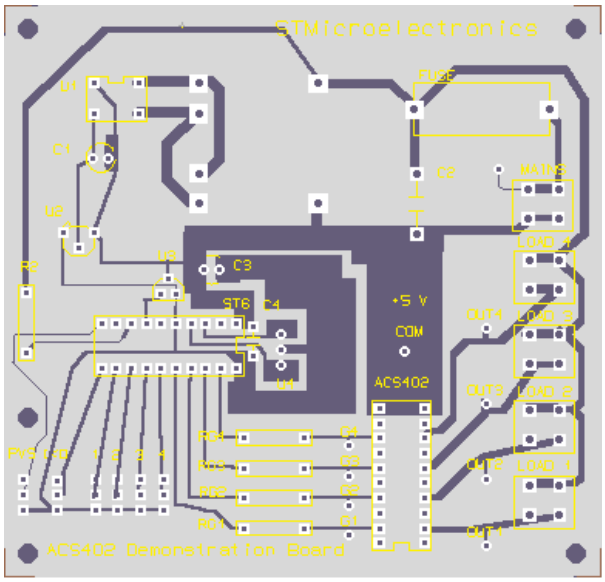


Fig. A-2: Demonstration board printed circuit.



ANNEX B: ESD diode conduction due to kick-back.

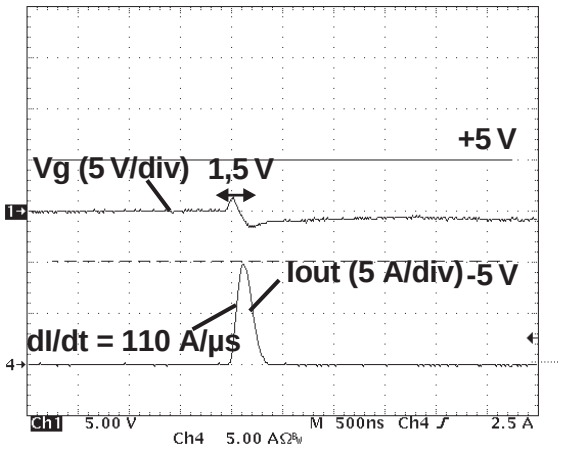
An over-voltage can appear across the gate and COM (or A1 for triacs) terminals at high turn-on di/dt rates. This effect is called the “kick-back”. It is due to the high density current at turn-on which causes high conduction voltage drop. Since the conduction begins around the gate area, the forward voltage is in part applied to the gate.

This gate spike is clamped by the micro-controller internal electrostatic discharge (ESD) diodes, which can be damaged if conduction lasts for too long. In order to prevent ESD diodes conduction, their voltage must remain negative. When considering figure 1 at ACS turn-on, i.e. when the push transistor M1 is off and the pull transistor M2 is on, a circulating current will never occur through D2 if the current i_R remains positive. This yields to the equation B1:

Equation B1:

$$R \; x \; i_R = -V_{M2} + V_s + V_g > 0$$

Fig. B-1: Kick-back test with ACS402.



As M2 is conducting, its voltage drop can be neglected. Thus, the previous relation gives:

Equation B2:

$$V_g > -V_s$$

If D1 conducts, this means that the supply voltage is held by M2, neglecting D1 drop voltage. This MOS transistor is thus in a linear mode. Its current equals its saturating level, called i_{sat}.
Now, since the i_{sat} current is necessarily higher than V_s/R ratio- in order to secure the micro-controller operation -we can write the following relationship.

Equation B3:

$$V_{D1} = V_g - R \; x \; i_{sat} < V_g - V_s$$

A sufficient condition to ensure that V_{D1} remains below zero is that V_g remains below Vs. This condition, plus the equation B2, gives the following safety rule for no ESD diode conduction:

Equation B4:

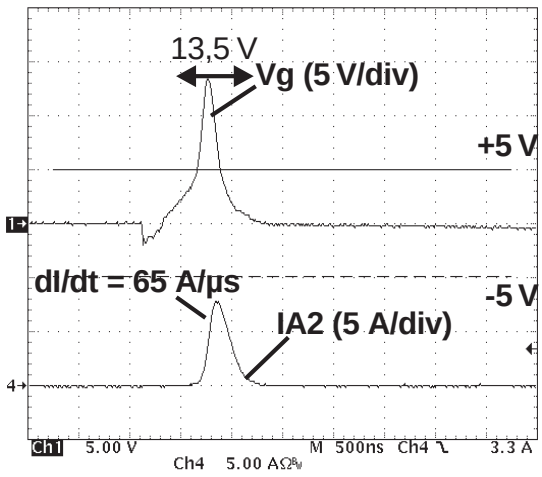
$$-V_s < V_g < +V_s$$

To compare the kick-back effect of triacs and ACSs, a special test circuit has been defined. It consists on turning on the switch with a 10 nF capacitor connected directly across the A1-A2 or OUT-COM terminals. The capacitor is charged at 300 V. Figures B.1 and B.2 show the experimental results obtained with such a testing method, for positive bias voltage.

A Z0109 (0.8 A I_{RMS}- 10 mA i_{gt} ST triac) doesn’t fulfill with the equation 4, for the V_{GA1} voltage reaches 13.5 volts with a 65 A/µs dI/dt rate. This is largely above the supply voltage. With the ACS402, the maximum V_g voltage is 1.5 Volts, and is still within the equation B4 limits despite a dI/dt which is twice as big as with the Z0109.

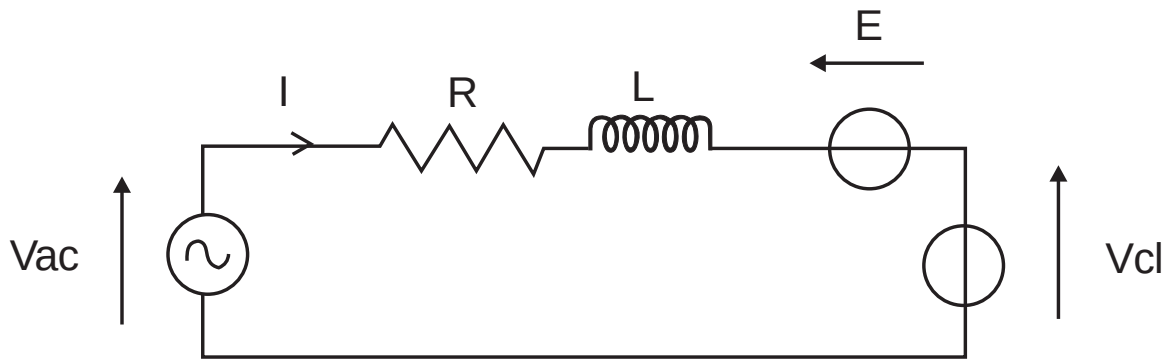
ACS / MCU interface would then be secured even at turn-on at peak mains voltage or on a short-circuit.

Fig. B-2: Kick-back test with Z0109 triac.



ANNEX C: How to calculate the junction temperature during clamping periods ?

Fig. C-1: Electric equivalent circuit at clamping.



1- Dissipated power evaluation.

It should be kept in mind that the load inductive energy is not entirely absorbed by the die at clamping. Another part is dissipated by the Joule effect in the load resistor or absorbed by the mains. A way to accurately evaluate the clamping energy is then to estimate the ACS current waveform, versus the time. The energy is then calculated by integrating this waveform and the product of the clamping voltage along the turn-off period.

Let us consider a typical AC load equivalent circuit shown in figure C.1. The load current during the clamping time is given by the following relationship.

Equation C1:

$$i(t) = i(t_0) + \frac{V_{CL} + E - Vac}{R}\left(e^{-\frac{R}{L}(t-t_0)} - 1 \right)$$

It is difficult to evaluate the influence of E in a general way. Its sign depends on its phase towards the current and the value of the holding current. But, it can be said that the back electromotive force has little influence for most universal and synchronous motors in which impedances are high and E is close to zero. Furthermore, for all other loads, such as passive loads or asynchronous motors, the b.e.m.f E is null. For this reason, let us neglect its value. Let cos φ be the load power factor and V the RMS mains voltage. Since the clamping occurs near the zero crossing current, the value of the main voltage at t_0, for a positive current, is given by the relationship C2.

Equation C2:

$$V_{ac} = -V\sqrt{2\left|1 - \cos^2 \varphi\right|}$$

The figure C2 shows the current waveforms calculated with such an hypothesis, and assuming that the holding current does not depend on the current rate of decrease. The junction temperature influence on the i_H and V_{CL} levels is also not considered. Then, $i(t_0)$, in the equation C1, is always equal to the i_H value given for a 25°C junction temperature (ex: around 30 mA for an ACS402 or ACS108). The ACS clamping voltage is taken as being equal to 700 V. Calculations are carried out for 100 mA RMS loads with different power factors, and for a 230 V 50 Hz mains voltage.

Considering figure C.2, we can see that the load current is always inferior to a linearly decreasing current beginning at (i_H, t_0) point and ending at (0, t_{ZC}). Furthermore, the temperature elevation due to a rectangular power pulse is always superior to one due to a decreasing triangular power pulse of same average value [3].

So, a pessimistic way to calculate the junction temperature is to simplify the clamping losses shape by a constant power pulse of $V_{CL}.I_H/2$ value and t_{ZC}-t_0 time long. The energy absorbed by the die during a clamping event (E_{CL}) depends on two ACS parameters (V_{CL} & I_H) and on the clamping duration:

Equation C3:

$$E_{CL} = \frac{1}{2}\, x\, V_{CL} I_H\, x\, \left(t_{ZC} - t_0 \right)$$

2- Transient maximum junction temperature.

The clamping time is given by equation C1, which gives way to the following one:

Equation C4:

$$t_{ZC} - t_0 = -\frac{L}{R}\ln\left[1 - \frac{R}{V_{CL} + E - Vac} I_H\right]$$

Neglecting the on-state dissipated power in front of clamping dissipated power, the junction temperature rise at the end of the clamping phase is:

Equation C5:

$$\Delta T_j = Zth\left(t_{ZC} - t_0\right) x \frac{1}{2} V_{CL} I_H$$

Figure C3 shows the maximum ΔT_j reached for different load RMS currents and power factors. Calculations are similar whatever the package is (TO92, DIL20, SOT223), because in such a range of times, the Zth is only due to the die area.

Note that ΔT_j first increases. On this curve part, the load peak current is lower than the i_H level (taken equal to its worst value: 60 mA). So, when the load RMS current increases, the turned-off current increases too. When the load peak current becomes higher than i_H, ΔT_j decreases because of the load series inductance decrease (here the turn-off current is constant and equals i_H).

It can be concluded that, if the junction temperature was 110°C before turn-off, the maximum transient temperature can reach 160 °C. As these events last less than a ms (refer to figure C.2), such junction temperatures can be permitted.

Fig. C-2: Current waveform during clamping phase for 100mA / 230V RMS loads.

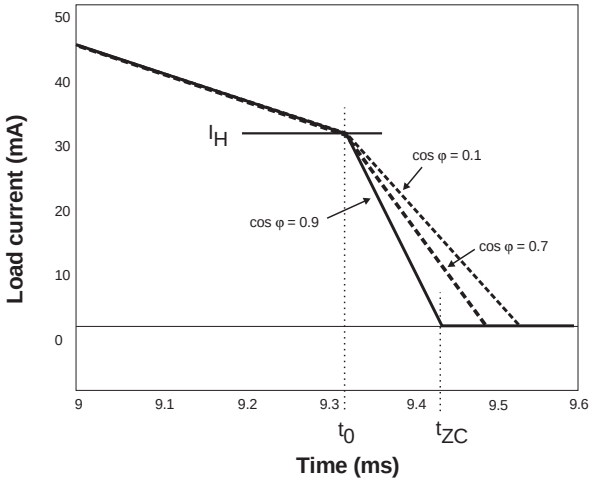
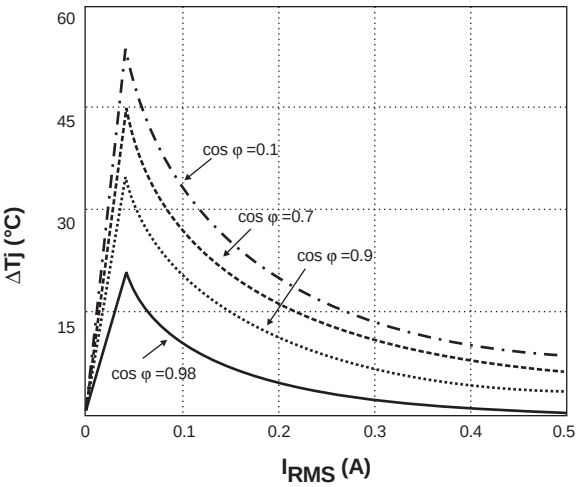


Fig. C-3: Supplementary temperature rise at clamping depending on load nature (for ACS402-5SB4 or ACS108-5SX).



3- Repetitive clampings.

To evaluate heating due to repetitive clampings, the expression C6 can be used, assuming that the clampings occur at a constant period T and that the conduction losses can be neglected in front of the previous ones:

Equation C6:

$$\Delta T_{rep} = \frac{1}{2} V_{CL} I_H \; x \left[\frac{t_{ZC} - t_0}{T} Rth + \left(1 - \frac{t_{ZC} - t_0}{T}\right) Zth\left(T + t_{ZC} - t_0\right) - Zth\left(T\right) + Zth\left(t_{ZC} - t_0\right)\right]$$

In practice T (above 1 s) is very much higher than the clamping duration. The equation C6 can then be simplified to the following one:

Equation C7:

$$\Delta T_{rep} = \frac{1}{2} V_{CL} I_H \, x \left[\frac{t_{ZC} - t_0}{T}\right] x Rth$$

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