AN1135
APPLICATION NOTE

DESIGNING WITH L6911B, 5 BIT STEP DOWN CONTROLLER

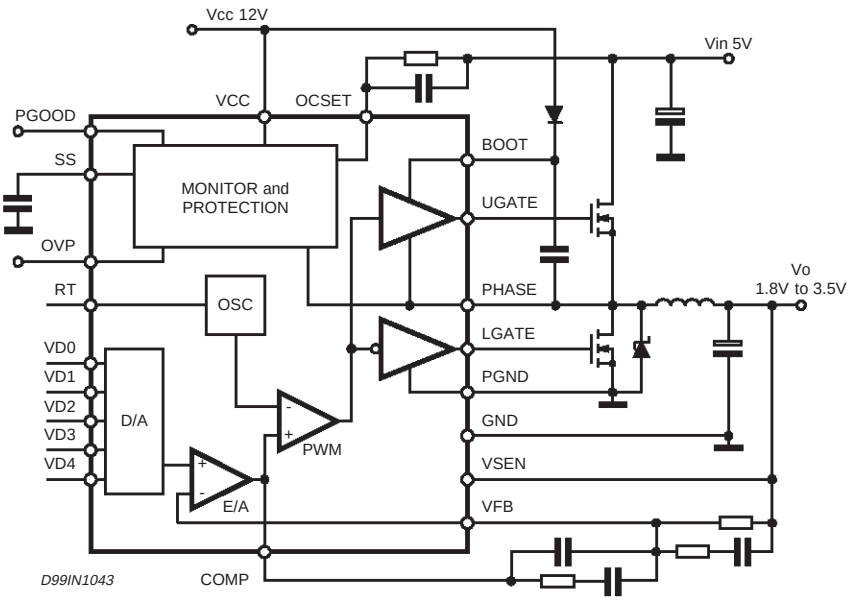
The increase of computing capability and the consequential rising in complexity of modern microprocessors have lead to the reduction of the supply voltages, the increase of the clock frequency and of the current required.

The L6911B is a new PWM controller specifically designed to provide a high performance DC-DC conversion for advanced microprocessors. This paper deals on how to use this device in design applications.

Device Description

The device, whose internal block diagram is shown in figure 1, is an integrated circuit realised in BCD technology. It is a controller for a synchronous-rectified Buck converter operating in voltage mode, which provides all the features (a five bit digital to analog converter, an high performance error amplifier, a built-in programmable oscillator) needed to implement and properly control a VRM SMPS for advanced microprocessor supplies with a minimum components count. It is available in SO20 package.

Figure 1. Internal Block Diagram.

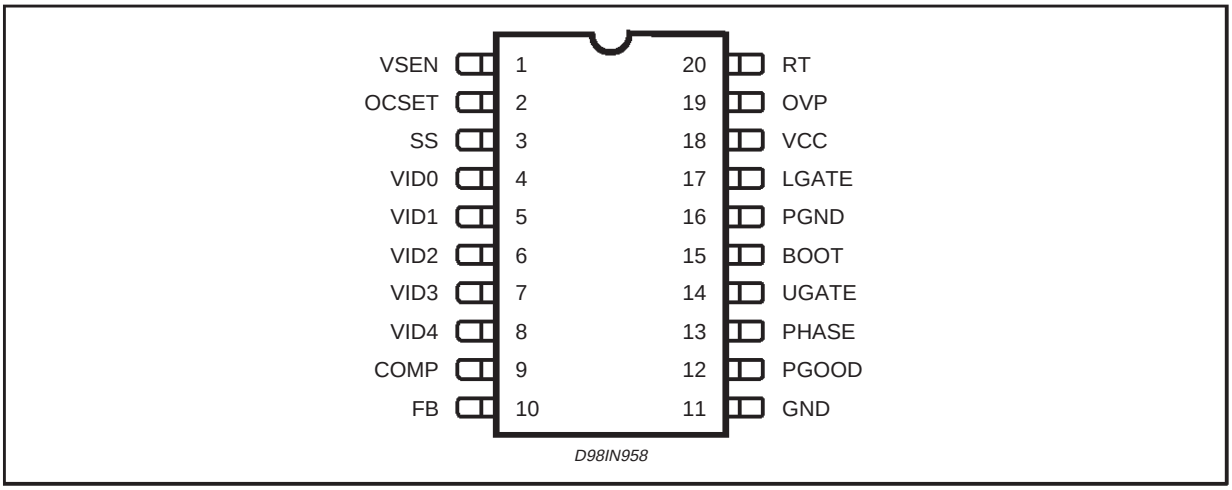


The most significant features of the device are the following points:

- TTL-compatible 5 bit programmable output from:
  1.3V to 2.05V with 0.05 binary steps;
  2.1V to 3.5V with 0.1 binary steps;
- voltage mode PWM control;
- excellent output accuracy +/-1% over line, and temperature variations;
- digitally trimmed high precision internal reference;

- operating supply voltage from 5V or 12V;
- very fast load transient 0% to 100% duty cycle;
- power good output;
- overvoltage protection;
- overcurrent protection realised using the upper MOSFET's RDSON;
- operating frequency from 50kHz to 1MHz;
- disable function.

Figure 2. Pin Out.



Pins Description

N°	Pin	Function
1	VSEN	Connected to the output is able to detect overvoltage conditions and the PGOOD signal. This pins is not used for the feedback.
2	OCSET	A resistor connected from this pin and the upper MOS drain sets the current limit protection. The internal 200µA current generator sinks a current from the drain through the external resistor, generating a threshold that is compared with the MOS drop. To reduce noise and avoid undesirable triggering a small ceramic capacitor has to be connected in parallel to the resistor.
3	SS	The soft start time is set connecting an external capacitor between this pin and GND. The internal current generator forces 10µA through the capacitor. This pin can be used to disable the device forcing a voltage lower than 0.4V.
4-8	VID0-4	Voltage identification pins. These open collector inputs (TTL compatible) are internally pulled up. They are used to program the output voltage as specified in the table of the datasheet. They set also the powergood and the overvoltage threshold.
9	COMP	This pin is connected to the error amplifier output to compensate the feedback loop.
10	FB	This pin is connected to the error amplifier inverting input. The non inverting input of the error amplifier is connected to the DAC output.
11	GND	All internal voltage references are referred to this pin.
12	PGOOD	This pin is an open collector output and it is forced low if the output voltage is not within +/-10% of the programmed one.

Pins Description (continued)

N°	Pin	Function
13	PHASE	This pin is connected to the source of the upper MOS and provides the return path for the high side driver. This pin monitors the drop across the upper MOS for the current limitation.
14	UGATE	High side gate driver output. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
15	BOOT	Bootstrap capacitor pin. The bootstrap capacitor must be connected between this pin and phase; the BOOT diode must be connected between his pin and V_{CC}
16	PGND	Power ground pin. This pin has to be connected closely to the low side MOS source in order to reduce the noise injection into the device.
17	LGATE	Low side gate driver output. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
18	VCC	Connected this pin to the 12V or 5V bus it provides the device bias supply. A capacitor has to be connected between this pin and PGND close to the device, to supply the impulsive current requirement of the lower driver. Do not connect V_{IN} to 12V if V_{CC} is 5V.
19	OVP	Over voltage protection. If the output voltage reaches the 15% above the programmed voltage, this pin is driven high and can be used to drive an external SCR that shuts down the supply voltage.
20	RT	Oscillator switching frequency pin. Connecting a resistor between this pin and GND or V_{CC} is possible to change the switching frequency. The voltage at this pin is fixed at 1.26V. Forcing a 50µA current at this pin the built in oscillator stops to switch.

Oscillator

The switching frequency is internally fixed to 200kHz. This value is suitable for a wide range of applications. However it can be varied using an external resistor (R_T) connected between R_T pin and GND or V_{CC}. In particular connecting it to GND the frequency is increased, in according to the following relationship (figure 3):

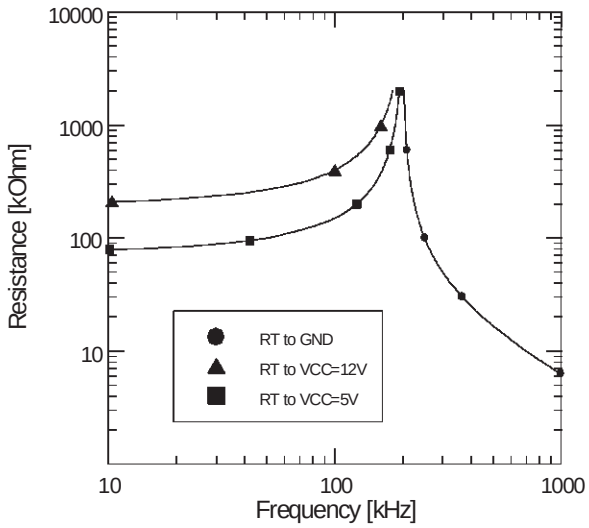
$$f_S = 200kHz + \frac{5 \cdot 10^6}{R_T\ [k\Omega]}$$

Connecting R_T to V_{CC} = 12V or to V_{CC} = 5V the frequency is reduced, in according to the following relationships (figure 3):

$$f_S = 200kHz - \frac{4 \cdot 10^7}{R_T\ [k\Omega]} \quad \text{if } V_{CC} = 12V,$$

$$f_S = 200kHz - \frac{15 \cdot 10^6}{R_T\ [k\Omega]} \quad \text{if } V_{CC} = 5V$$

Figure 3. Resistance vs. Frequency



The PWM Ramp is generated charging and discharging an internal capacitor with a constant current. In practice the current delivered to the oscillator is varied from the standard value equal to 50µA, allowing a switching frequency different from 200kHz. Thanks to the digital trimming of both the oscillator current and of the oscillator capacitor the maximum deviation of the switching frequency from the calculate value using the above equations is ±15% for all the R_T range (R_T > 6kΩ if connected to ground and R_T > 200kΩ if connected to V_{CC} = 12V).

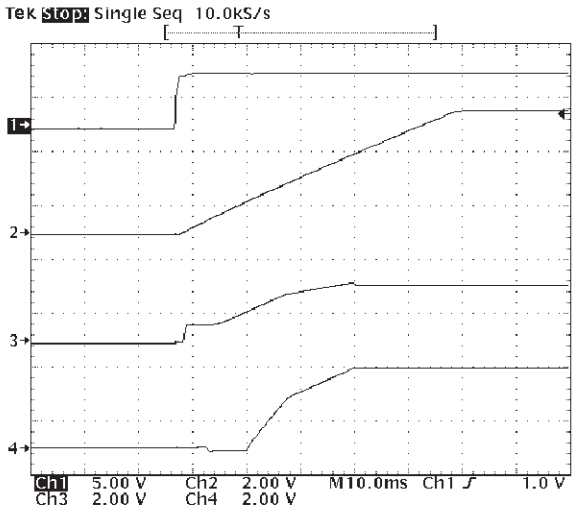
Digital to Analog Converter

The built-in digital to analog converter allows the adjustment of the output voltage from 1.3V to 2.05V with 0.05V binary steps and from 2.1V to 3.5V with 0.1V binary steps. The internal reference is digitally trimmed, ensuring 1% precision (see the datasheet). The output voltage programming is reported in the datasheet.
The voltage identification (VID) pin configuration also sets the power-good (PGOOD) and the over- voltage protection (OVP) thresholds.
The DAC is realised by means of a series of resistors that provides a partition of the voltage reference. The VID code drives a multiplexer that selects a voltage on a precise point of the divider. The DAC output is delivered to an amplifier obtaining the VPROG voltage reference (i.e. the set-point of the error amplifier).

Soft Start

At start-up a ramp is generated charging the external capacitor C_{SS} by means of a 10µA constant current, as shown in figure 4 (V_{IN} = V_{CC} = 5V, V_{OUT} = 3V, C_{SS} = 100nF, without any load).
When the voltage across the soft start capacitor V_{SS} reaches 0.5V the lower power MOS is turned on. As V_{SS} reaches 1V (i.e. the oscillator triangular wave inferior limit) also the upper MOS begins to switch.
The V_{SS} growing voltage initially clamps the output of the error amplifier, and consequently V_{OUT} linearly increases, as shown in figure 4. In this phase the system works in open loop. When V_{SS} is equal to V_{COMP} the clamp on the output of the error amplifier is released. In any case another clamp on the input of the error amplifier remains active, allowing to V_{OUT} to grow with a lower slope (i.e. the slope of the V_{SS} voltage, see figure 4). In this second phase the system works in closed loop with a growing reference. As the output voltage reaches the desired value V_{PROG} also the clamp on the error amplifier input is removed, and the soft start finishes.
The soft start pin is internally shorted to GND until both V_{CC} and OCSET overcames the turn-on threshold.

Figure 4. Soft Start, Ch1 = V_{IN} Ch2 = V_{SS} Ch3 = V_{COMP} Ch4 = V_{OUT}



DRIVER SECTION

Figure 5. Ch1 = V_{LGATE} Ch2 = I_{GATE} V_{CC} = 5V

Figure 6. Ch1 = V_{LGATE} Ch2 = I_{GATE} V_{CC} =12V

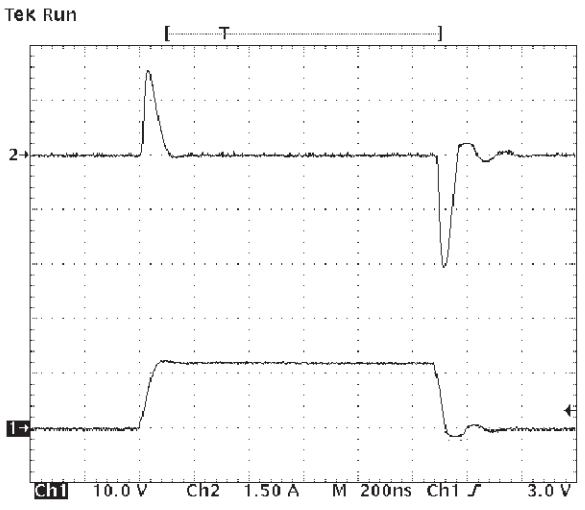


Figure 7. Ch1 = V_{UGATE} Ch4 = I_{GATE} V_{CC} = 5V

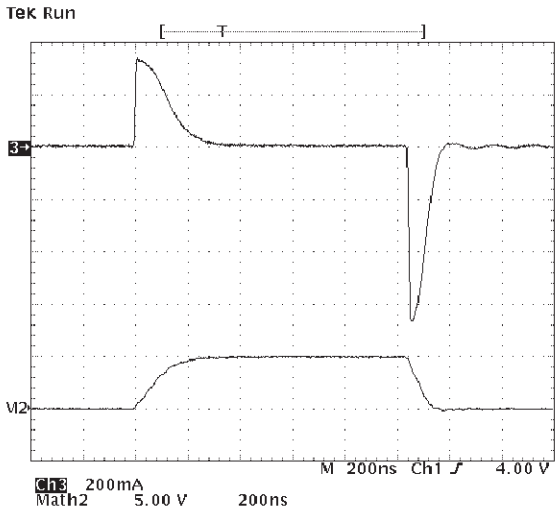
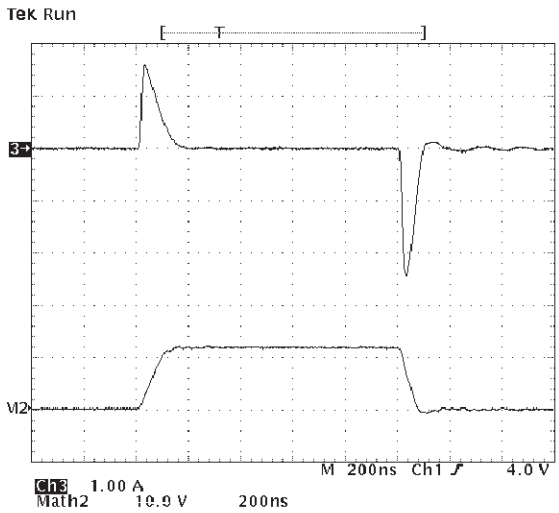


Figure 8. Ch1 = V_{UGATE} Ch4 = I_{GATE} V_{CC} =12V



The high driver capability on the high and low side drivers allows to use different types of power MOS (also multiple MOS to reduce the R_{DSON}), maintaining fast switching transition. In the PCB it is possible to mount up to three SO8 power MOS for both the low and the high side.

The peak current is shown for both the lower (figures 5 and 6) and the upper (figure 7 and 8) driver at 5V and 12V. A 10nF capacitive load has been used in these measurements.

For the lower driver the source peak current is 600mA@V_{CC} = 5V and 2.3A@V_{CC} = 12V, and the sink peak current is 1.2A@V_{CC} = 5V and 3A@V_{CC} = 12V.

Similarly or the upper driver the source peak current is 350mA@V_{CC} = 5V and 1.6A@V_{CC} = 12V, and the sink peak current is 650mA@V_{CC} = 5V and 2.4A@V_{CC} = 12V.

Monitor and Protection

The output voltage is monitored by means of pin 1 (V_{SEN}). If it is not within 10% of the programmed value, the powergood output is forced low.

The device provides overvoltage protection, when the output voltage reaches a value 15% grater than the nominal one. If the output voltage exceed this threshold, the OVP pin is forced high, triggering an external SCR to shuts the supply (V_{CC}) down, and the lower driver is turned on.

To perform the overcurrent protection it compares the drop across the high side MOS, due to the R_{DSON}, with the voltage across the external resistor (R_{OCS}) connected between the OCSET pin and drain of the upper MOS. Thus the overcurrent threshold (I_P) can be calculated with the following relationship:

$$I_P = \frac{I_{OCS} \cdot R_{OCS}}{R_{DSON}}$$

where the typical value of I_{OCS} is 200µA (see the datasheet). To calculate the R_{OCS} value it must be considered the maximum R_{DSON} (also the variation with temperature) and the minimum value of I_{OCS}. Substituting the parameters of the demo board (I_{OCSMIN} = 170µA, R_{OCS} = 1kΩ, $R_{DSONMAX}$ = 9mΩ) in the equation above, I_P results equal to 19A. To avoid undesirable trigger of overcurrent protection this relationship must be satisfied:

$$I_P \geq I_{OUTMAX} + \frac{\Delta I}{2} = I_{PEAK}$$

where ΔI is the inductance ripple current and I_{OUTMAX} is the maximum output current.

In case of output short circuit the soft start capacitor is discharged and the system works in hiccup mode, as shown in figure 9 and 10 (Ch1 = V_{SS} and Ch2 = Inductor current).

Figure 9. Hiccup Mode V_{CC} = V_{IN} = 5V

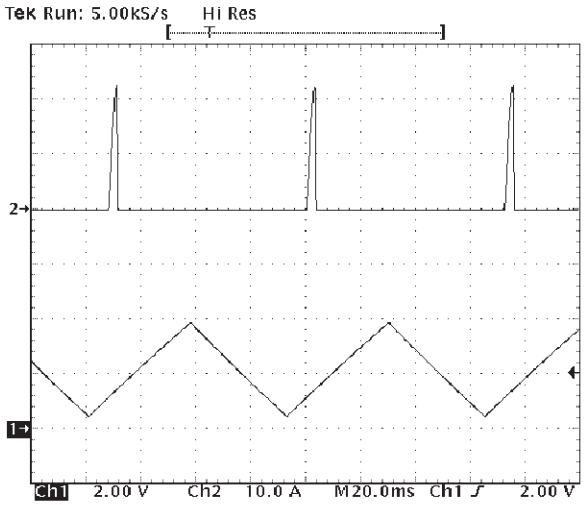
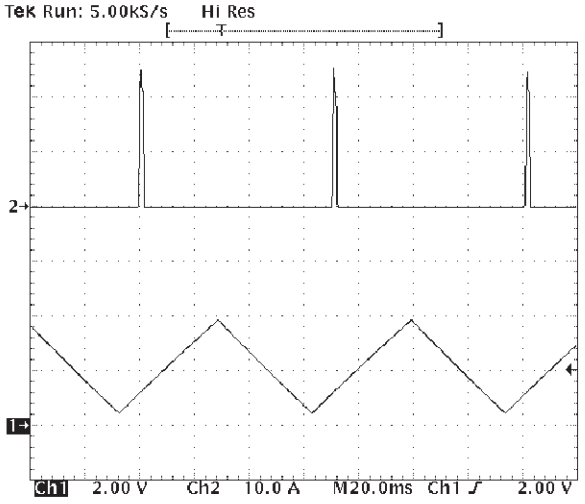


Figure 10. Hiccup Mode V_{CC} = V_{IN} = 12V



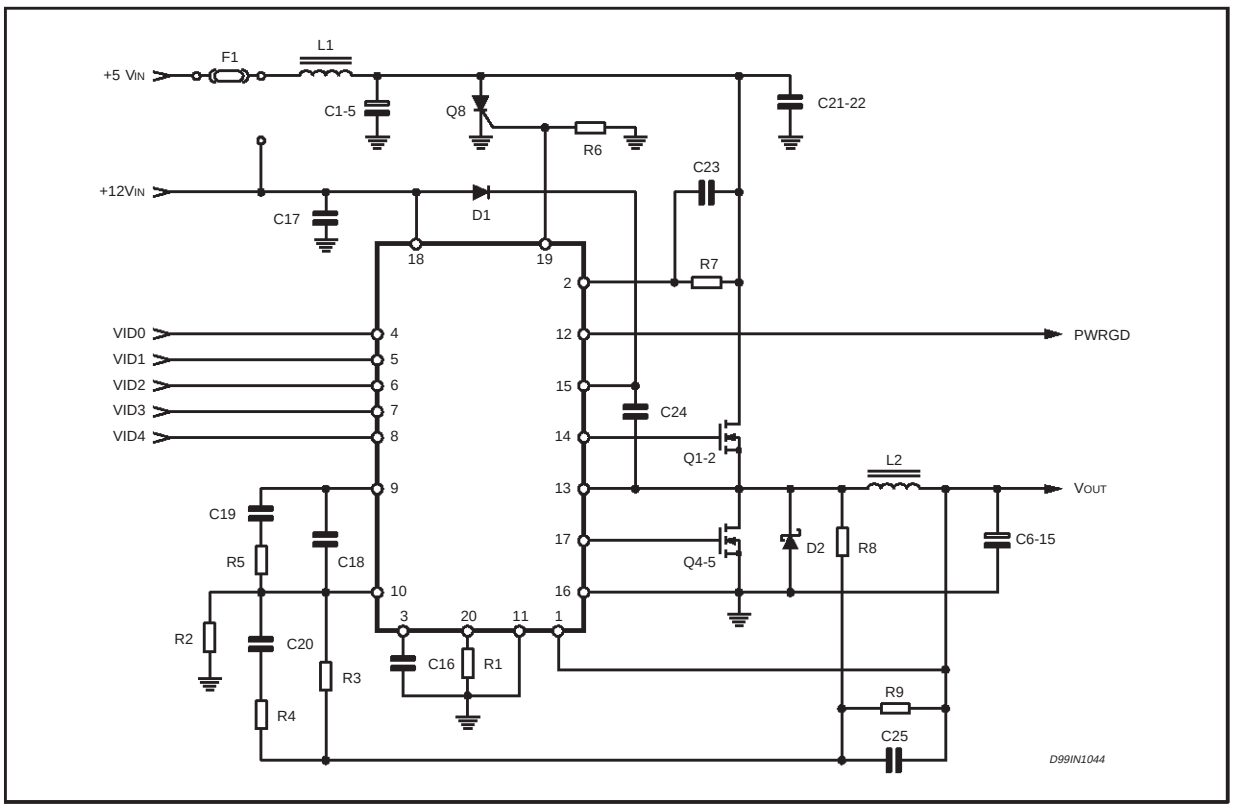
Application Circuit

Figure 11 shows the schematic circuit of the evaluation board. The design has been developed for an output current up to 14A, as requested by new microprocessors.

The device is supplied by the 12V input rail, and it is also able to operate with a 5V supply voltage; in this case 12V input can be directly connected to the 5V power source.

Also the main power source can be either +5V or +12V, changing the position of the fuse (see figure 11 and the PCB layout).

Figure 11. Schematic circuit



Inductor

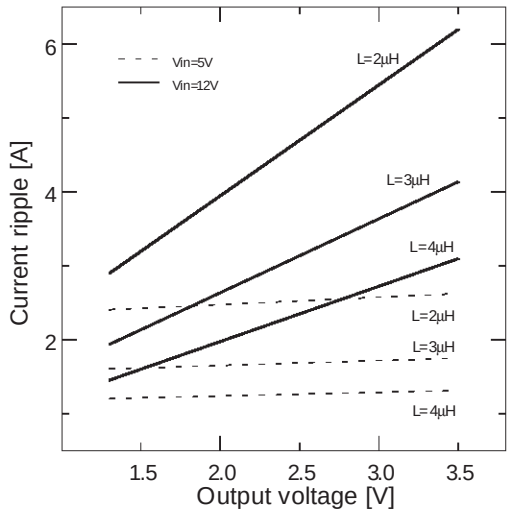
The inductance value is defined by a compromise between the transient response time, the efficiency, the cost and the size. The inductor has to be calculated to sustain the output and the input voltage variation to maintain the ripple current ΔI_L between 20% and 30% of the maximum output current. In order to optimise the load transient response time, the current ripple is fixed to 30%. The inductance value can be calculated with this relationship:

$$L = \frac{V_{IN} - V_{OUT}}{f_s \cdot \Delta I_L} \cdot \frac{V_{OUT}}{V_{IN}}$$

where f_{SW} is fixed at 200kHz to improve the efficiency, V_{IN} is the input voltage and V_{OUT} is the output voltage. Figure 12 shows the ripple current vs the output voltage for different values of the inductor value, with V_{IN} = 5V and V_{IN} = 12V.

Since the maximum output current is equal to 14A, to have a 30% ripple (4A) in worst case we have chosen a inductance equal to 3µH. So the ripple is 4.1A@3.5V with V_{IN} = 12V and 1.7A@3.5V with V_{IN} = 5V. In worst case the peak current is 18.1A.

Figure 12. Inductor ripple current vs V_{OUT}



Output Capacitor

Since the microprocessors require a current variation beyond of 10A during load transients, with a slope in the range of tenth A/µs, the output capacitor is a basic component for the fast response of the power supply. In fact for first few microseconds the current to the load is supplied by them. The controller recognises immediately the load transient and sets the duty cycle at 100%, but the current slope is limited by the inductor value.

The output voltage has a first drop due to the current variation inside the capacitor (neglecting the effect of the ESL):

$$\Delta V_{OUT} = \Delta I_{OUT} \cdot ESR$$

In the demo ten Sanyo capacitors, model 6MV1000GX are used, with a maximum ESR equal to 69mΩ. Therefore the resultant ESR is 69mΩ/10 = 6.9mΩ. For a load transient of 14A in worst case the drop results:

$$\Delta V_{OUT} = 14 \cdot 0.00069 = 96.6mV$$

A minimum capacitor value is required to sustain the current during the load transient without discharge it. The voltage drop due to the output capacitor discharge is given by the following equation:

$$\Delta V_{OUT} = \frac{\Delta I_{out}^2 \cdot L}{2 \cdot C_{OUT} \cdot (V_{INMIN} \cdot D_{MAX} - V_{OUT})}$$

Substituting the parameters and considering that D_{MAX} is equal to 100%, for a load transient of 14A and V_{OUT} equal to 2.5V, the drop results equal to 13mV.

Input Capacitor

The input capacitor has to sustain the ripple current produced during the on time of the upper MOS, so it must have a low ESR to minimise the losses. The rms value of this ripple is:

$$I_{rms} = I_{OUT} \cdot \sqrt{D - 2 \cdot \eta \cdot \frac{D^2}{\eta} + \left(\frac{D}{\eta}\right)^2}$$

where η is the expected efficiency and D is the duty cycle. For I_{OUT} = 14A and with D = 0.5, in which the equation reaches his maximum value, I_{rms} is equal to 7A. Five Sanyo electrolytic capacitors 25MV330GX, with a maximum ESR equal to 69mΩ, are chosen to sustain this ripple. Therefore the resultant ESR is 69mΩ/5 = 13.8mΩ. So the losses in worst case are:

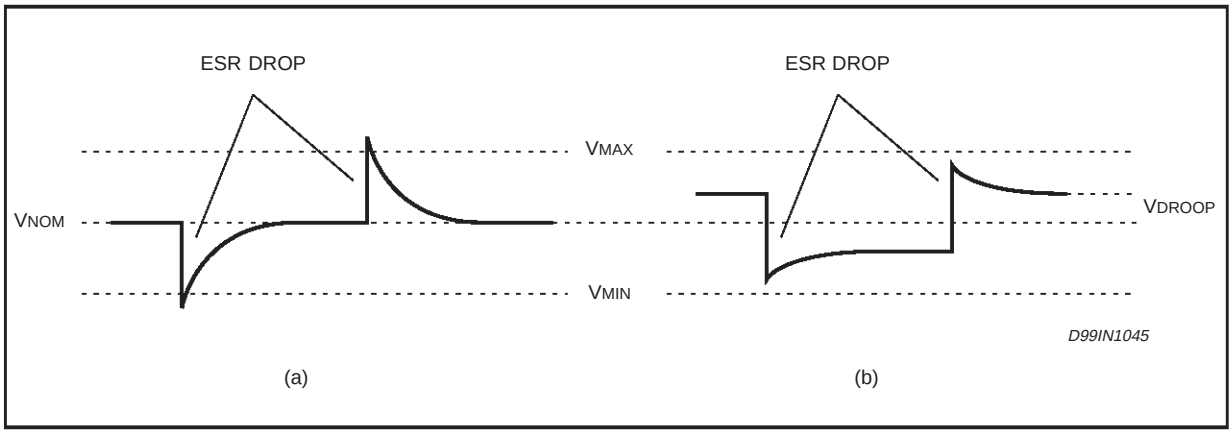
$$P = ESR \cdot I_{rms}^2 = 670mW$$

Transient Response

The control loop is a voltage mode (figure 11 and figure 16) that uses a droop function to satisfy the requirements for a VRM module, reducing the size and the cost of the output capacitor.

This method "recovers" part of the drop due to the output capacitor ESR in the load transient, introducing a dependence of the output voltage on the load current (figure 13 and 15): at light load the output voltage will be higher the nominal level, while at high load the output voltage will be lower the nominal value.

Figure 13. Output transient response without (a) and with (b) the droop function



As shown in figure 13, the ESR drop is present in any case, but using the droop function the total deviation of the output voltage is minimised. In practice the droop function introduces a static error (Vdroop in figure 13) proportional to the output current (see also figure 15). Since a sense resistor is not present, the output dc current is measured by using the intrinsic resistance of the inductance (a few mW). So the low-pass filtered inductor voltage (that is the inductor current) is added to the feedback signal, implementing the droop function in a simple way. The static characteristic of the closed loop system is:

$$V_{OUT} = V_{PROG} + V_{PROG} \cdot \left(\frac{R_3 + R_8 // R_9}{R_2}\right) - \frac{R_L \cdot R_8 // R_9}{R_8} \cdot I_{OUT}$$

where V_{PROG} is the output voltage of the digital to analog converter (i.e. the set point) and RL is the inductance resistance. The second term of the equation allows a positive offset at zero load; the third term introduces the droop effect. Note that the droop effect is equal the ESR drop if:

$$\frac{R_L \cdot R_8 // R_9}{R_8} = ESR$$

In figure 15 this linear characteristics is compared with the measured behavior for an output current from 1A to 14A. A R_L equal to 10mΩ has been substituted in the relationship above, considering the tempera-

ture effect and the soldering of the choke (i.e. the increase of the inductance resistance).

Figure 14 shows the acquired waveforms of the output voltage for a 0-14A load transient. Ch1 is the output voltage (with a 2V offset set on the scope) and the Ch2 is the output current.

Figure 14. Output Transient Response

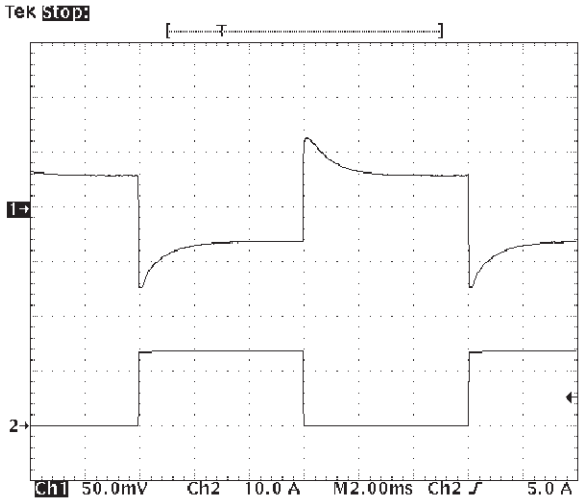
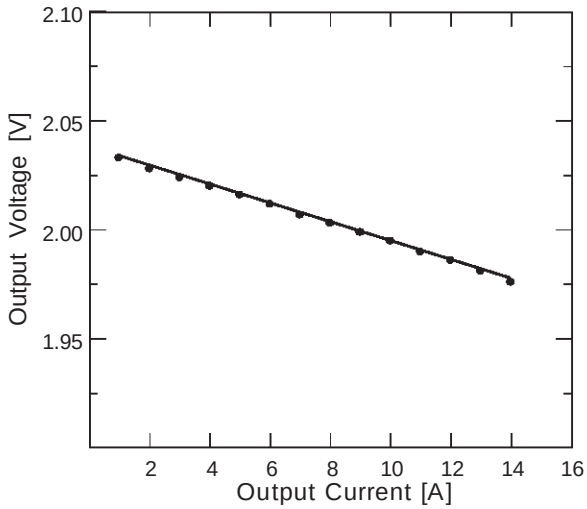
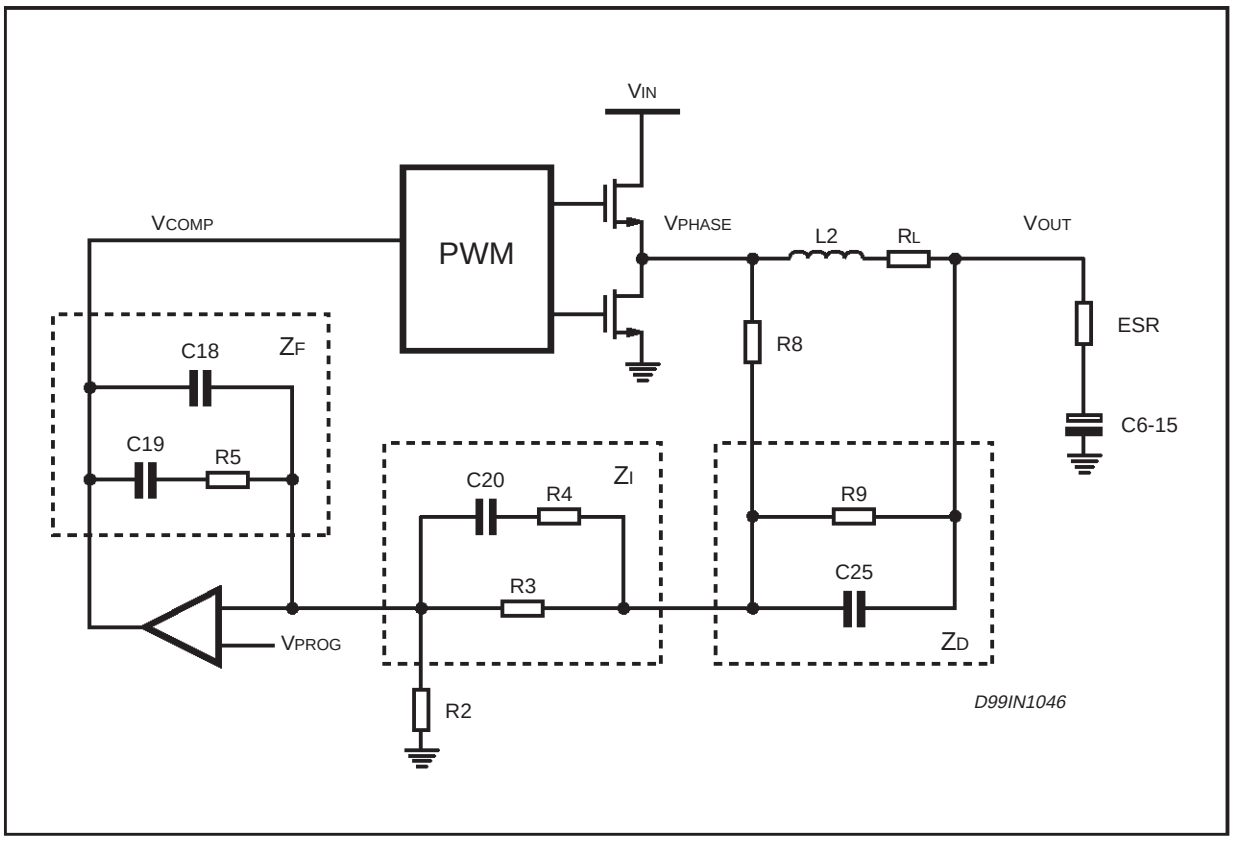


Figure 15. Static Regulation



Compensation network

Figure 16. Compensation Network



The compensation network is shown in figure 16. Since the voltages V_{PHASE} and V_{OUT} are both taken in low impedance nodes, it is possible to calculate the transfer functions between V_{PHASE} and V_{COMP}, and between V_{OUT} and V_{COMP} by using superposition. Neglecting the effect of R2 (i.e. the input of the error amplifier is a virtual ground) the following relationships can be written:

$$\frac{V_{COMP}(s)}{V_{PHASE}(s)} = -\frac{1}{R_8 + Z_D(s)\,//Z_I(s)} \cdot \frac{Z_D(s)}{Z_D(s) + Z_I(s)} \cdot Z_F(s) = F(s) \cdot Z_D(s)$$

$$\frac{V_{COMP}(s)}{V_{OUT}(s)} = -\frac{1}{Z_D(s) + R_8\,//Z_I(s)} \cdot \frac{R_8}{R_8\,//Z_I(s)} \cdot Z_F(s) = F(s) \cdot R_8$$

where:

$$F(s) = \frac{Z_F(s)}{R_8 \cdot Z_D(s) + R_8 \cdot Z_I(s) + Z_I(s) \cdot Z_D(s)}$$

$$Z_F(s) = \frac{1}{sC_{18}} // \left(R_5 + \frac{1}{sC_{19}}\right); \quad Z_I(s) = R_3 // \left(R_4 + \frac{1}{sC_{20}}\right); \quad Z_D(s) = R_9 // \frac{1}{sC_{25}}$$

To continue the analysis we can use the system in figure 17, in which the PWM modulator gain M has been introduced:

$$M = \frac{V_{IN}}{\Delta V_{OSC}}$$

where ΔV_{OSC} is the ramp amplitude of the oscillator (typ. 1.9V). G(s) is the output LC filter block (i.e. L_2 and $C_{TOT} = C_6//C_7//...C_{15}$).

Figure 17. Two loops control system

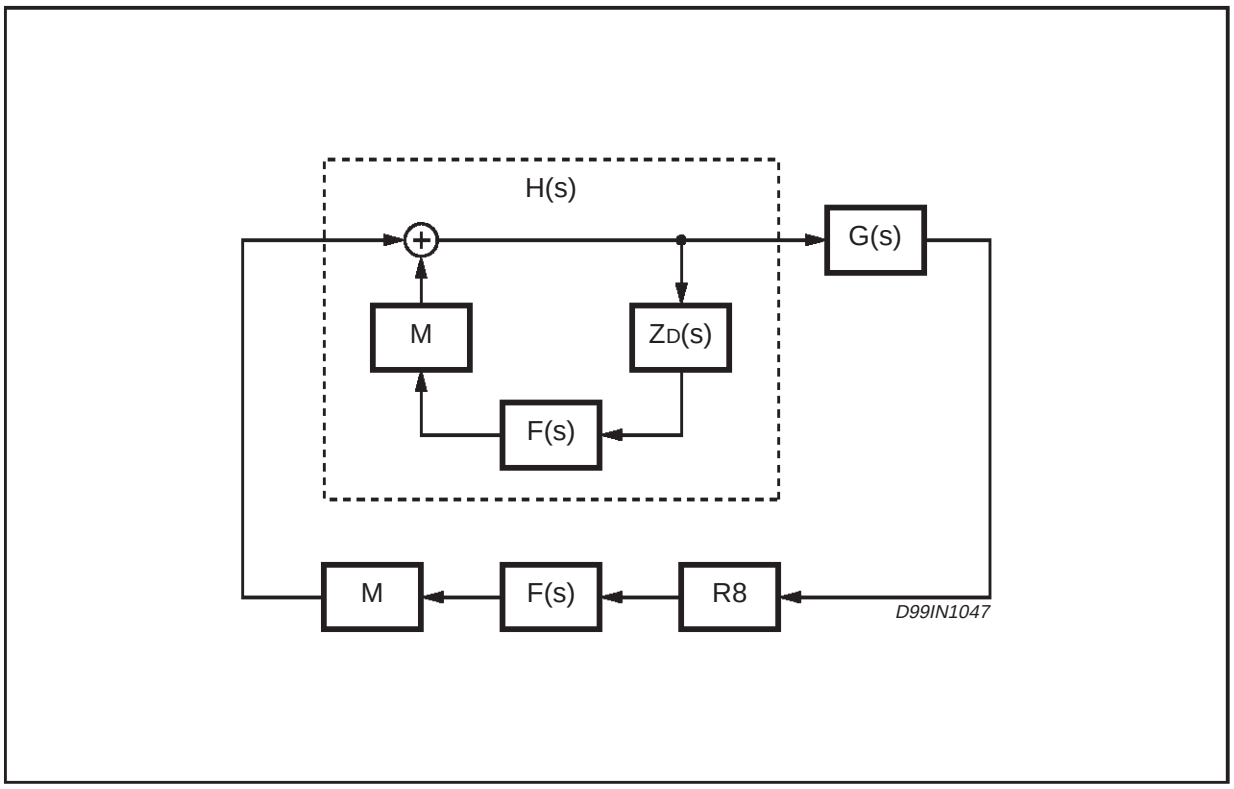


Figure 18. Inner loop Bode plot

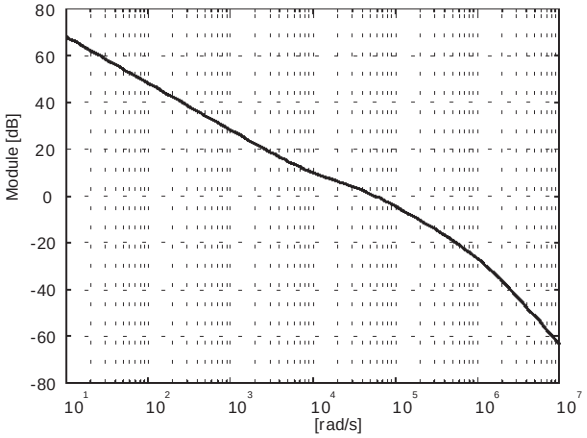
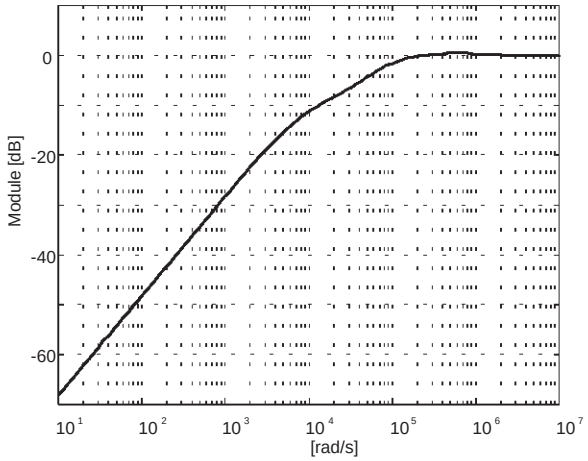


Figure 19. H(s) Bode plot



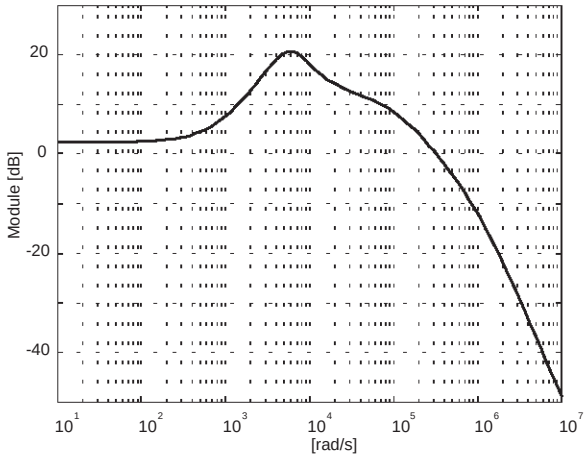
Referring to figure 17 the transfer function H(s) of the inner loop results:

$$H(s) = \frac{1}{1 - M \cdot F(s) \cdot Z_D(s)} \cong -\frac{1}{M \cdot F(s) \cdot Z_D(s)}$$

The above approximation is possible if the inner loop gain is quite high (>>1). This condition is usually satisfied; in fact it is indispensable to have a good regulation and low audio susceptibility. H(s) gain crosses the 0 dB axis at ω_H with a -20dB/dec slope, ensuring the loop stability. Looking at the H(s) bode plot, it results equal to 0dB beyond ω_H. A simple way to consider this behavior is adding a pole at ω_H:

$$H(s) = -\frac{1}{M \cdot F(s) \cdot Z_D(s) \cdot \left(1 + \frac{s}{\omega_H}\right)}$$

Figure 20. System loop gain $G_{LOOP}(s)$ Bode plot



The calculation of the outer loop will be simplified: M and F(s) cancel, obtaining this expression:

$$G_{LOOP}(s) = \frac{R_8}{Z_D(s)} \cdot G(s) \cdot \frac{1}{1 + \frac{s}{\omega_H}}$$

Substituting all the terms:

$$G_{LOOP}(s) = R8 \cdot \frac{1 + sc25 \cdot R9}{R9} \cdot \frac{1 + sC_{TOT} \cdot ESR}{s^2 L_2 C_{TOT} + sC_{TOT} \cdot (ESR + R_L) + 1} \cdot \frac{1}{1 + \frac{s}{\omega_H}}$$

The $Z_D(s)$ pole becomes a zero, while the LC(s) singularities remain unaltered. A suitable choice for locating the poles and the zeros of $G_{LOOP}(s)$ is: place the pole at ωH for compensating the ESR zero, and place the $Z_D(s)$ pole for the desired transient response. In fact closing the loop the time constant R_9C_{25} becomes a pole of the entire system, and it fixes the time response.

Efficiency

The measured efficiency versus load current for different values of output voltage is shown in figure 16. The measures was done at V_{IN} = 5V for different values of the output voltage (2V and 2.8V). The supply voltage of the device V_{CC} has always been connected directly to the power source V_{IN} (i.e. $V_{CC} = V_{IN}$).

In the application two MOSFETs STS12NF30L (30V, 10mΩ typ. with V_{GS} = 4.5V) connected in parallel are used for both the low and the high side.

Figure 21. Efficiency vs. load

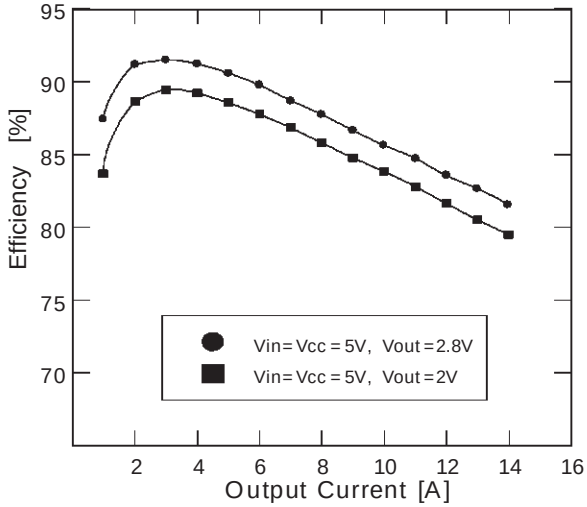


Figure 22. PCB and Components Layouts.

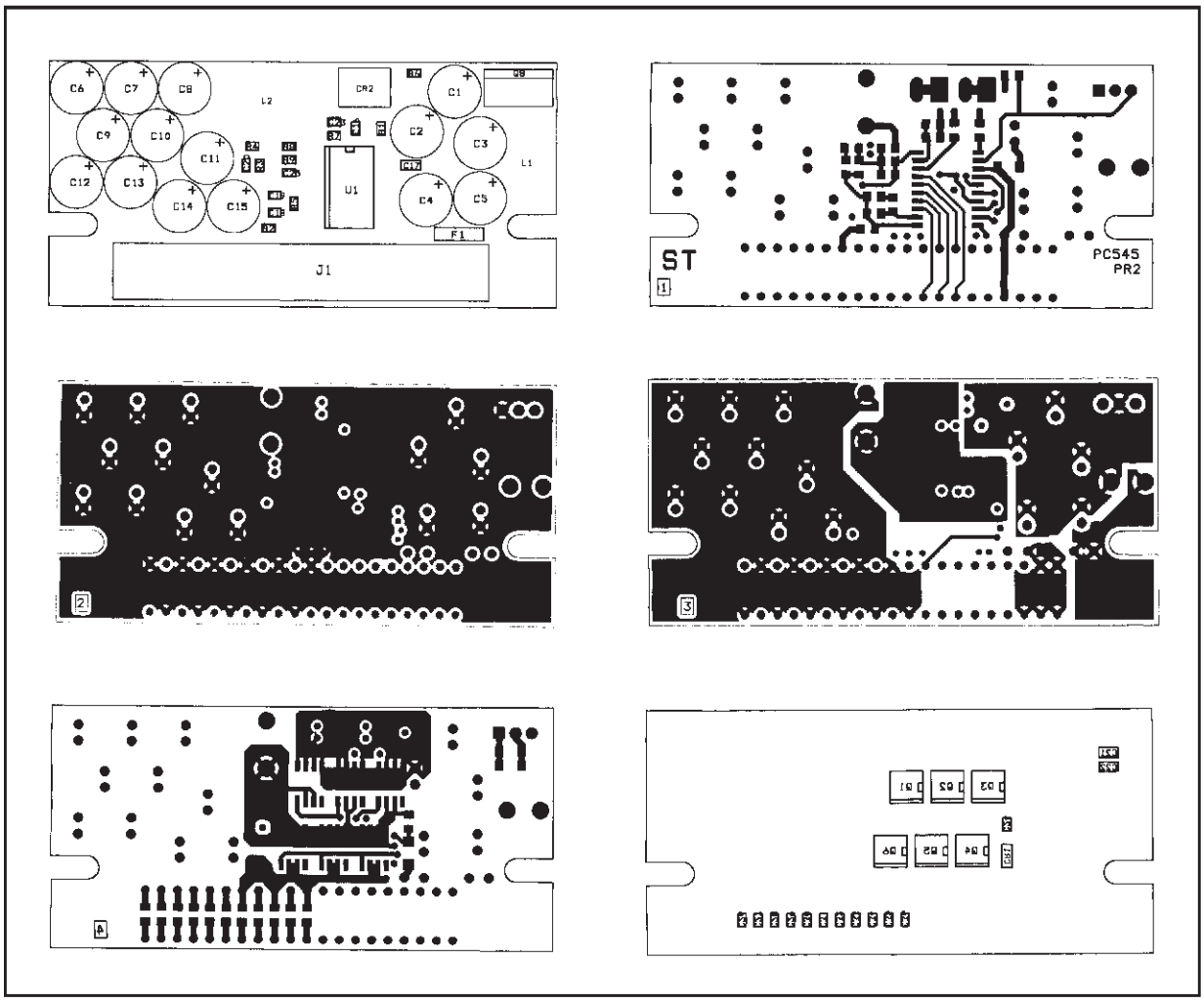
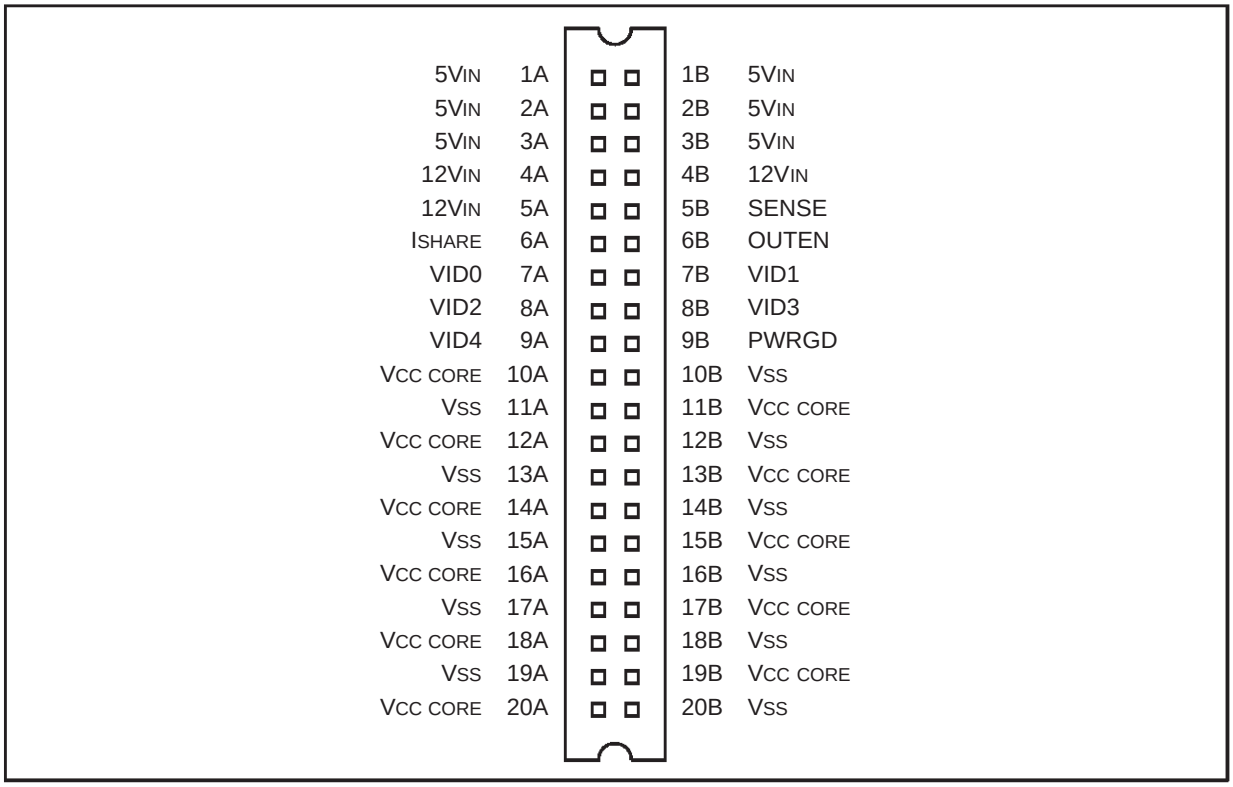


Figure 23. Connector pin orientation



Part List

R2	499k	1%	SMD 0805
R3, R7	1k	1%	SMD 0805
R4	20		SMD 0805
R5, R8	20k		SMD 0805
R6	10k		SMD 0805
R9	15k		SMD 0805
C1,C2,..C5	330µ	SANYO - 25MV330GX	Radial 8x20mm
C6,C2,..C15	1000µ	SANYO - 6MV1000GX	Radial 8x20mm
C16,C24,C25	100n	Ceramic	SMD 0805
C17	4.7µ	Ceramic	SMD 1206
C18	2.2n	Ceramic	SMD 0805
C19	8.2n	Ceramic	SMD 0805
C20	82n	Ceramic	SMD 0805
C23	1n	Ceramic	SMD 0805
C21, C22	1µ	Ceramic	SMD 1206
L1	1.5µ	T44-52 Core, 7T-18AWG	
L2	3µ	T5052B Core, 10T-16AWG	
U1	L6911B	STMicreolectronics	SO20
Q1,Q2,..Q4	STS12NF30L	STMicroelectronics	SO8
Q8	N.C.		TO220
D1	1N4148	STMicroelectronics	DL-35
D2	STPS3L25U	STMicroelectronics	SMB
F1	251015A-15A	Littlefuse	AXIAL
	532956-7	AMP connector	

littlediode
COMPONENTS FOR ALL

Littlediode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.