



# AN1119 APPLICATION NOTE

## Correct Power-On and Power-Off for the M93Cxx and M93Sxx

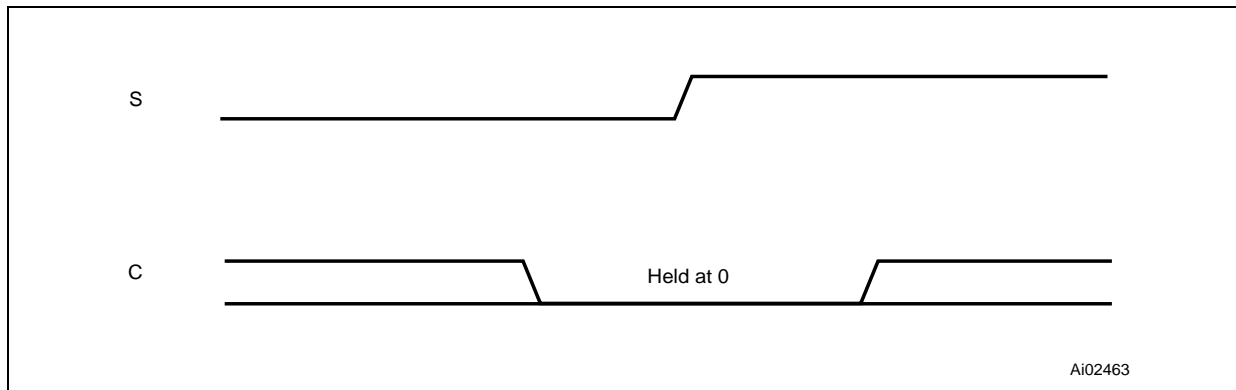
This document has been written for those users who have become used to using the members of the ST93C/CSxx and M93C/Sxx family outside of their specifications.

**Table 1. Members of the ST93C/CSxx and M93Cxx Family**

Earlier Members	Later members
ST93C06	M93C06
ST93C46, ST93CS46	M93C46, M93S46
ST93C56, ST93CS56	M93C56, M93S56
ST93C66, ST93CS66	M93C66, M93S66
	M93C86, M93S86

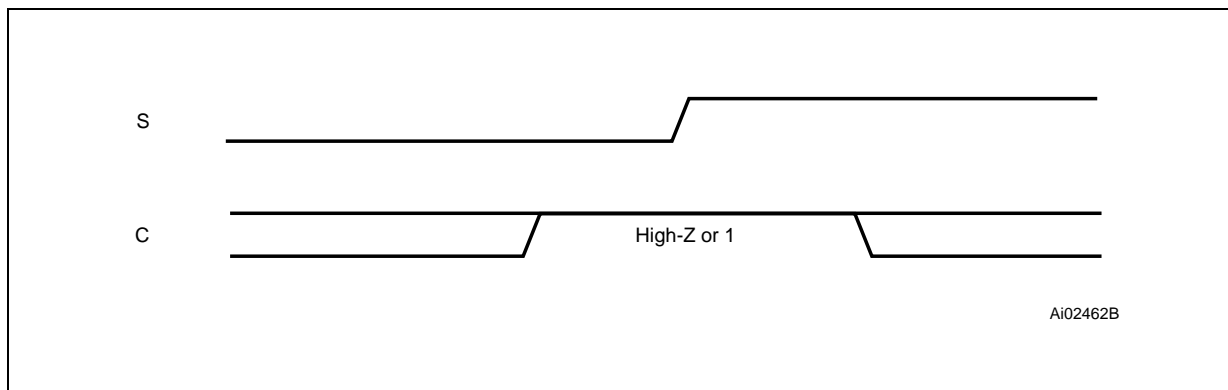
It is very important to use each of these devices only in the way specified in the data sheets. In particular, as shown in Figure 1, it is important for the Serial Clock (C) input to be held Low whenever there is a rising edge on the Chip Select (S) input.

**Figure 1. Correct Sequence**



If a rising edge of the Chip Select (S) input is allowed to occur while the Serial Clock (C) input is High or high-impedance, as shown in Figure 2, the behavior of the device becomes unpredictable.

**Figure 2. Hazardous Sequence**



### MAIN SOURCES OF ERROR: POWER-UP AND MCU RECOVERY START-UP

There are two main causes of users using these devices outside their specifications:

- Uncontrolled inputs during Power-Up and Power-Down
- Uncontrolled inputs during Microcontroller Recovery Start-up Time

#### Uncontrolled Inputs During Power-Up and Power-Down

During power-up, all three input lines (C, D and S) start in their uncharged state, and might well be undriven. There is no control of Low-to-High transitions being picked up from noise. Also, there is no guarantee that if drive is later applied simultaneously to the three signals, that the Chip Select (S) line will cross the Low-to-High threshold before either of the other two.

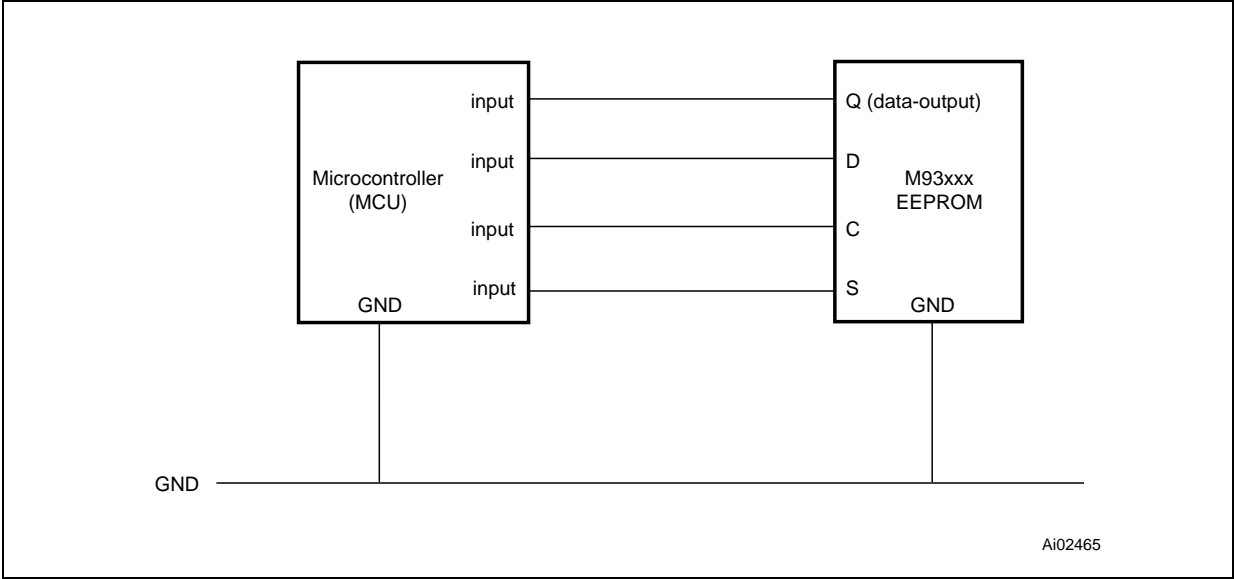
During power-down, the problem of noise pick-up on undriven lines returns as the main source of hazard. Most microcontrollers will attempt to avoid these problems by going into a Microcontroller Recovery Start-up Mode when the  $V_{CC}$  line is outside its specified range. However, as discussed next, this does not completely resolve the problems.

#### Uncontrolled Inputs During Microcontroller Recovery Start-up Time

During the Microcontroller Recovery Start-up Time, which is typically several milliseconds in duration, some microcontrollers configure all I/O lines in their input mode, as shown in Figure 3. That is, they are all set to their high-impedance state. Under these conditions, with inputs C, D and S all undriven, each line behaves like a small antenna, and can pick up electromagnetic noise radiation. It is not impossible for there to be a rising edge on the Chip Select (S) input while C or D is floating High.

Alternatively, some microcontrollers configure all I/O lines as outputs during the Microcontroller Recovery Start-up Time, and drive the lines High. As soon as Chip Select (S) crosses the Low-to-High threshold, the EEPROM is enabled, and will decode whatever enters its D and C inputs. If these are acting outside the specification, the behavior of the EEPROM becomes unpredictable.

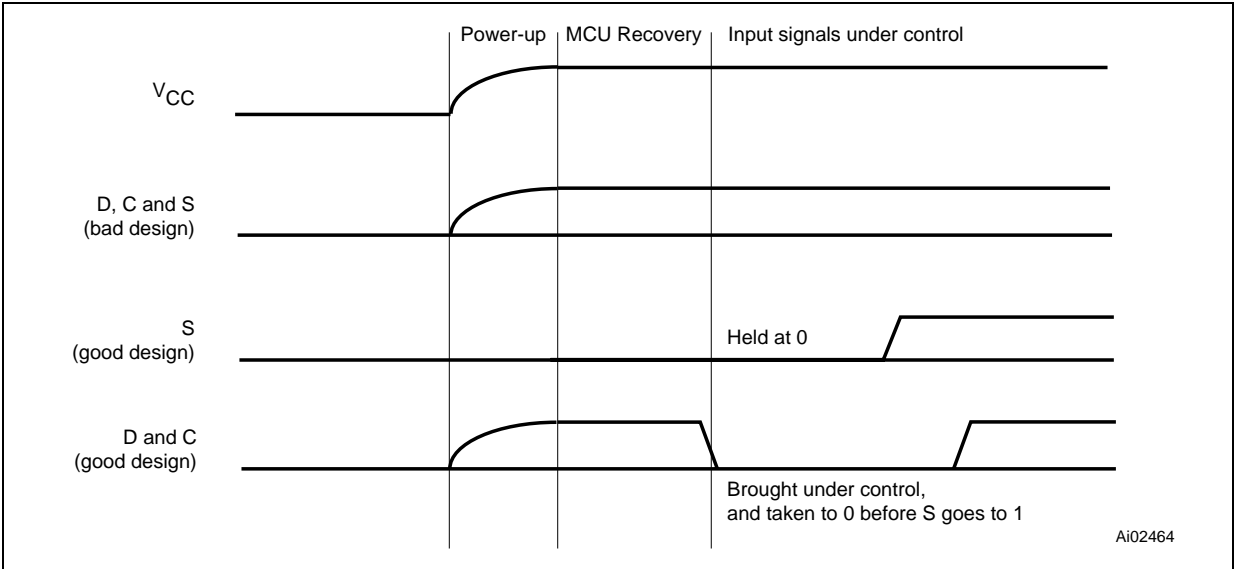
Figure 3. All Signals Being Treated as Inputs



**CORRECT POWER-UP AND MICROCONTROLLER RECOVERY**

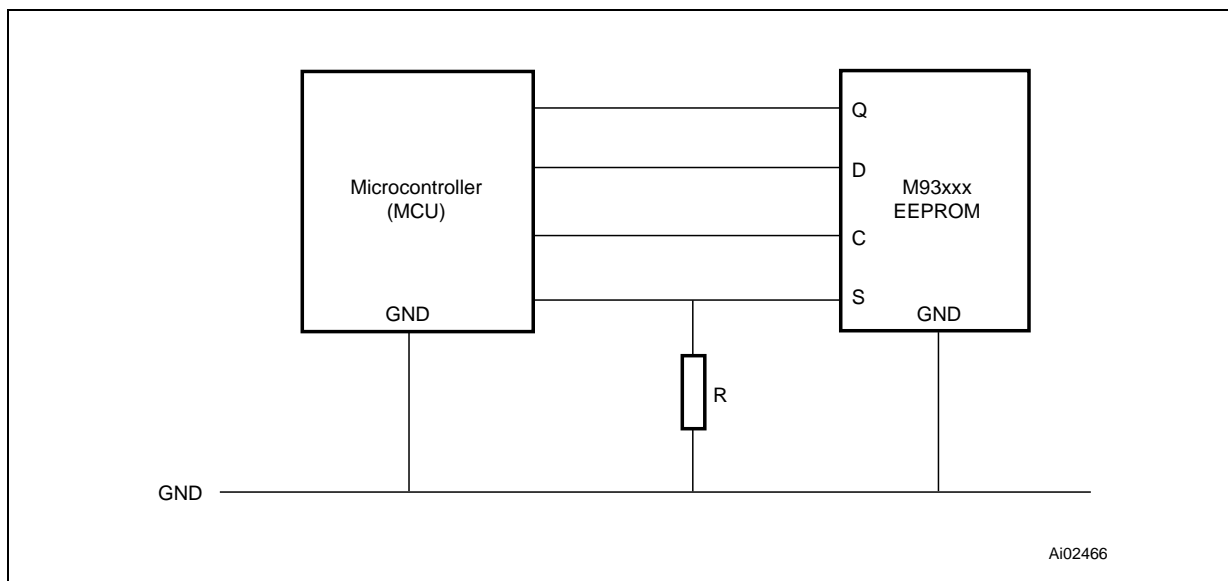
The critical line is the Chip Select (S) input. For safety, it can be tied Low by a pull-down resistor, so that it does not float High when the input is undriven.

Figure 4. Signal Transients of Bad and Good Design



While the Chip Select (S) input is held Low, the chip is not selected, and it does not matter what signals occur on the other lines (provided that they remain within the specified safe range). It is only necessary, therefore, for the Chip Select (S) input to be tied Low by a pull-down resistor, as shown in Figure 5, so that it never goes High when it is undriven, as confirmed in Figure 4.

Figure 5. Safe Design with a Pull-Down Resistor on the Chip-Select (S) Line

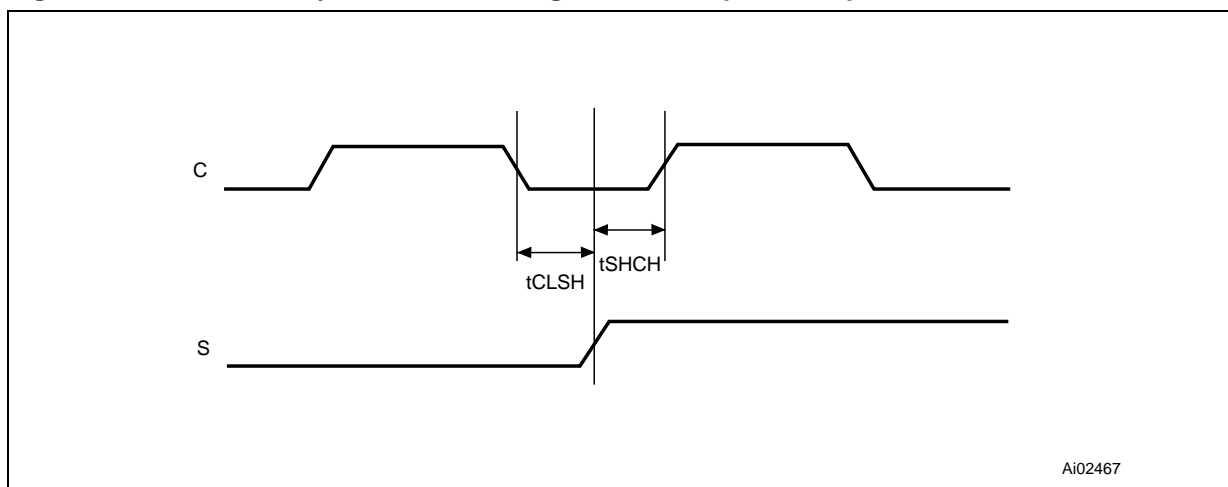


The value for the pull-down resistor can be calculated from the minimum logic 1 input voltage,  $V_{IH}$ , that is recognized by the M93xxx, and the maximum source current,  $I_{OH}$ , that can be sustained by the microcontroller. The resistance must be greater than the quotient of these two values:  $R > V_{IH(M93xxx)}/I_{OH(MCU)}$ .

**INPUT SIGNALS UNDER CONTROL**

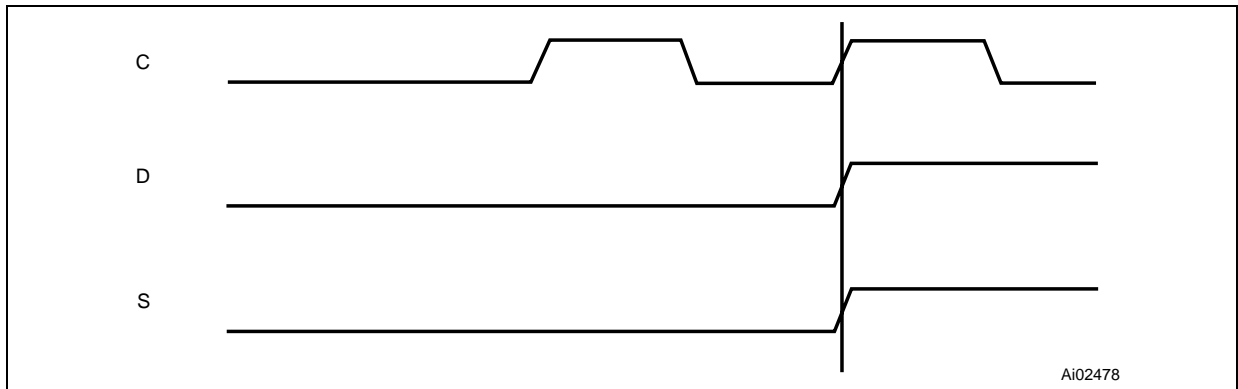
Once the application power-up and power-down are properly controlled, it is next important to check that the specification is adhered to for all normal uses of the chip-select signal (as indicated in Figure 4). The data sheet specifies that there is a minimum chip-select set-up time,  $t_{CLSH}$ , and a minimum chip-select hold time,  $t_{SHCH}$  (as shown in Table 6 of the M93C06/46/56/66/76/86 data sheet). That is, the clock must be held Low for at least  $t_{CLSH}$  before Chip Select (S) is allowed to go from Low to High, and to continue to be held Low for at least  $t_{SHCH}$  after the rising edge of Chip Select (S) (as shown in Figure 6, which is an extract from Figure 4 of the M93C06/46/56/66/76/86 data sheet).

Figure 6. Extract from: Synchronous Timing, Start and Op-Code Input”



**INCORRECT CONTROL OF THE INPUT SIGNALS**

Figure 7 shows an example of incorrect use of the input signals. The designer has assumed, incorrectly, that it is safe for all three signals (C, D and S) to rise at the same time. However, the interpretation of this event is undefined, and will be decoded randomly as being a {Select} event, or a {Select, D=0} event, or a {Select, D=1} event. The last of these being interpreted, therefore, as a start bit. It is for this reason that this sort of sequence is forbidden, and recognized as being a use of the device outside of its specification.

**Figure 7. Incorrect Sequence**

## AN1119 - APPLICATION NOTE

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If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

*apps.eeprom@st.com* (for application support)  
*ask.memory@st.com* (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.

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