FETs As Voltage-Controlled Resistors

Introduction: The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

For a junction field-effect transistor (JFET) under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor. Maximum drain-source current, I_{DSS}, and minimum resistance $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts (V_{GS} = 0). If the gate voltage is increased (negatively for n-channel JFETs and positively for p-channel), the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage- controlled resistor.

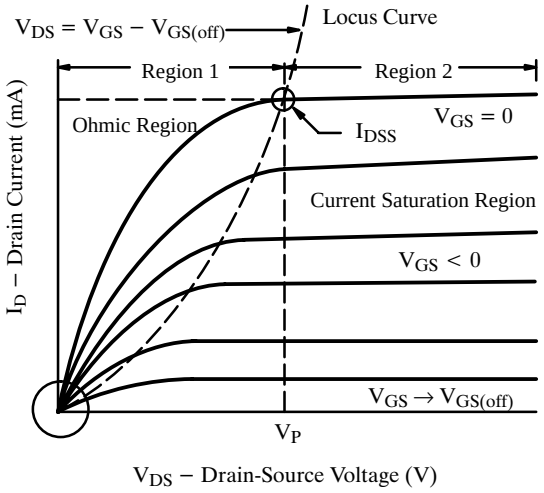

Figure 1. Typical N-Channel JFET Operating Characteristics

Figure 1 details typical operating characteristics of an n-channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain-to-source is different for each value of gate-source bias voltage. The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

Resistance Properties of FETs

The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{DS}, is essentially the same as that of dc resistance, r_{DS}, and is a function of V_{GS}.

Figure 2 shows an extension of the operating characteristics into the third quadrant for a typical n-channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $I_D/V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at V_{GS} = 0 and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.

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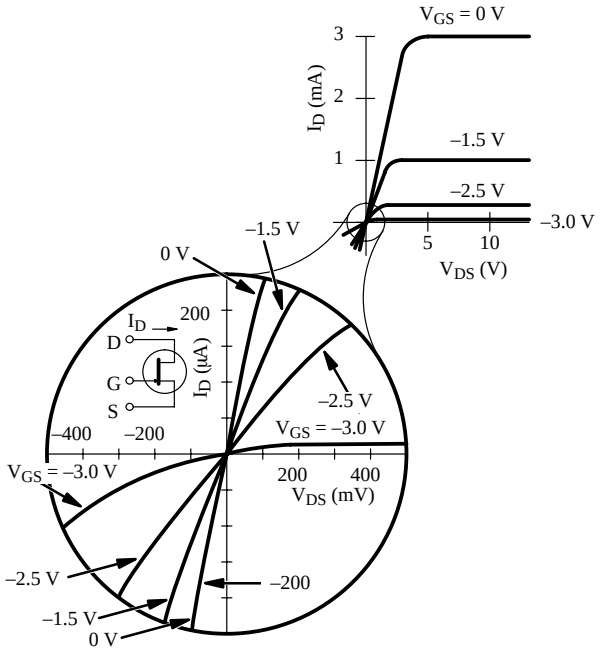


Figure 2. N-Channel JFET Output Characteristics Enlarged Around V_{DS} = 0 V

The graph in Figure 3 is useful in estimating r_{DS} values at any given value of V_{GS}. The resistance is normalized to its specific value at V_{GS} = 0 V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

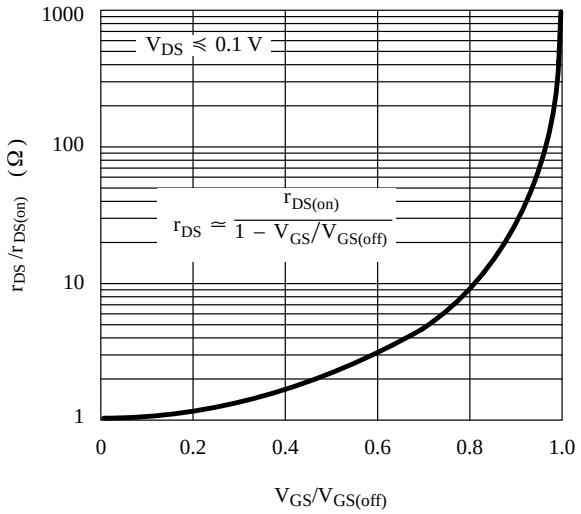


Figure 3. Normalized r_{DS} Data

Siliconix offers a family of n-channel FETs specifically intended for use as voltage-controlled resistors. These devices have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω, where VCR2N = 20 – 60 Ω, VCR4N = 200 – 600 Ω, VCR7N = 4 k – 8 kΩ.

Applications for VCRs

A simple application of a FET VCR is shown in Figure 4, the circuit for a voltage divider attenuator.

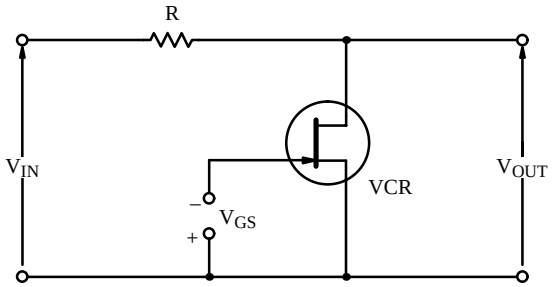


Figure 4. Simple Attenuator Circuit

The output voltage is:

$$V_{OUT} = \frac{V_{IN} r_{DS}}{R + r_{DS}} \quad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is:

$$V_{OUT(min)} = \frac{V_{IN} r_{DS(on)}}{R + r_{DS(on)}} \quad (2)$$

Signal Distortion: Causes

Figure 2 shows that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 5 shows how the current has an opposite effect in the third quadrant, increasing negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

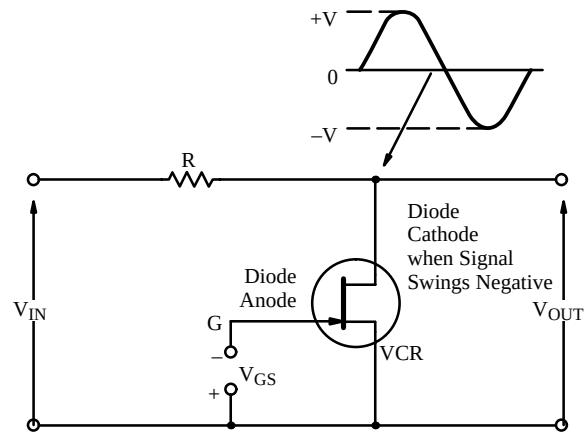


Figure 5. Simple Attenuator Circuit

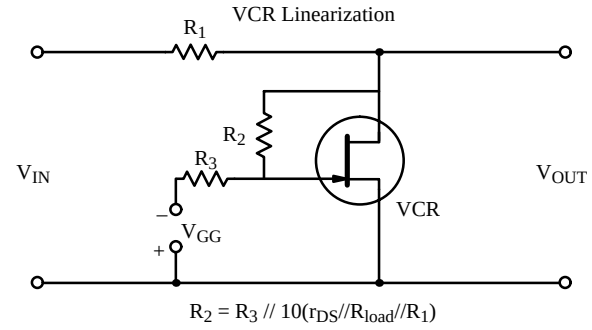


Figure 6.

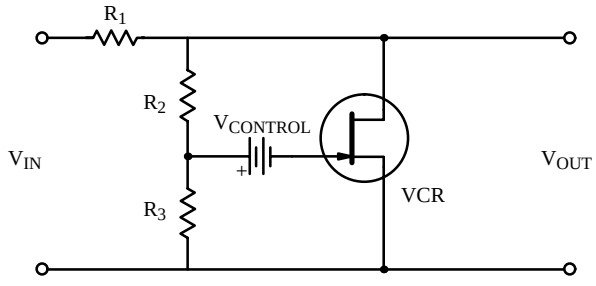


Figure 7.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 6.

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the dc gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 6 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10\,[R_1 \| r_{DS}\,(max) \| R_L] \qquad (3)$$

Typically, 470-kΩ resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)} \| R_L$ to $[(r_{DS(on)} \| R_L) + R_1]$ give the desired output voltage, or:

$$V_O = V_I \frac{r_{DS(on)} \| R_L}{(r_{DS(on)} \| R_L) + R_1} \qquad (4)$$

The feedback technique used in Figure 6 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 5 for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 7 and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Experimental Results

Figures 8 and 9 show low voltage output characteristic curves for a typical Siliconix n-channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 8 shows a two-volt peak-to-peak signal on the V_{GS} = 0 V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

The forward-biased gate-drain PN junction may be seen at approximately –0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion at 2 V peak-to-peak.

In Figure 9, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

In Figures 8 and 9, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS}. No feedback network is employed in Figure 8, and measured distortion is greater than 8%. In Figure 9, the feedback resistors have been added and distortion has been reduced to less than 0.5%.

Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants.

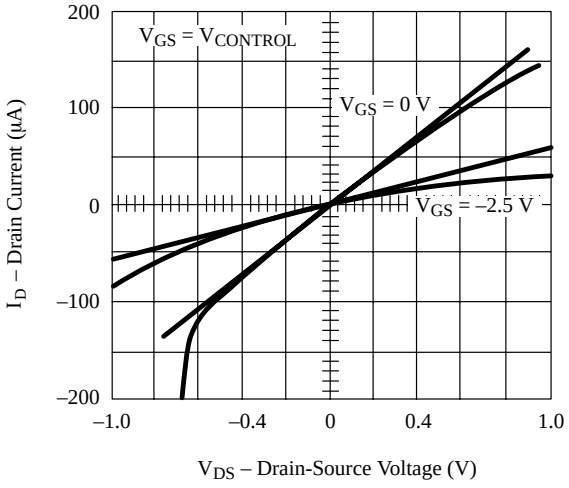


Figure 8. VCR7N Without Feedback

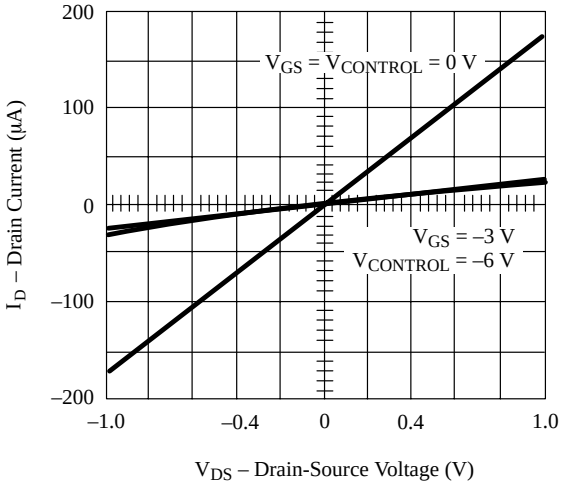


Figure 9. VCR7N With Feedback.

Table 1: Distortion vs. Temperature

Temperature (°C)	Without Feedback		With Feedback	
	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\ r_{DS(on)}$
+125	>13%	>6%	<0.5%	<0.5%
+25	>10%	>5%	<0.5%	<0.5%
–55	3.9%	3.2%	<0.5%	<0.5%

Distortion resulting from changes in temperature is also minimized by the feedback resistor technique. On-resistance will change with temperature in an inverse manner to the behavior of FET drain current. Table 1 presents the result of VCR laboratory performance tests of distortion versus temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

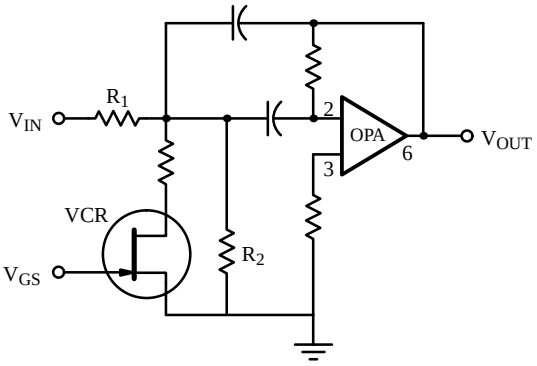
Summary

This application note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no dc bias voltage in the signal loop, an ideal characteristic for many applications.

Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

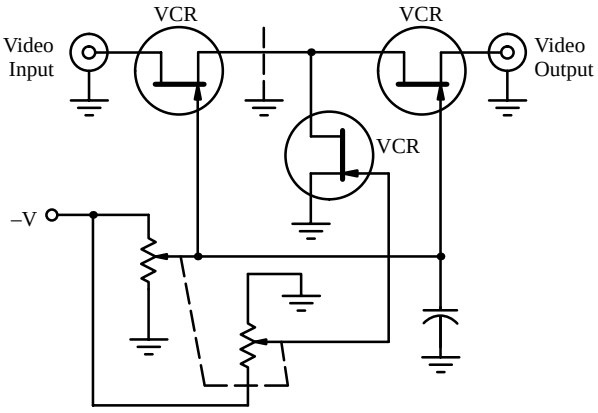
It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ compatible with the desired r_{DS} value if large signal levels are to be encountered.

A number of other FET VCR applications are shown in Figures 10 through 15.



Lowest frequency at JFET $V_{GS(off)}$ and tuned by R_2.
Upper frequency is controlled by R_1.

Figure 10. Voltage-Tuned Filter Octave Range



The “T” attenuator provides for optimum dynamic linear range attenuation.

Figure 11. Voltage Controlled Variable Gain Amplifier

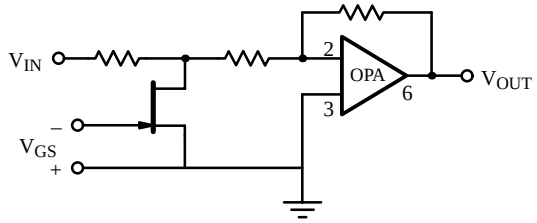


Figure 12. Electronic Gain Control

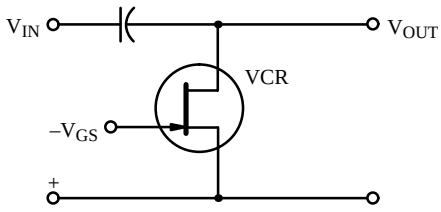


Figure 13. VCR Phase Advance Circuit

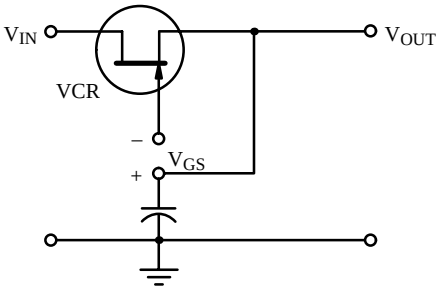


Figure 14. VCR Phase Retard Circuit

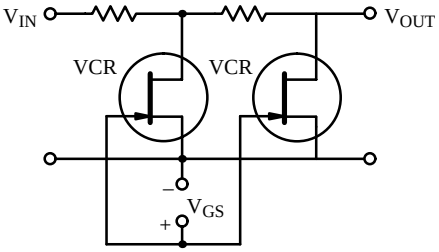


Figure 15. Cascaded VCR Attenuator

Table 2: Popular JFETs for VCR Applications

Range $r_{DS(on)}$ (Ω)	M/C – Hermetic	Plastic Thru Hole*	Suface Mount*
20 – 60	VCR2N	J111	SST111
100 – 600	VCR4N	2N5486	SST5486
4 k – 8 k	VCR7N	PN4119A	SST4119

*Approximate equivalents to VCR_N specifications.

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