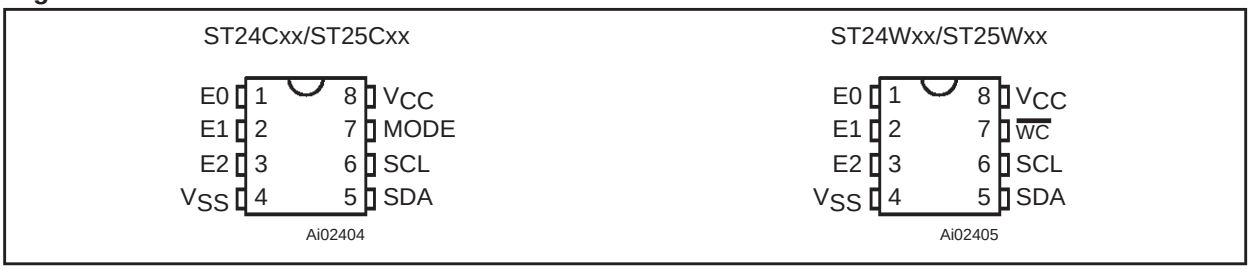
AN1006
APPLICATION NOTE

The Write Control Feature on I²C EEPROM

The ST24xxx/ST25xxx EEPROM devices are fully compatible with the I²C ™ standard. Some, though, have the extra feature of offering a hardware write control (WC) line. The purpose of this document is to highlight the advantages of this facility.

On the ST24Cxx/ST25Cxx I²C EEPROM devices, pin 7 is used to select between the multibyte and page-write modes. On the ST24Wxx/ST25Wxx I²C EEPROM devices, this is replaced by the WC line, as shown in Figure 1.

Figure 1. ST24xxx/ST25xxx Pin Connections



WC is an active-low signal. When it is held low, erase and write commands are executed; when it is held high, erase and write operations are inhibited (and any erase or write commands issued by the master device are ignored).

This feature has been designed to be used by the application hardware whenever there is any question as to the validity of the data. The device can thereby reject the data, and wait for the master device to send it again. In particular, the ST24W/25Wxx series, in combination with suitable hardware design, can offer better data protection against the following conditions:

- during power-up and power-down sequences, when voltage levels are wandering out of specification
- whenever high levels of electrical noise are detected, and the validity of the received data becomes questionable
- whenever the I²C bus is shared by devices using other protocols, and unexpected conflicts arise
- under other detectable fault conditions, specific to the application.

For specific examples of the use of this feature, please see Application Notes *AN404* and *AN627*.

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.

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