AN1005
APPLICATION NOTE

Extending the I^2C Bus — XI^2C

The I^2C (Inter Integrated-Circuit) standard was designed for applications that need to be highly efficient of board space. It has been adopted almost universally by consumer equipment makers for internal communication between the digital ICs in their products. It is also gaining popularity in other types of equipment.

The standard uses a two wire bus: respectively the serial data line (SDA) and the serial clock line (SCL). Each line is configured for use in a wired-or arrangement, with one external pull-up resistor each. Data on SDA is synchronous with respect to SCL.

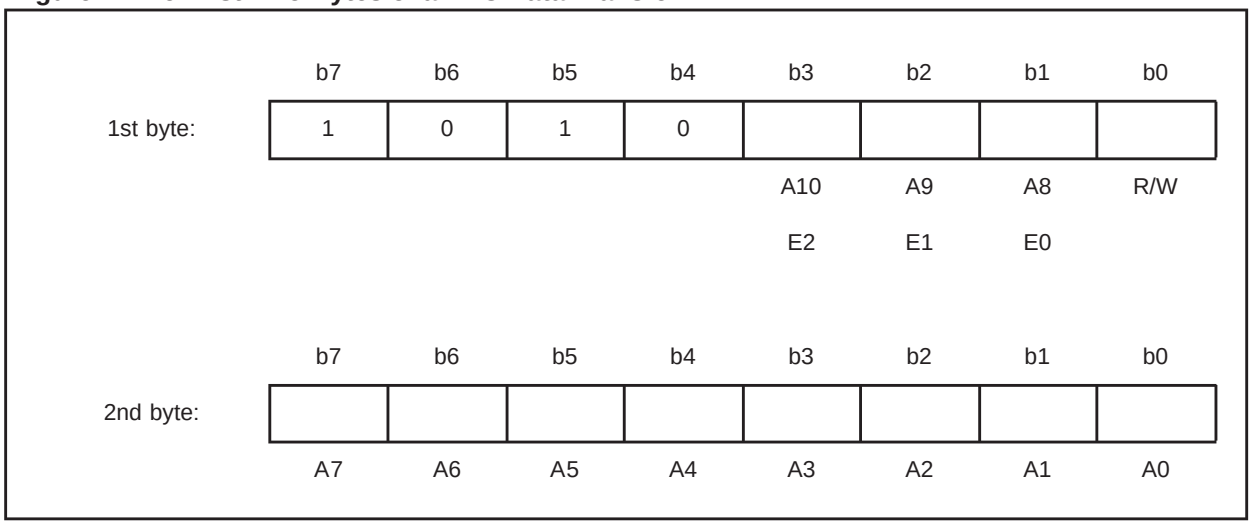
Specific combinations of data and clock signals are used to mark the Start or Stop of a data transfer. Devices on the bus can act as transmitters or receivers of data. Their action can also be described as being initiators (masters) or responders (slaves) of the data transfer.

Each type of circuit connected to the bus has a unique "device select code". For example, all memory devices have the four bit code "1010" and will only respond if they detect this code.

I^2C BUS

Figure 1 shows how the first byte of a data transfer contains the EEPROM select code "1010", the chip enable E2-E0 or address bits A10-A8, and the read/write operation bit. The second byte contains the address bits A7 to A0.

Figure 1. The First Two Bytes of an I^2C Data Transfer



Addresses on the I^2C bus, therefore, are limited to 11 bits, and hence to an address space of 2 Kbyte. In the case of a 2 Kbyte memory chip, the address is decoded directly from the A10 to A0 settings. In the case of a 256 byte memory chip, only address bits A7 to A0 are used. This leaves the bits in the first byte available for use as chip select bits, E2 to E0. The 256 byte memory chip will only respond to the address in bits A7 to A0 if the pattern in the E2 to E0 bits is the same as that which has been hard-wired on the E2

to E0 pins of the chip itself. In this way, it is possible to select between as many as eight 256 byte memory chips, and hence an address space still of the maximum 2 Kbyte capacity.

Between these two extremes, it is also possible to implement a memory capacity of 2 Kbyte using two 1 Kbyte memory chips, or four 512 byte memory chips. The four possible configuration, therefore, are as follows:

- 1 chip containing 2 Kbyte, 16 Kb, of memory (addresses A10-A8 in the first byte, A7-A0 in the second)
- 2 chips containing 1 Kbyte (one chip enable, E, to select between them, and address bits A9-A8 in the first byte, A7-A0 in the second)
- 4 chips containing 512 bytes (two chip enables, E2-E1, to select between them, and address bit A8 in the first byte, A7-A0 in the second)
- 8 chips containing 256 bytes (three chip enables, E2-E0, in the first byte to select between them, and address bits A7-A0 in the second)

THE EXTENDED I^2C BUS

The I^2C bus suffers from two limitations built into its specification:

- It allows a maximum of 11 bit addressing, giving a memory limit of 2 Kbyte (16 Kb).
- It offers a maximum transfer rate of 100 Kb/second.

As equipment was needing ever larger amounts of EEPROM for parameter storage, it became apparent that a new standard was required. In January 1992, a new specification was published for the I^2C bus which increased the speed up to 400 Kb/second, and added an option for extending the slave-select (chip enable) bits to 10 bits (E0 to E9), thus allowing up to 1024 slave devices to be connected to the bus.

Upon receiving the special four bit code “1111”, in place of the usual “1010”, the hardware would switch from the default I^2C mode, and would expect the next eleven bits (3 bits in the current byte, and 8 in the next) to contain a leading 0 followed by E9 to E0.

However, SGS-THOMSON was not happy with this proposal as it is not backward compatible with the previous standard. ***This format is not supported by ST’s EEPROM devices***.

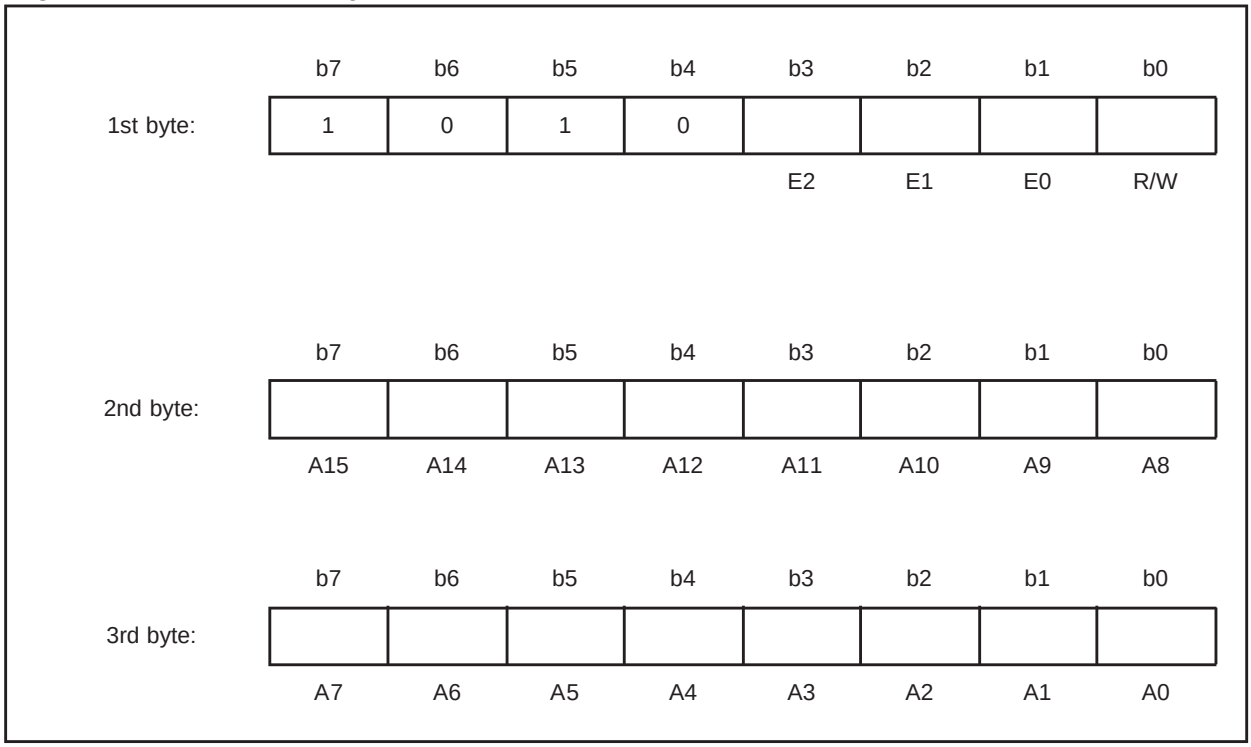
Instead, SGS-THOMSON took the initiative to request a further change to the I^2C bus. The aim was to extend the memory addressing itself, rather than just the number of chip enable lines, by using two address bytes instead of one. This would allow up to three bits for chip enable selection E2-E0 (or addresses A18-A16) and a full 16 bit address A15 to A0. Memory addresses could thereby be extended from eight blocks of 256 bytes to eight blocks of 64 Kbytes (a total capacity of 512 Kbyte, 4 Mb). This request was granted, and gave rise to the Extend I^2C format, otherwise known as “XI^2C”. The format is depicted in Figure 2.

A further feature of this format is that, if bits b3-b1 of the first byte are used for chip enable E2-E0, it is possible to implement a system that addresses a mixture of I^2C and XI^2C devices.

400 K BITS PER SECOND

The main implications of changing to faster clocking rates are felt not only by the bus interface, in which the timing schedule needs adaptation, but also by the spike suppression circuitry in the memory chip. Each input must be able to reject noise pulses of up to 50 ns in width, and each output must be able to sink up to 6 mA at VOL = 0.6 V, and to have a output fall time of no more than 250 ns.

Figure 2. The First Three Bytes of an XI^{2}C Data Transfer



NEW PRODUCTS

The first devices to use the XI^{2}C standard are listed in Table 1. The total theoretical capacity is 4 Mb, so future ST product growth is assured for many years to come.

Table 1. Members of the M24xxx Eagle Range

Product	Description
M24C32	32 Kb XI^{2}C EEPROM, organised as 4 Kbyte
M24C64	64 Kb XI^{2}C EEPROM, organised as 8 Kbyte
M24128	128 Kb XI^{2}C EEPROM, organised as 16 Kbyte
M24256	256 Kb XI^{2}C EEPROM, organised as 32 Kbyte
M24512	512 Kb XI^{2}C EEPROM, organised as 64 Kbyte

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.

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