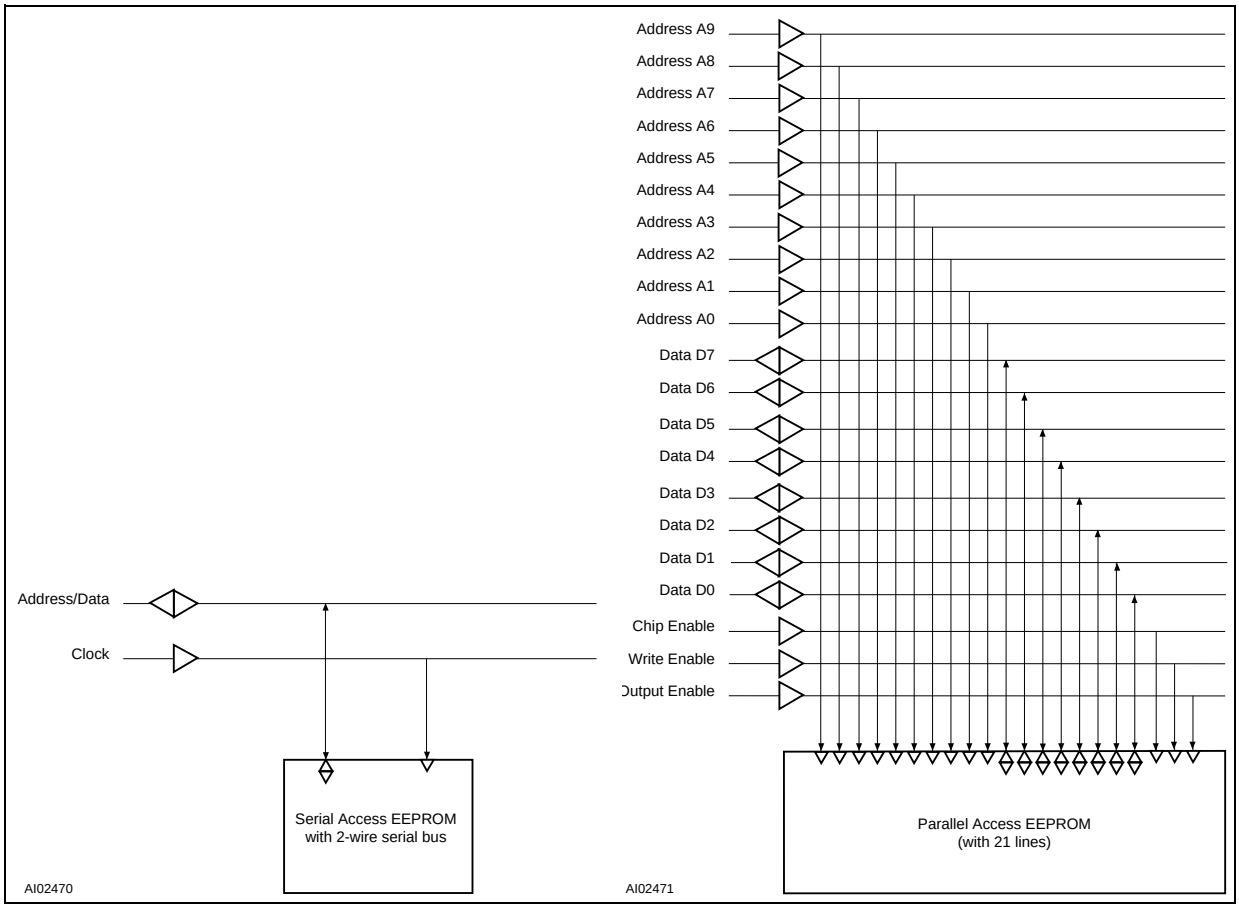
AN1001
APPLICATION NOTE

Choice of Serial EEPROMs Requires Understanding of Bus Differences

Serial access memory devices offer many advantages over their parallel access counterparts. The list on the next page assumes the use of 10-bit addressing, as depicted in Figure 1. The differential becomes even greater as the address space is increased.

Figure 1. Serial Access versus Parallel Access



The advantages of serial access to the EEPROM, or other slave devices, over parallel access, can be listed as follows:

- Fewer interconnect lines and PCB tracks:
  - A factor of 1/18th compared to the PCB area that is taken up by the ten address and eight data lines
- Fewer line buffers:
  - A factor of 1/18th comparing the PCB area that is taken up by address and data buffers
  - A factor of between 1/8th and 1/18th of the cost of address and data buffers (remembering that the address buffers of the parallel memory can be simple unidirectional devices)
- Fewer control lines:
  - A factor of 1/3rd, say, of the PCB area taken up by the control line pins of the chip
- Fewer interconnect pins:
  - A factor of 1/5th, say, of the PCB area taken up by the pins of the chip, and hence its footprint
- Fewer on-chip buffers: A factor of between 1/8th and 1/18th of the silicon area taken up by pads and I/O buffers for the address and data lines:
  - Therefore, serial access memory devices have more silicon area available for increasing the memory capacity, appearing on the market earlier than parallel access memory devices using comparable technology.

The greatest disadvantage of serial access memory, of course, is access time.

- Lower data rate, due to the serial multiplexing of the single data line:
  - A factor of between 1/8th and 1/10th (depending on the number of stop and acknowledge bits) of the data transfer rate, during the data transfer cycles.
  - An even worse factor for the address transfer rate, partly because of the 10-bit address width, and partly because of the prefix instruction required to put the memory in its address-mode.

For many applications, though, the access times of parallel access memory devices represent “overkill” – being unnecessarily fast for the requirements of the application. EEPROM is not used like RAM, and is used, in many applications, mainly for system parameter tables. These do not require very high speed access to the data for reading or writing, so serial bus speeds of 100 kHz to 1 MHz are more than adequate.

COMPARISON OF THE FOUR MAJOR SERIAL ACCESS STANDARDS

Having decided that serial access EEPROM is an appropriate choice for the application, the next design problem faced by the engineer is one of choosing the most appropriate serial bus standard. There are four main ones to choose from, each one available in STMicroelectronics memory products, and each offering differing capabilities in terms of bus size, bus protocol, noise immunity and access time.

- I^2C bus
- XI^2C bus
- SPI bus
- MICROWIRE bus

This document discusses these four standards, and the design trade-offs with which the application designer is faced when choosing between them.

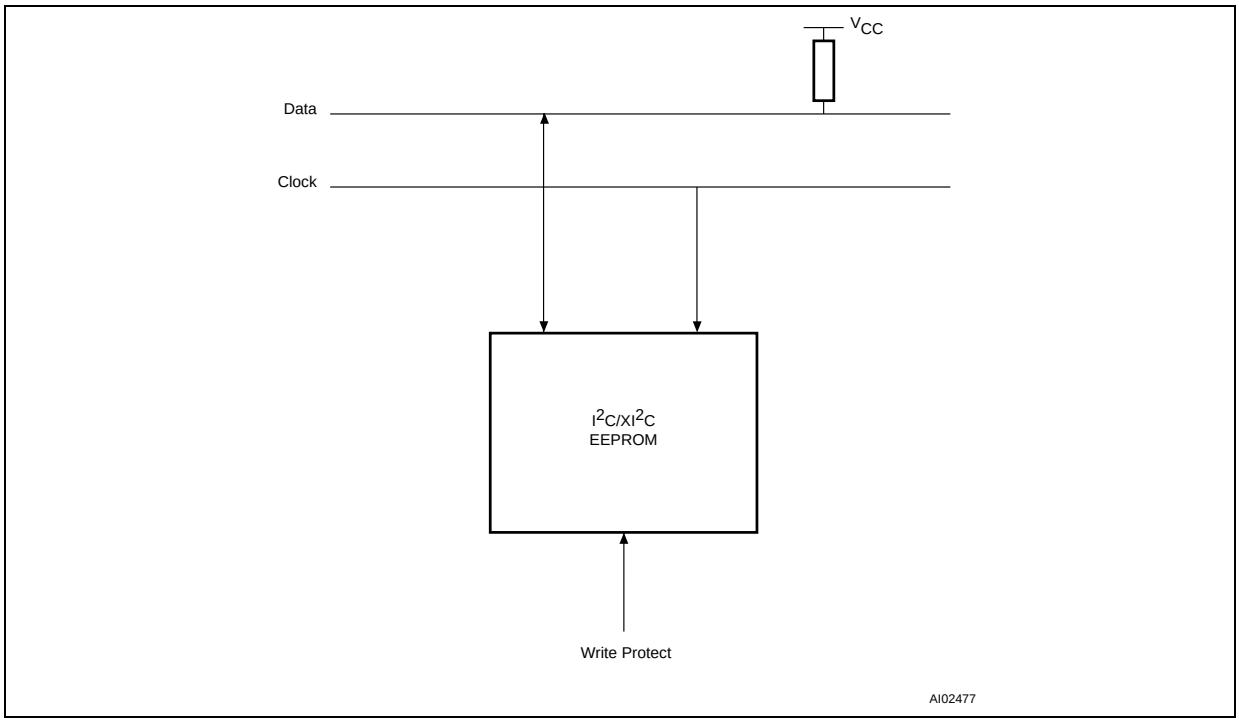
I²C AND XI²C BUSES

Perhaps the most popular of the four standards is the I²C bus, designed by Philips. It was initially aimed at consumer applications market. A wide spectrum of devices is available today, not only memory devices.

The I²C standard specifies a two-wire bus, as shown in Figure 2. Its sophisticated protocol allows systems to support many devices on the bus, with the capability even of allowing multiple masters, as well as multiple slaves.

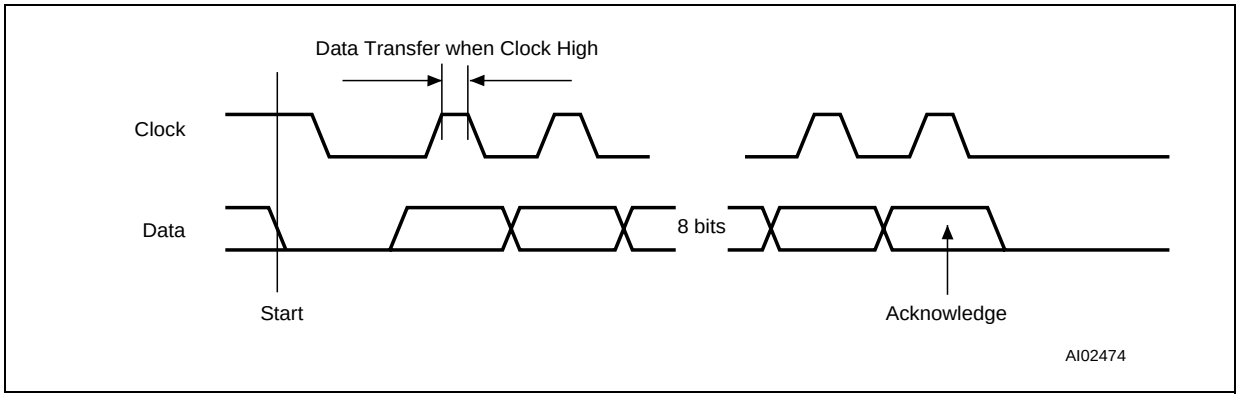
The original I²C standard only allowed an address space of up to 16 Kbit of memory, but the subsequent XI²C (extended I²C) bus standard, has extended this to 4 Mbit. The bus speed is limited to 100 kHz for I²C and 400 kHz for XI²C. The noise immunity in both cases is good.

Figure 2. I²C and XI²C Bus Block Diagram



Bus transfers start when the clock line is high on the falling edge of the data, as shown in Figure 3. Transfers are always 8 bits, followed by a ninth – an acknowledge bit from the bus receiver. Data is transferred when the clock signal is high. The data line is wired “or” with an external pull-up resistor to V_{CC}.

Figure 3. I²C and XI²C Bus Timing

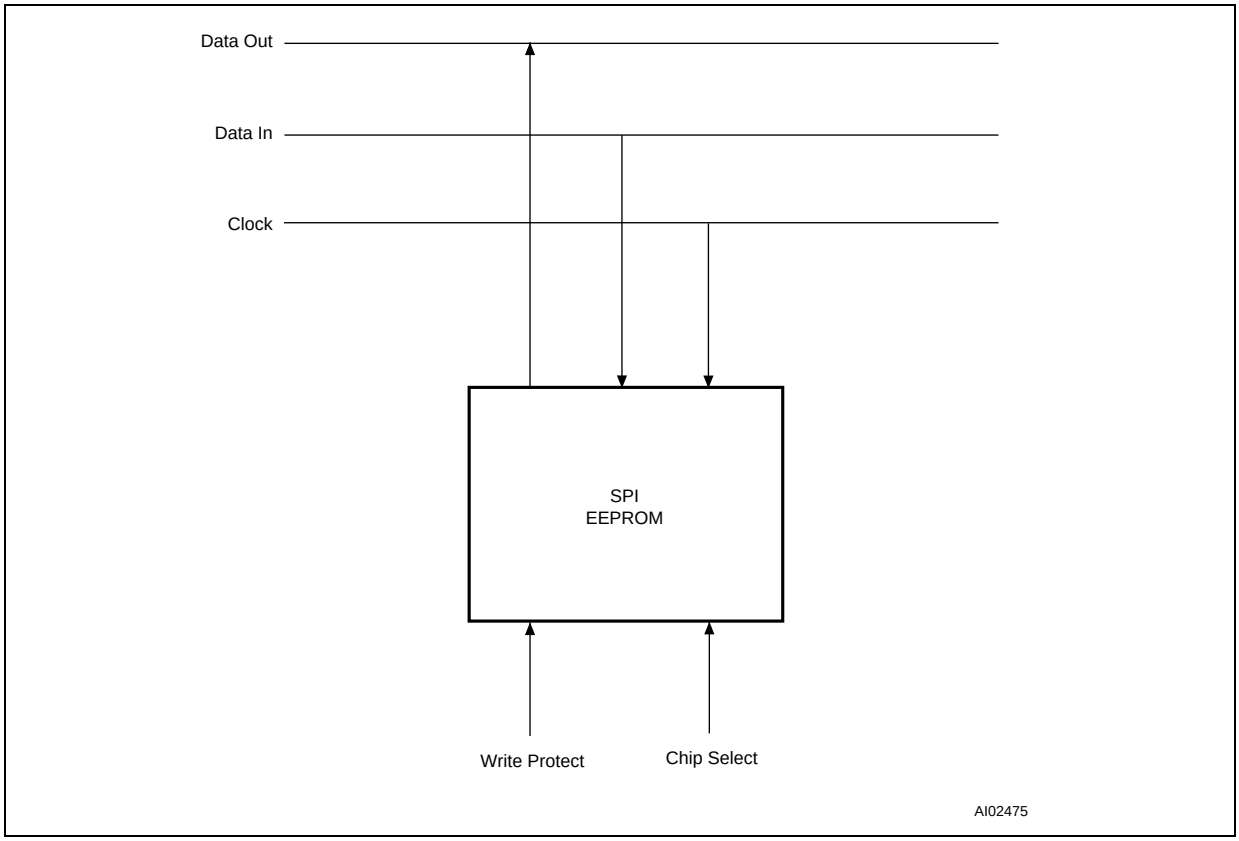


SPI BUS

The SPI standard was first proposed by Motorola, for its microcomputers, but is now offered by ST and other companies, integrated as a peripheral into their MCUs, and is rapidly gaining support.

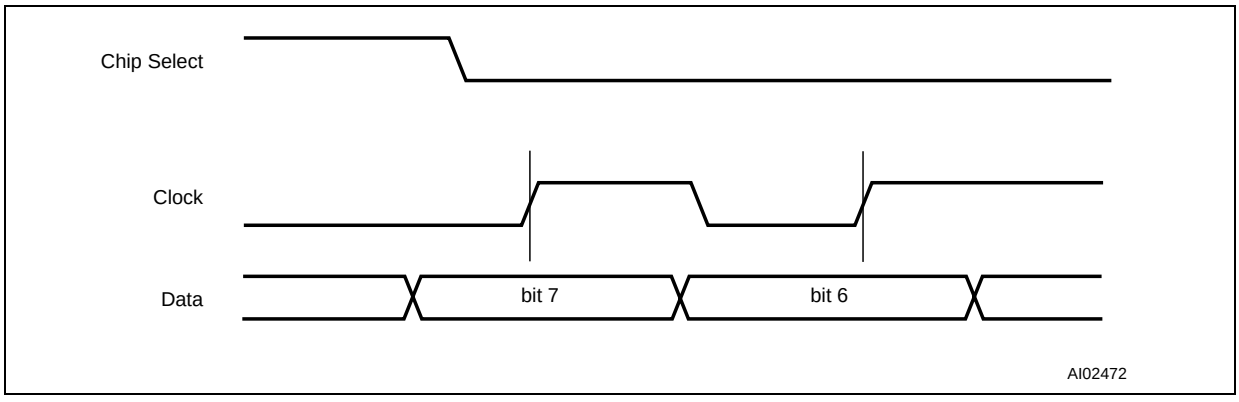
Memories using this bus have four signal wires (data input, data output, clock and chip select), as shown in Figure 4. Each device on the bus must have its own, separate, chip select line. This means there is no limit to the number of slaves on one SPI bus, but each increase demands another MCU I/O line. The maximum bus speed is 5 MHz, and the noise immunity is very good.

Figure 4. SPI Bus Block Diagram



Bus transfers start after the chip select goes low, as shown in Figure 5. Transfers are always 8 bit, and each bit is detected on the rising edge of the clock. A write protect input is provided.

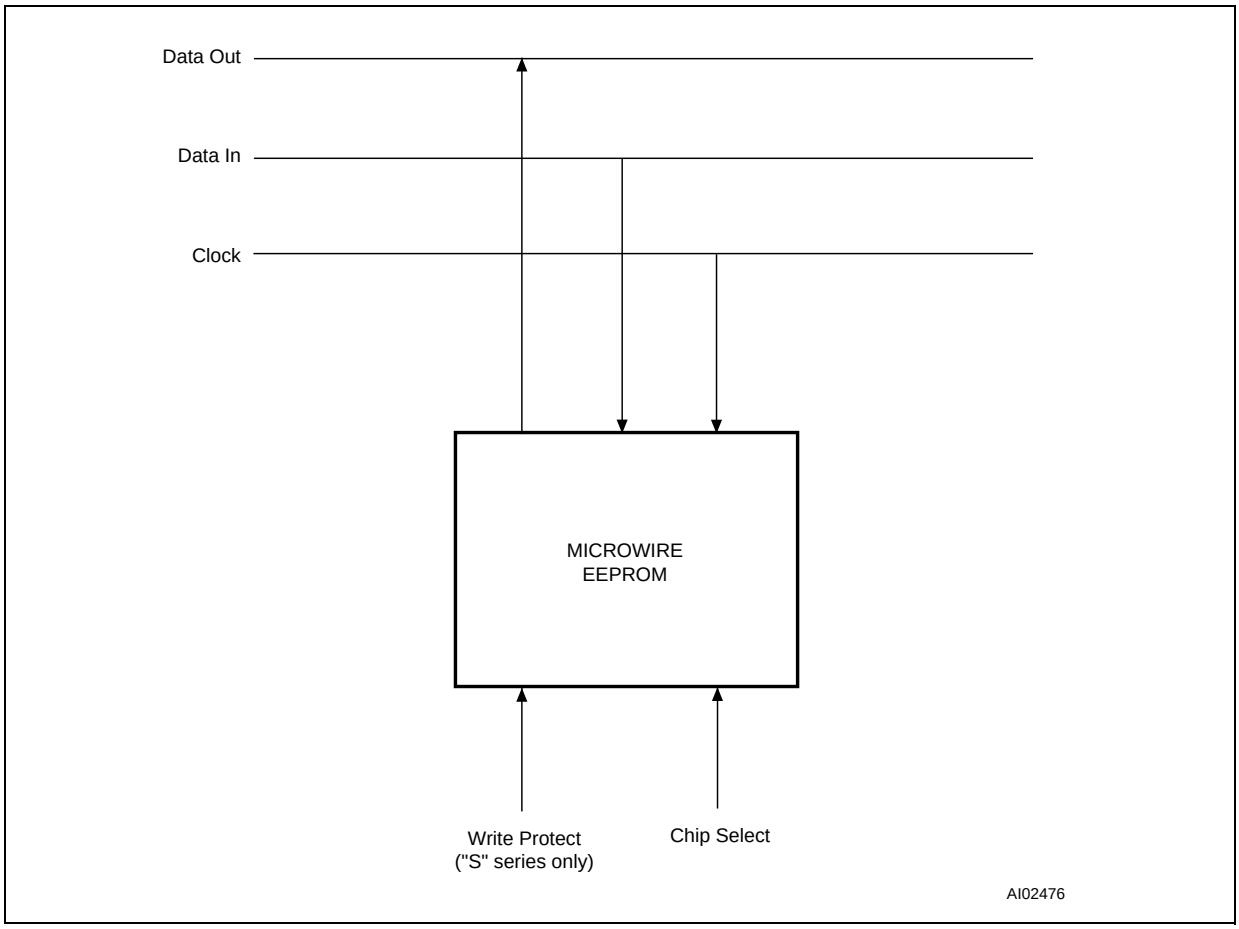
Figure 5. SPI Bus Timing



MICROWIRE™

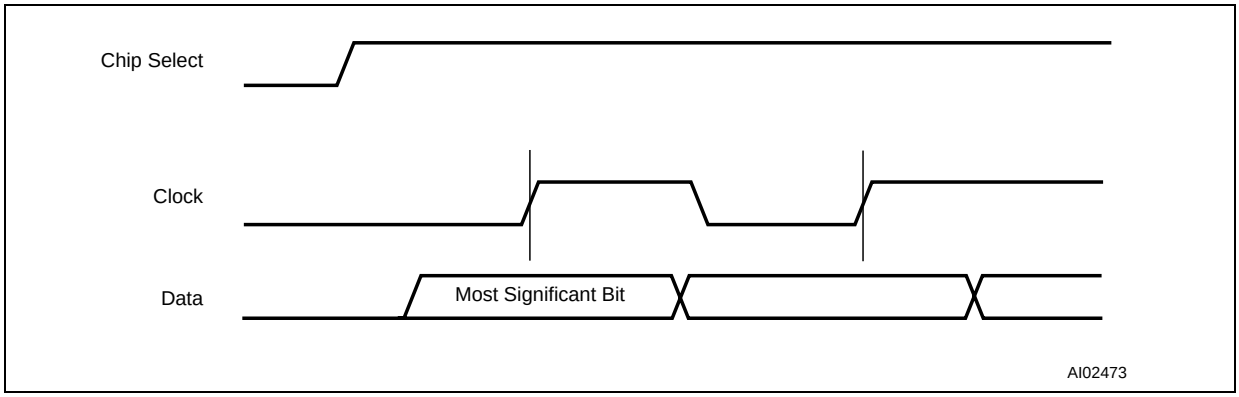
The MICROWIRE bus is based on the system that was developed for the MCU products of National Semiconductor. However, market support for this bus no longer appears to be growing. Like the SPI bus, it uses four wires and requires a chip select for each device on the bus, as shown in Figure 6. The maximum bus speed is quite high, at 1 MHz.

Figure 6. MICROWIRE Bus Block Diagram



Bus transfers start after chip select goes high. Each data bit is detected on the rising edge of the clock, as shown in Figure 7. A Write Enable input is provided on the “S” series devices.

Figure 7. MICROWIRE Bus Timing



THE BUS CHOICES

The choice of appropriate bus standard revolves round the following four major concerns:

- The number of interface pins on the MCU:
  - Here the I^2C or XI^2C buses are clear winners, since they need only two lines.
- The system communication protocol:
  - For simple read or writes to the memory by an MCU, any of the bus types offers the same potential, but in a system where many different types of circuit are connected to the bus, or where a complex system of multi-masters/multi-slaves is used, only the I^2C or XI^2C can provide the necessary resources.
- Speed:
  - This is not a primary concern in many EEPROM applications, but where it is important, the SPI and MICROWIRE buses are favoured.
- Noise immunity, data security and protection from data corruption:
  - These concerns are not completely determined by the choice of bus standard. Large differences exist between different manufacturers, and even between the different products from one manufacturer. However, this issue is discussed further on the next page.

DATA TRANSFER SPEED AND WRITE COMPLETION POLLING

The read data transfer speed of the serial buses varies from:

- one byte every 1.6 µs for the SPI with a 5 MHz clock
- one byte every 8 µs for the MICROWIRE with a 1 MHz clock
- one byte every 22.5 µs for the XI^2C with a 400 kHz clock.
- one byte every 90 µs for the I^2C with a 100 kHz clock.

All four standards support a burst mode, or sequential read mode, in which a contiguous block of any size can be read, one byte after another. I^2C and XI^2C types also support page write operations, allowing between 8 and 32 consecutive bytes to be written in 5 to 10 ms. The SPI standard is similar, but only the newer “CS” series of MICROWIRE devices offer a page write of 4 words (4x16 bits).

The ST specification, for all families of serial EEPROM, states a maximum write time of 10 ms. However, the actual value, which is managed automatically and internally, is typically much faster than this. To take advantage of the faster typical write time in systems, designers use memory polling to detect when the write sequence has finished.

The I^2C and XI^2C bus devices offer a very efficient polling system by detecting a memory acknowledge signal (a single bit that is sent by the EEPROM, or other bus receiver, in the ninth bit time after the memory is addressed or data is exchanged). Thus to poll the I^2C devices, it is sufficient to send a single one byte address to the memory and to check the acknowledge bit that is sent response.

For the SPI bus, the polling technique requires that an internal status register be read to check a write-in-progress bit. This requires a read sequence of only two bytes’ length.

The MICROWIRE devices can be polled by simply placing the chip select line high. A data output low indicates that writing is still in progress.

NOISE IMMUNITY AND DATA SECURITY

Some defences, against noise and corrupt write commands, are applied automatically, internally within the device:

- A *low-pass filter* on each input pin allows noise glitches to be ignored.
- *Clock counting* allows the device to time-out if the validity of the write operation becomes dubious (such as if it has exceeded the maximum specified duration).

Other defences can be applied only at the command of the external circuitry. This is potentially the strongest defence since the external circuitry can be designed to monitor for quite elaborate conditions that are specific to the particular application.

- The *Write Control* pin (WC) can be used to disable write sequences completely when conditions are unstable.
- The user-defined Read-Only Area, along with a previously set-up address pointer in the memory, can be used to make the selected block behave like ROM.

It is possible to overlap the effects of the internal and external defences. For example, de-assertion of the WC pin, during a write cycle on some devices, causes the internal write cycle to be aborted. This is a useful fail-safe defence if the source of the glitch on the WC line is also injecting noise on the data lines.

Table 1 shows the different memory ranges, capacities and features of ST's serial EEPROMs.

Table 1. ST Serial EEPROMs (in production or for release in 1995)

Bus Type	Series	Capacity	Sequential Read	Page Write	Write Control	Write Protection
I^2C	ST24Cxx	1 Kbit-16 Kbit	x	x		4 Kbit-16 Kbit
	ST24Wxx	1 Kbit-16 Kbit	x	x		4 Kbit-16 Kbit
	M24Cxx	1 Kbit-16 Kbit	x	x	x	
XI^2C	M24xxx	16 Kbit-256 Kbit	x	x	x	
SPI	M95xxx	1 Kbit-64 Kbit	x	x	x	x
MICROWIRE	M93Cxx	256 bit-4 Kbit	x	x		
	M93Sxx	1 Kbit-4 Kbit	x	x		x

Because of its better clock counting protocol, the XI^2C standard offers good noise immunity. Each 8-bit data transfer is accompanied by a ninth bit acknowledge by the device on the bus which is the current data receiver. Moreover, a memory write cycle can only be triggered after both a correct series of acknowledges and a corresponding correct count of clock pulses. Products that include an external write control input give added protection to the memory, especially during power up.

These EEPROMs are designed to function even when V_{CC} has dropped to 1.8 V, and can be functional as low as 1.5 V. However, because the MCU is not necessarily guaranteed to be functional at these voltages, random signals from the MCU can trigger spurious write cycles. This can be prevented by holding the write control inputs low, along with the MCU reset signal, until the bus signals are stable. Both I^2C ("W" series) and XI^2C ("E" series) products from ST feature write control inputs. In addition, the XI^2C types include an input filter on the data lines which rejects pulses narrower than 50 ns, thus filtering short noise glitches.

The I^2C EEPROMs (“ST24Cxx” and “ST24Wxx” series, 4 Kbit to 16 Kbit capacities) also offer software programmed data protection. Up to half of the memory can be made to behave like ROM. A non-volatile register is set up to point to the address at which the write protection begins.

Of the two higher speed buses, SPI and MICROWIRE, SPI offers the better noise immunity and the greater data protection. The SPI protocol reads instructions, addresses and data from the bus by sampling on the rising edge of the clock. Since all transfers are in 8-bit format, this allows an internal counter to inhibit writing to the memory should the chip select go high, to indicate the start of a write cycle, when the count is not a multiple of eight. Additional immunity is provided by the instruction set which includes commands to enable a write control latch before a write cycle can begin. Lastly, detection of an incorrect command instruction will automatically de-select the chip.

Data protection in the SPI products is provided by both an external write protect input, like the I^2C and XI^2C devices, plus a programmable, non-volatile block protection scheme that allows zero, 25%, 50% or 75% of the total memory array to be write protected.

The protocol of the MICROWIRE bus has several features that allow protection against spurious glitches on data or clock lines. Two families of MICROWIRE products offer different levels data protection. The “S” family offers both a write enable input and programmable block write protection, in addition to the data protection features that were already provided in the older “C” family.

THE MEMORY ENDURANCE

A final consideration when choosing an EEPROM device is its reliability after repeated write/erase cycles. All types of non-volatile memory using floating-gate technology suffer from a gradual wear-out of the oxide. This leads to a deterioration of the cells’ ability to store a “1” or a “0”, and hence to malfunction and loss of data.

The endurance of the memory depends on the quality of the CMOS manufacturing process, the technology and the memory cell design. ST EEPROMs use a unique and very successful cell layout and process technology which is able to offer a performance of over one million write/erase cycles for medium capacity memory devices (up to 16 Kbit). This is ten times better than competitive products, and even if not called for in the specific application, it can be viewed as an additional “noise protection”, as it guarantees much better security of memory retention during the lifetime of the equipment.

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.eeprom@st.com (for application support)

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.

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