12-Bit-ADC with Microprocessor Interface

AD574

1.0 SCOPE

This specification documents the detailed requirements for Analog Devices space qualified die including die qualification as described for Class K in MIL-PRF-38534, Appendix C, Table C-II except as modified herein.

The manufacturing flow described in the STANDARD DIE PRODUCTS PROGRAM brochure at http://www.analog.com/marketSolutions/militaryAerospace/pdf/Die_Broc.pdf is to be considered a part of this specification.

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD574

2.0 Part Number. The complete part number(s) of this specification follow:

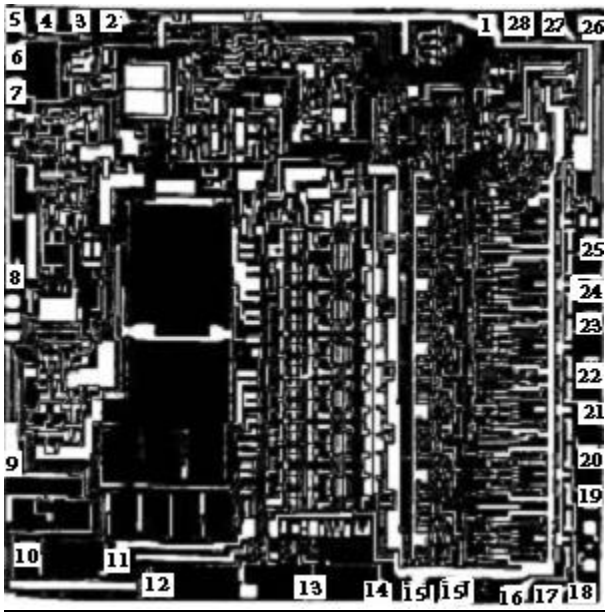
Part Number	Description
AD574-000C	12-Bit-ADC with Microprocessor Interface
AD574R000C	Radiation Tested 12-Bit-ADC with Microprocessor Interface

3.0 Die Information

3.1 Die Dimensions

Die Size	Die Thickness	Bond Pad Metalization
179 x 180	19 mil ± 2 mil	Al/Cu

3.2 Die Picture



1 V_{LOGIC}	28 STATUS
2 12/ $\overline{8}$	27 DB11
3 $\overline{CS}$	26 DB10
4 A_0	25 DB9
5 R/$\overline{C}$	24 DB8
6 CE	23 DB7
7 V_{CC}	22 DB6
8 REF_{OUT}	21 DB5
9 AC	20 DB4
10 REF_{IN}	19 DB3
11 V_{EE}	18 DB2
12 BIP OFF	17 DB1
13 $10V_{IN}$	16 DB0
14 $20V_{IN}$	15 DC

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3.3 Absolute Maximum Ratings

V_{CC} to Digital Common…..... 0 to +16.5V dc
V_{EE} to Digital Common…..... 0 to -16.5V dc
V_{LOG} to Digital Common…..... 0 to +7V dc
Analog to Digital Common..... ±1V dc
Control Inputs (CE, $\overline{CS}$, A_O, 12/8, R/ $\overline{C}$) to Digital Common……..-0.5V dc to V_{LOG}+0.5V dc
Analog Inputs (REF IN, BIP OFF, 10 V_{IN}) to Analog Common……V_{EE} to V_{CC}
20 V_{IN} Analog Input Voltage to Analog Common ..... ±24V dc
$V_{REF\ OUT}$ .....Indefinite short to
.....common, 10mS
.....short to V_{CC}
Storage Temperature .....-65°C to +150°C
Junction Temperature (T_J)…… .....……..+175°C
Operating Temperature Range.....-55°C to +125°C

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4.0 Die Qualification

In accordance with class-K version of MIL-PRF-38534, Appendix C, Table C-II, except as modified herein.
(a) Qual Sample Size and Qual Acceptance Criteria – 10/0
(b) Qual Sample Package – Ceramic DIP
(c) Pre-screen electrical test over temperature performed post-assembly prior to die qualification.

Table I -Dice Electrical Characteristics

Parameter	Symbol	Conditions 1/	Limit Min	Limit Max	Units
Power Supply Current From V_{LOG}	I_{LOG}			40	mA
Power Supply Current From V_{CC}	I_{CC}			5	mA
Power Supply Current From V_{EE}	I_{EE}		-30		mA
Resolution			12		Bits
Integral Linearity Error Differential Linearity Error (Minimum Resolution For Which No Missing Codes Guaranteed)	ILE DLE		-0.5 12	0.5	LSB Bits
Unipolar Offset Voltage Error	V_{IO}		-2.0	2.0	LSB

Table I – Dice Electrical Characteristics (Continued)					
Parameter	**Symbol**	**Conditions 1/**	**Limit Min**	**Limit Max**	**Units**
Bipolar Offset Voltage Error	B_Z		-4.0	4.0	LSB
Gain Error	ΔA_E	With 50Ω resistor from REF OUT to REF IN		.25	% of F.S.
Power Supply Sensitivity (Maximum Change In Full Scale Calibration)	$+P_{SS1}$	$+13.5V \le V_{CC} \le +16.5V$	-1.0	1.0	LSB
	$+P_{SS2}$	$+11.4V \le V_{CC} \le +12.6V$			
	$+P_{SS3}$	$+4.5V \le V_{LOG} \le +5.5V$	-0.5	0.5	
	$-P_{SS1}$	$-16.5V \le V_{EE} \le -13.5V$	-1.0	1.0	
	$-P_{SS2}$	$-12.6V \le V_{EE} \le -11.4V$			
Input Impedance	Z_{IN}	10V span	3	7	kΩ
		20V span	6	14	
Internal Reference Voltage	V_{REF}	2/	9.98	10.02	V
Input Voltage (CE, $\overline{CS}$, 12/8, R/$\overline{C}$, A_0) 3/	V_{IH}	Logic "1"	2.0	5.5	V
	V_{IL}	Logic "0"	-0.5	0.8	
Input Current	I_{IN}		-20	+20	µA
Output Voltage (DB11-DB0,STS)	V_{OL}	Logic "0", I_{SINK}=+1.6mA		0.4	V
Output Voltage (DB11-DB0)	V_{OH}	Logic "1", I_{SOURCE}=+500µA	2.4		V
High Impedance State Output Current	I_Z	High-Z state, DB11 – DB0 only	-20	+20	µA

Table I Notes:

1/ V_{CC} = ±15V, V_{LOG} = +5V, V_{EE} = -15V, T_A = 25°C, unless otherwise specified.

2/ The reference voltage external load current shall be a constant dc and shall not exceed 1.5 mA. Reference should be buffered for operation of ±12V supplies. External load should not change during conversion.

3/ 12/ 8 is not TTL compatible and must be hard wired to V_{LOG} or digital ground.

Table II - Electrical Characteristics for Qual Samples						
Parameter	**Symbol**	**Conditions 1/**	**Sub-groups**	**Limit Min**	**Limit Max**	**Units**
Power Supply Current From V_{LOG}	I_{LOG}		1, 2, 3		40	mA
		M, D, L, R 5/	1		40	
Power Supply Current From V_{CC}	I_{CC}		1, 2, 3		5	
		M, D, L, R 5/	1		5	
Power Supply Current From V_{EE}	I_{EE}		1, 2, 3	-30		
		M, D, L, R 5/	1	-30		
Integral Linearity Error	ILE		1	-0.5	0.5	LSB
			2, 3	-1.0	1.0	
		M, D, L, R 5/	1	-1.0	1.0	
Differential Linearity Error (Minimum Resolution For Which No Missing Codes Guaranteed) 6/	DLE		1	12		Bits
			2, 3	12		
Unipolar Offset Voltage Error	V_{IO}	Using internal reference	1	-2.0	2.0	LSB
		M, D, L, R 5/	1	-3.0	3.0	
Unipolar Offset Drift 6/	$\frac{\Delta V_{IO}}{\Delta T}$	Using internal reference	2, 3	-1.0	1.0	
Bipolar Offset Voltage Error	B_Z	Using internal reference	1	-4.0	4.0	
		M, D, L, R 5/	1	-5.0	5.0	
Bipolar Zero Offset Drift 6/	$\frac{\Delta B_Z}{T}$	Using internal reference	2, 3	-2.0	+2.0	
Gain Error	ΔA_E	With 50Ω resistor from REF OUT to REF IN	1		.25	% of F.S.
		M, D, L, R 5/	1		.35	
Gain Error Drift 6/	$\frac{\Delta A_E}{\Delta T}$	Using internal reference	2, 3	-25.0	25.0	ppm/ °C
Power Supply Sensitivity (Maximum Change In Full Scale Calibration) 6/	$+P_{SS1}$	$+13.5V \le V_{CC} \le +16.5V$	1	-1.0	1.0	LSB
	$+P_{SS2}$	$+11.4V \le V_{CC} \le +12.6V$				
	$+P_{SS3}$	$+4.5V \le V_{LOG} \le +5.5V$	1	-0.5	0.5	
	$-P_{SS1}$	$-16.5V \le V_{EE} \le -13.5V$	1	-1.0	1.0	
	$-P_{SS2}$	$-12.6V \le V_{EE} \le -11.4V$				
Input Impedance 6/	Z_{IN}	10V span	1	3	7	kΩ
		20V span	1	6	14	

Table II - Electrical Characteristics for Qual Samples

Parameter	Symbol	Conditions 1/	Sub-groups	Limit Min	Limit Max	Units
Output Voltage (DB11-DB0, STS) 6/	V_{OL}	Logic "0", T_A = +25°C, I_{SINK} = +1.6mA	1, 2, 3		40	mA
Output Voltage (DB11-DB0) 6/	V_{OH}	Logic "1", T_A = +25°C, I_{SOURCE} = +500µA	1	2.4		V
High Impedance State Output Current 6/	I_Z	High-Z state, T_A = +25°C, DB11-DB0 only	1	-20	+20	µA
Low R/$\overline{C}$ Pulse Width 4/ 6/	t_{HRL}		9	250		ns
STS Delay from R/$\overline{C}$ 4/ 6/	t_{DS}		9		600	ns
Data Valid After R/$\overline{C}$ Low 4/ 6/	t_{HDR}		9		25	ns
STS Delay After Valid Data 4/ 6/	t_{HS}		9	300	1000	ns
High R/$\overline{C}$ Pulse Width 6/	t_{HRH}		9	300		ns
Data Access Time 6/	t_{DDR}		9		250	ns
STS Delay from CE 6/	t_{DSC}		9		350	ns
CE Pulse Width 6/	t_{HEC}		9	300		ns
Conversion Time 6/	t_C	8-bit cycle	9	10	24	µs
		12-bit cycle	9	15	35	
Access Time (from CE) 6/	t_{DD}		9		200	ns

Table II Notes:

1/ V_{CC} = ±15V, V_{LOG} = +5V, V_{EE} = -15V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified.

2/ The reference voltage external load current shall be a constant dc and shall not exceed 1.5 mA. Reference should be buffered for operation of ±12V supplies. External load should not change during conversion.

3/ 12/8 is not TTL compatible and must be hard wired to V_{LOG} or digital ground.

4/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits.

5/ Tested at 100Krad

6/ Not Tested Post Irradiation.

Table III - Delta Parameter Table								
Parameter	Symbol	Sub-groups	Post Burn In Limit		Post Life Test Limit		Life Test Delta	Units
			Min	Max	Min	Max		
Unipolar Offset Voltage Error	Uni V_{IO}	1	-2.0	2.0	-2.5	2.5	±0.5	LSB
Bipolar Offset Voltage Error	Bpze	1	-4.0	4.0	-5.0	5.0	±1.0	LSB
Gain Error	A_E	1	-0.25	0.25	-0.25	0.35	±.10	%FSR

5.0 Life Test/Burn-In Information

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B or C.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	04-Oct-2001
B	Update web address	Jan. 25, 2002
C	Update web address. Add Radiation limits and part number.	4-Mar-03
D	Update 1.0 Scope description.	2 Aug. 2007
E	Update header/footer & add to 1.0 Scope description.	Feb. 14, 2008
F	Remove reference to condition 5/ note on Table I & add Junction Temperature (T_J)..... +175°C & Operating Temperature Range....-55°C to +125°C to Section 3.3-Absolute Max. Ratings	March 27, 2008
G	Updated Section 4.0c note to indicate pre-screen temp testing being performed.	6-JUN-2009
H	Updated Font and Font Size to Standardize to ADI format	20-Sep-2011

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