

## 93L34 8-Bit Addressable Latch

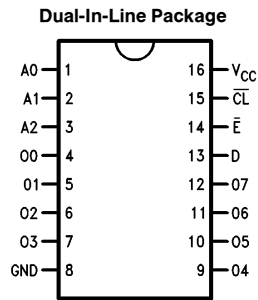
### General Description

The 93L34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

### Features

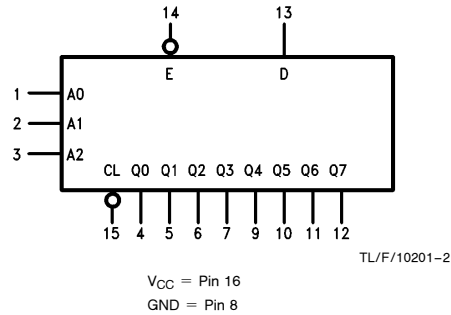
- Serial to parallel capability
- Eight bits of storage with output of each bit available
- Random (addressable) data entry
- Active high demultiplexing or decoding capability
- Easily expandable
- Common conditional clear

### Connection Diagram



TL/F/10201-1

### Logic Symbol



Order Number 93L34DMQB or 93L34FMQB  
See NS Package Number J16A or W16A

| Pin Names  | Description               |
|------------|---------------------------|
| A0-A3      | Address Inputs            |
| D          | Data Input                |
| $\bar{E}$  | Enable Input (Active LOW) |
| $\bar{CL}$ | Clear Input (Active LOW)  |
| Q0-Q7      | Parallel Latch Outputs    |

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                      |                 |
|--------------------------------------|-----------------|
| Supply Voltage                       | 7V              |
| Input Voltage                        | 5.5V            |
| Operating Free Air Temperature Range |                 |
| Military                             | –55°C to +125°C |
| Storage Temperature Range            | –65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol             | Parameter                       | 93L34 (Mil) |     |      | Units |
|--------------------|---------------------------------|-------------|-----|------|-------|
|                    |                                 | Min         | Nom | Max  |       |
| V <sub>CC</sub>    | Supply Voltage                  | 4.5         | 5   | 5.5  | V     |
| V <sub>IH</sub>    | High Level Input Voltage        | 2           |     |      | V     |
| V <sub>IL</sub>    | Low Level Input Voltage         |             |     | 0.7  | V     |
| I <sub>OH</sub>    | High Level Output Voltage       |             |     | –400 | μA    |
| I <sub>OL</sub>    | Low Level Output Current        |             |     | 4.8  | mA    |
| T <sub>A</sub>     | Free Air Operating Temperature  | –55         |     | 125  | °C    |
| t <sub>s</sub> (H) | Setup Time HIGH, D to $\bar{E}$ | 45          |     |      | ns    |
| t <sub>h</sub> (H) | Hold Time HIGH, D to $\bar{E}$  | –5          |     |      | ns    |
| t <sub>s</sub> (L) | Setup Time LOW, D to $\bar{E}$  | 45          |     |      | ns    |
| t <sub>h</sub> (L) | Hold Time LOW, D to $\bar{E}$   | –7          |     |      | ns    |
| t <sub>s</sub> (H) | Setup Time HIGH or LOW          | 10          |     |      | ns    |
| t <sub>s</sub> (L) | A <sub>n</sub> to $\bar{E}$     | 10          |     |      | ns    |
| t <sub>w</sub> (L) | $\bar{E}$ Pulse Width LOW       | 26          |     |      | ns    |
| t <sub>w</sub> (L) | $\bar{C}L$ Pulse Width LOW      | 35          |     |      | ns    |

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol          | Parameter                         | Conditions   | Min       | Typ (Note 1) | Max  | Units |
|-----------------|-----------------------------------|--|-----------|--------------|------|-------|
| V <sub>I</sub>  | Input Clamp Voltage               | V <sub>CC</sub> = Min, I <sub>I</sub> = –10 mA   |           |              | –1.5 | V     |
| V <sub>OH</sub> | High Level Output Voltage         | V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min | 2.4       |              |      | V     |
| V <sub>OL</sub> | Low Level Output Voltage          | V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min, V <sub>IL</sub> = Max |           |              | 0.3  | V     |
| I <sub>I</sub>  | Input Current @ Max Input Voltage | V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V   |           |              | 1    | mA    |
| I <sub>IH</sub> | High Level Input Current          | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V   | Inputs    |              | 20   | μA    |
|                 |                                   |  | $\bar{E}$ |              | 30   |       |
| I <sub>IL</sub> | Low Level Input Current           | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.3V   | Inputs    |              | –0.4 | mA    |
|                 |                                   |  | $\bar{E}$ |              | –0.6 |       |
| I <sub>OS</sub> | Short Circuit Output Current      | V <sub>CC</sub> = Max (Note 2)   | –2.5      |              | –25  | mA    |
| I <sub>CC</sub> | Supply Current                    | V <sub>CC</sub> = Max (Note 3)   |           |              | 21   | mA    |

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I<sub>CC</sub> is measured with all outputs open and all inputs grounded.

**Switching Characteristics**  $V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

| Symbol                 | Parameter                                | $C_L = 15\text{ pF}$ |          | Units |
|------------------------|--|----------------------|----------|-------|
|                        |  | Min                  | Max      |       |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\bar{E}$ to $Q_n$  |                      | 45<br>42 | ns    |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>D to $Q_n$          |                      | 65<br>45 | ns    |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_n$ to $Q_n$      |                      | 66<br>66 | ns    |
| $t_{PHL}$              | Propagation Delay<br>$\bar{C}L$ to $Q_n$ |                      | 55       | ns    |

**Functional Description**

The 93L34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 93L34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

**Mode Select Table**

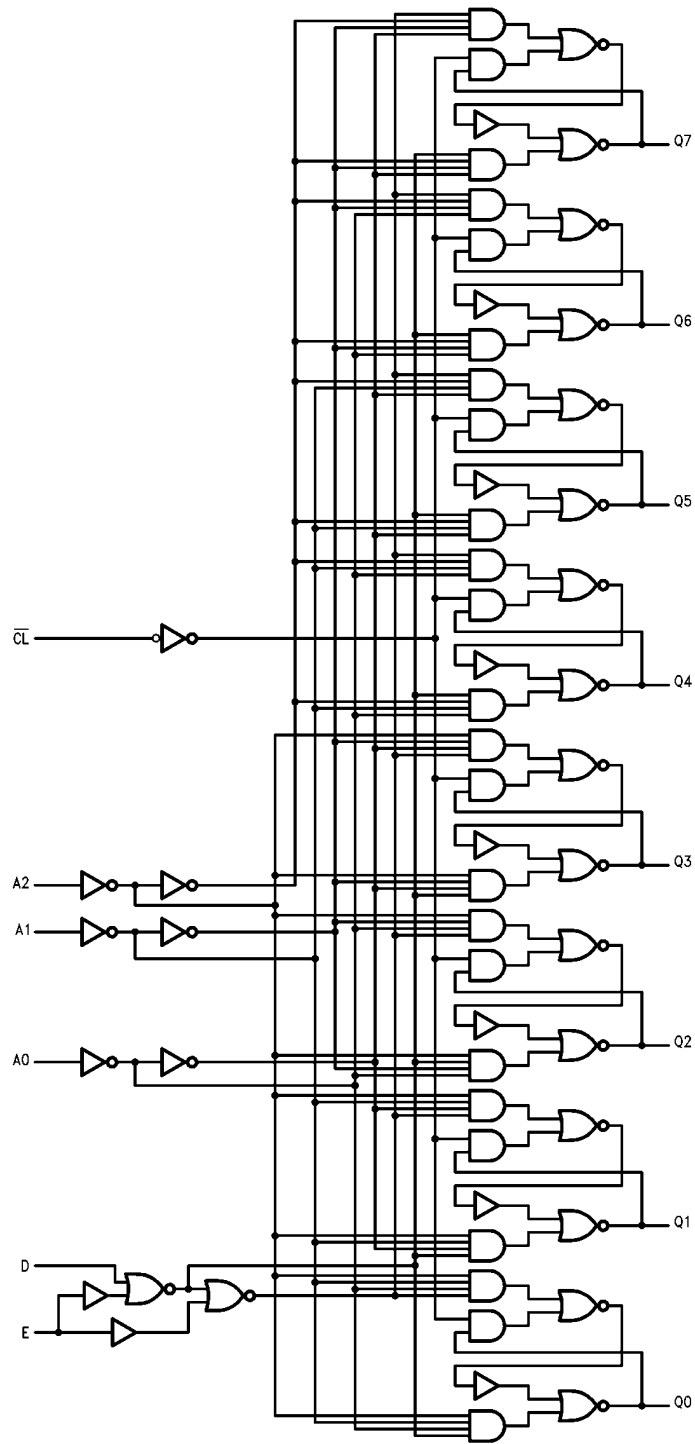
| $\bar{E}$ | $\bar{C}L$ | Mode                                |
|-----------|------------|-------------------------------------|
| L         | H          | Addressable Latch                   |
| H         | H          | Memory                              |
| L         | L          | Active HIGH 8-Channel Demultiplexer |
| H         | L          | Clear                               |

## Truth Table

| Inputs          |                |    |    |    | Outputs |      |      |      |      |      |      |      | Mode |                      |
|-----------------|----------------|----|----|----|---------|------|------|------|------|------|------|------|------|----------------------|
| $\overline{CL}$ | $\overline{E}$ | A0 | A1 | A2 | Q0      | Q1   | Q2   | Q3   | Q4   | Q5   | Q6   | Q7   |      |                      |
| L               | H              | X  | X  | X  | L       | L    | L    | L    | L    | L    | L    | L    | L    | Clear<br>Demultiplex |
| L               | L              | L  | L  | L  | D       | L    | L    | L    | L    | L    | L    | L    | L    |                      |
| L               | L              | H  | L  | L  | L       | D    | L    | L    | L    | L    | L    | L    | L    |                      |
| L               | L              | L  | H  | L  | L       | L    | D    | L    | L    | L    | L    | L    | L    |                      |
| •               | •              | •  | •  | •  | •       | •    | •    | •    | •    | •    | •    | •    | •    |                      |
| •               | •              | •  | •  | •  | •       | •    | •    | •    | •    | •    | •    | •    | •    |                      |
| L               | L              | H  | H  | H  | L       | L    | L    | L    | L    | L    | L    | L    | L    |                      |
| H               | H              | X  | X  | X  | Qt-1    | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Memory               |
| H               | L              | L  | L  | L  | D       | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Addressable<br>Latch |
| H               | L              | H  | L  | L  | Qt-1    | D    | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 |                      |
| H               | L              | L  | H  | L  | Qt-1    | Qt-1 | D    | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 |                      |
| •               | •              | •  | •  | •  | •       | •    | •    | •    | •    | •    | •    | •    | •    |                      |
| •               | •              | •  | •  | •  | •       | •    | •    | •    | •    | •    | •    | •    | •    |                      |
| H               | L              | H  | H  | H  | Qt-1    | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | Qt-1 | D    |                      |

H = HIGH Voltage Level    L = LOW Voltage Level    X = Immaterial    Qt-1 = Previous Output State

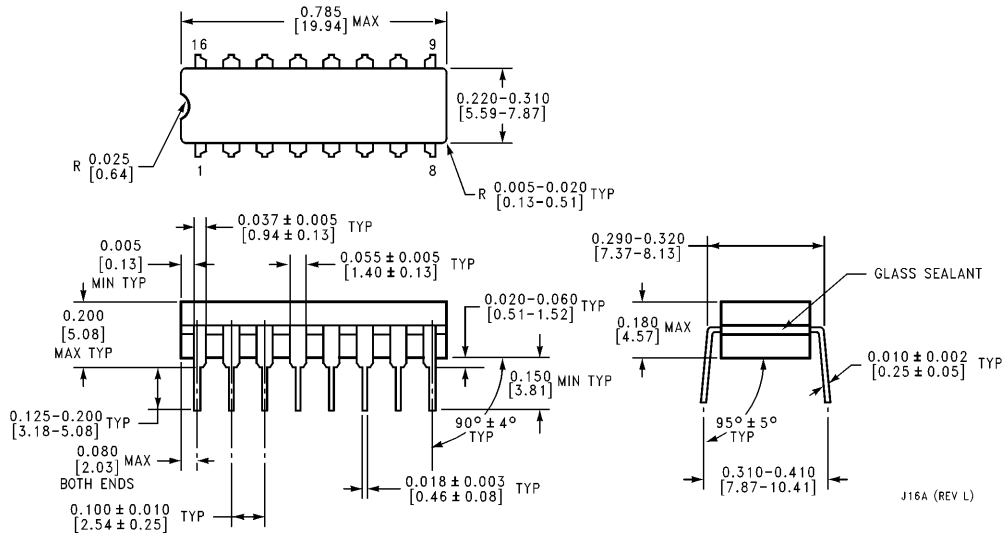
# Logic Diagram



TL/F/10201-3



**Physical Dimensions** inches (millimeters)

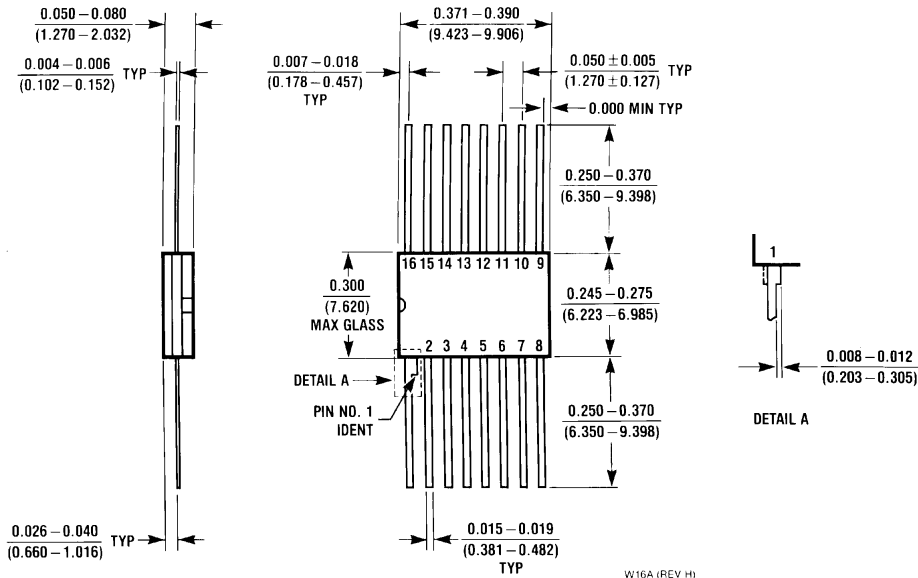


**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 93L34DMQB**  
**NS Package Number J16A**

J16A (REV L)

**93L34 8-Bit Addressable Latch**

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flat Package (W)**  
**Order Number 93L34FMQB**  
**NS Package Number W16A**

W16A (REV. H)

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