

# DATA SHEET

## **74HC1G66; 74HCT1G66** **Bilateral switch**

Product specification  
Supersedes data of 2001 Mar 02

2002 May 15

## Bilateral switch

## 74HC1G66; 74HCT1G66

## FEATURES

- Wide operating voltage range from 2.0 to 9.0 V
- Very low ON-resistance:
  - 45  $\Omega$  (typical) at  $V_{CC} = 4.5$  V
  - 30  $\Omega$  (typical) at  $V_{CC} = 6.0$  V
  - 25  $\Omega$  (typical) at  $V_{CC} = 9.0$  V.
- High noise immunity
- Low power dissipation
- Very small 5 pins package
- Output capability: non standard.

## DESCRIPTION

The 74HC1G/HCT1G66 is a high-speed Si-gate CMOS device.

The 74HC1G/HCT1G66 provides an analog switch. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

The non standard output currents are equal compared to the 74HC/HCT4066.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f = 6.0$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC1G	HCT1G	
$t_{PZH}/t_{PZL}$	turn-on time E to $V_{os}$	$C_L = 15$ pF; $R_L = 1$ k $\Omega$ ; $V_{CC} = 5$ V	11	12	ns
$t_{PHZ}/t_{PLZ}$	turn-off time E to $V_{os}$	$C_L = 15$ pF; $R_L = 1$ k $\Omega$ ; $V_{CC} = 5$ V	11	12	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance	notes 1 and 2	9	9	pF
$C_S$	maximum switch capacitance		8	8	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$C_S$  = maximum switch capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. For HC1G the condition is  $V_I = \text{GND to } V_{CC}$ .

For HCT1G the condition is  $V_I = \text{GND to } V_{CC} - 1.5$  V.

## FUNCTION TABLE

See note 1.

INPUT E	SWITCH
L	OFF
H	ON

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

Bilateral switch

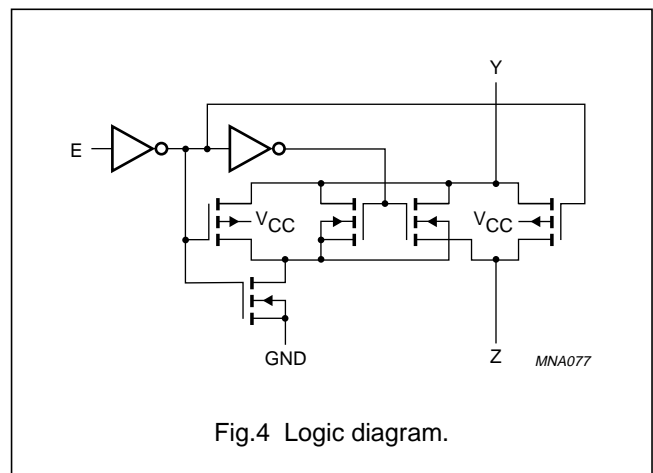
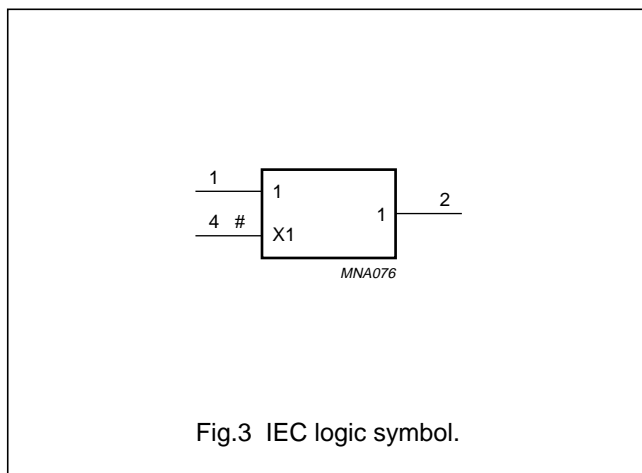
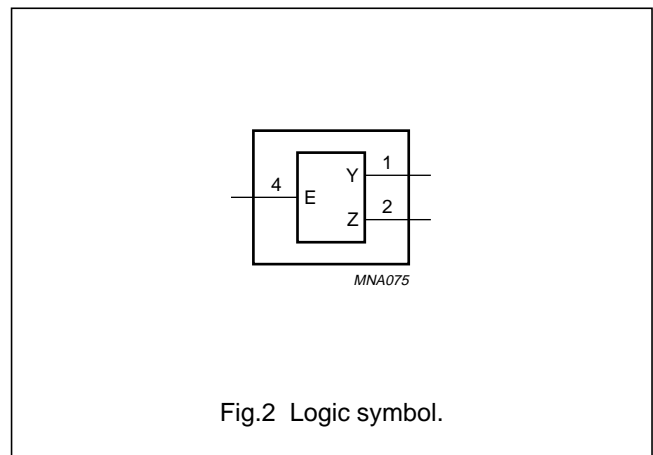
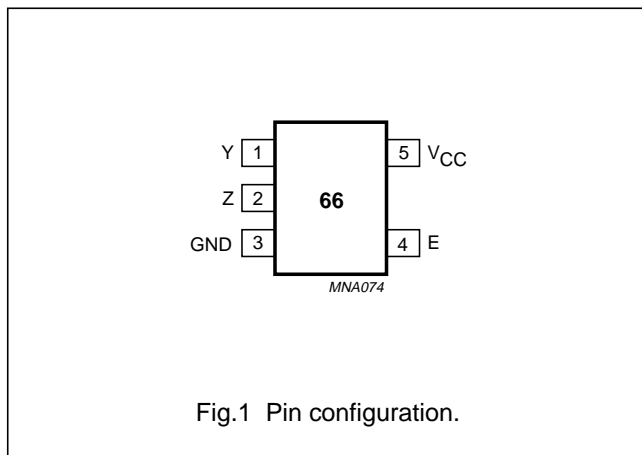
74HC1G66; 74HCT1G66

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC1G66GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	HL
74HCT1G66GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	TL
74HC1G66GV	-40 to +125 °C	5	SC-74A	plastic	SOT753	H66
74HCT1G66GV	-40 to +125 °C	5	SC-74A	plastic	SOT753	T66

PINNING

PIN	SYMBOL	DESCRIPTION
1	Y	independent input/output Y
2	Z	independent input/output Z
3	GND	ground (0 V)
4	E	enable input E (active HIGH)
5	V <sub>CC</sub>	supply voltage



## Bilateral switch

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC1G66			74HCT1G66			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
$V_I$	input voltage		GND	–	$V_{CC}$	GND	–	$V_{CC}$	V
$V_S$	switch voltage		GND	–	$V_{CC}$	GND	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	–	+125	–40	–	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns
		$V_{CC} = 10.0\text{ V}$	–	–	250	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); see note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+11.0	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_{SK}$	switch diode current	$V_S < -0.5\text{ V}$ or $V_S > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_S$	switch source or sink current	$-0.5\text{ V} < V_S < V_{CC} + 0.5\text{ V}$	–	±25	mA
$I_{CC}$	$V_{CC}$ or GND current		–	±50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_D$	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	200	mW
$P_S$	power dissipation per switch		–	100	mW

## Notes

- To avoid drawing  $V_{CC}$  current out of pin Z, when switch current flows in pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no  $V_{CC}$  current will flow out of terminal Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed  $V_{CC}$  or GND.
- Above 55 °C the value of  $P_D$  derates linearly with 2.5 mW/K.

## Bilateral switch

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## DC CHARACTERISTICS

## Family 74HC1G66

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb}$ (°C)					UNIT
		OTHER	$V_{CC}$ (V)	-40 to +85			-40 to +125		
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
$V_{IH}$	HIGH-level input voltage		2.0	1.5	1.2	–	1.5	–	V
			4.5	3.15	2.4	–	3.15	–	V
			6.0	4.2	3.2	–	4.2	–	V
			9.0	6.3	4.7	–	6.3	–	V
$V_{IL}$	LOW-level input voltage		2.0	–	0.8	0.5	–	0.5	V
			4.5	–	2.1	1.35	–	1.35	V
			6.0	–	2.8	1.8	–	1.8	V
			9.0	–	4.3	2.7	–	2.7	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND	6.0	–	0.1	1.0	–	1.0	$\mu$ A
			10.0	–	0.2	2.0	–	2.0	$\mu$ A
$I_S$	analog switch current, OFF-state	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - \text{GND}$ ; see Fig.6	10.0	–	0.1	1.0	–	1.0	$\mu$ A
	analog switch current, ON-state	$V_I = V_{IH}$ or $V_{IL}$ ; $ V_S  = V_{CC} - \text{GND}$ ; see Fig.7	10.0	–	0.1	1.0	–	1.0	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{IS} = \text{GND}$ or $V_{CC}$ ; $V_{OS} = V_{CC}$ or GND	6.0	–	1.0	10	–	20	$\mu$ A
			10.0	–	2.0	20	–	40	$\mu$ A

## Note

1. All typical values are measured at  $T_{amb} = 25$  °C.

## Bilateral switch

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## Family 74HCT1G66

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)					UNIT
		OTHER	V <sub>CC</sub> (V)	-40 to +85			-40 to +125		
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	0.1	1.2	0.8	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	0.1	1.0	–	1.0	μA
I <sub>S</sub>	analog switch current, OFF-state	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  V <sub>S</sub>   = V <sub>CC</sub> – GND; see Fig.6	5.5	–	0.1	1.0	–	1.0	μA
	analog switch current, ON-state	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;  V <sub>S</sub>   = V <sub>CC</sub> – GND; see Fig.7	5.5	–	0.1	1.0	–	1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>is</sub> = GND or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or GND	4.5 to 5.5	–	1	10	–	20	μA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V	4.5 to 5.5	–	–	500	–	850	μA

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Bilateral switch

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## Family 74HC1G66 and 74HCT1G66

For 74HC1G66:  $V_{CC} = 2.0, 4.5, 6.0$  or  $9.0$  V; note 1.

For 74HCT1G66:  $V_{CC} = 4.5$  V.

SYMBOL	PARAMETER	TEST CONDITIONS			$T_{amb}$ (°C)					UNIT
		OTHER	$V_{CC}$ (V)	$I_S$ ( $\mu$ A)	-40 to +85			-40 to +125		
					MIN.	TYP. <sup>(2)</sup>	MAX.	MIN.	MAX.	
$R_{ON}$	ON-resistance (peak)	$V_{is} = V_{CC}$ to GND; $V_I = V_{IH}$ or $V_{IL}$ ; see Fig.5	2.0	100	–	–	–	–	–	$\Omega$
			4.5	1000	–	42	118	–	142	$\Omega$
			6.0	1000	–	31	105	–	126	$\Omega$
			9.0	1000	–	23	88	–	105	$\Omega$
	ON-resistance (rail)	$V_{is} = GND$ ; $V_I = V_{IH}$ or $V_{IL}$ ; see Fig.5	2.0	100	–	75	–	–	–	$\Omega$
			4.5	1000	–	29	95	–	115	$\Omega$
			6.0	1000	–	23	82	–	100	$\Omega$
			9.0	1000	–	18	70	–	80	$\Omega$
		$V_{is} = V_{CC}$ ; $V_I = V_{IH}$ or $V_{IL}$ ; see Fig.5	2.0	100	–	75	–	–	–	$\Omega$
			4.5	1000	–	35	106	–	128	$\Omega$
			6.0	1000	–	27	94	–	113	$\Omega$
			9.0	1000	–	21	78	–	95	$\Omega$

## Notes

- At supply voltages approaching 2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.
- All typical values are measured at  $T_{amb} = 25$  °C.

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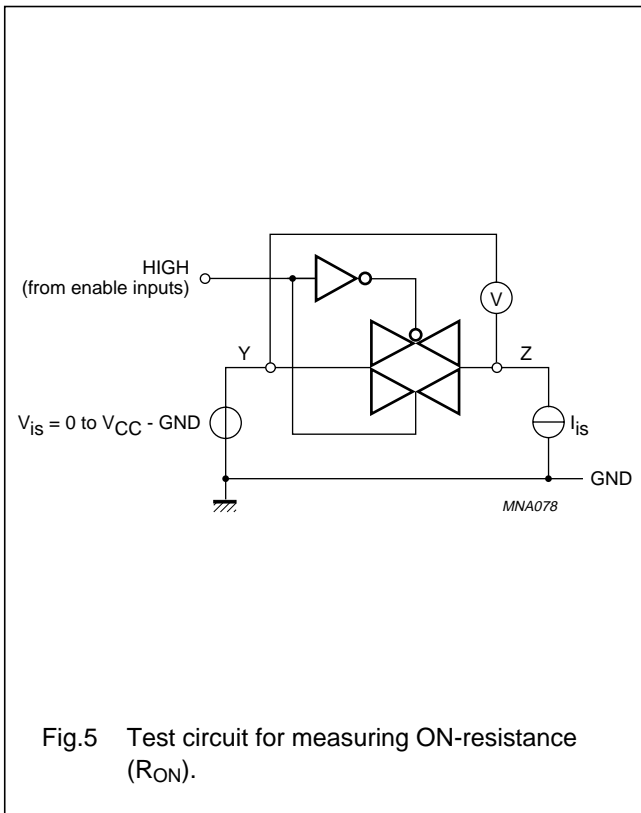


Fig.5 Test circuit for measuring ON-resistance ( $R_{ON}$ ).

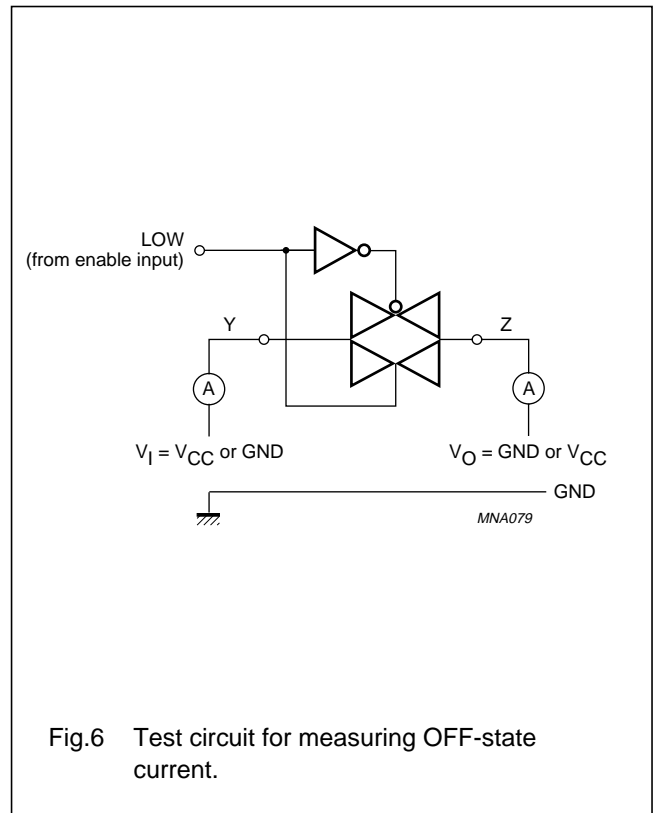


Fig.6 Test circuit for measuring OFF-state current.

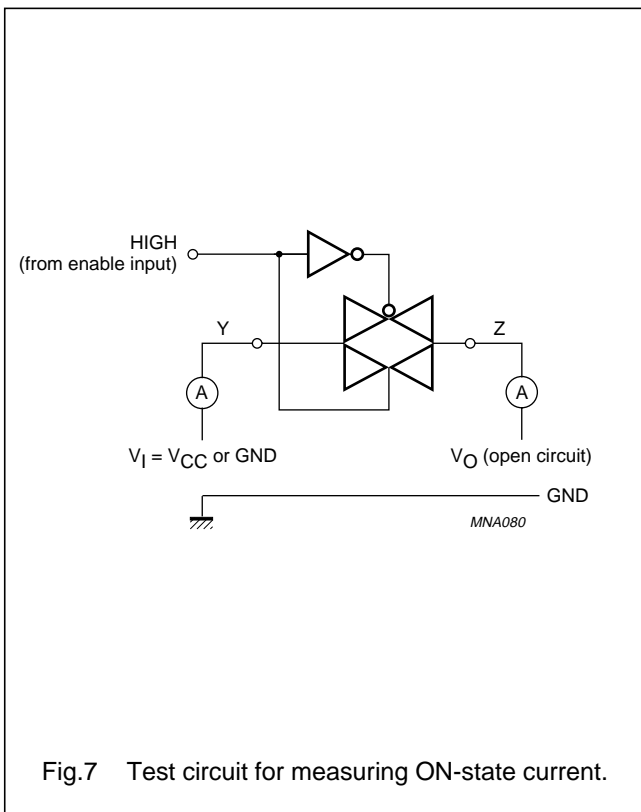


Fig.7 Test circuit for measuring ON-state current.

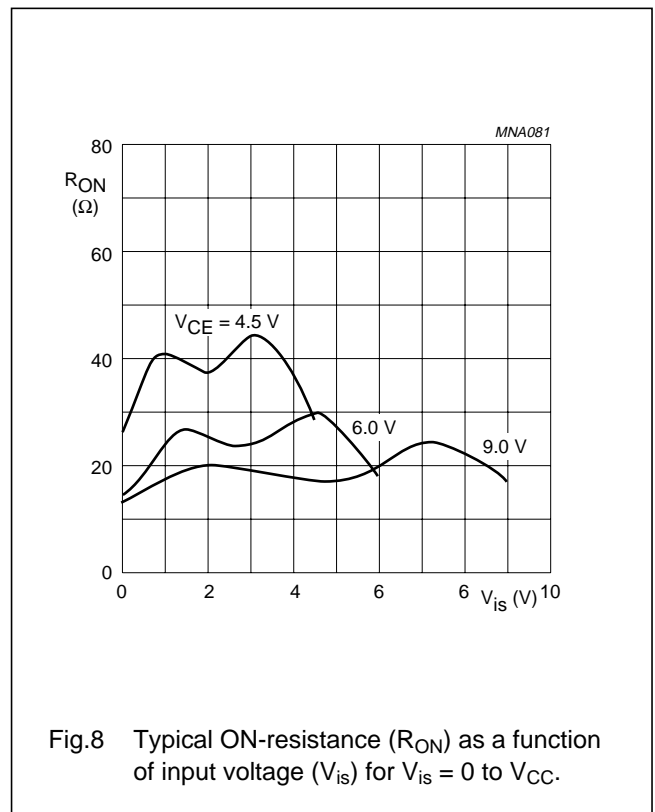


Fig.8 Typical ON-resistance ( $R_{ON}$ ) as a function of input voltage ( $V_{is}$ ) for  $V_{is} = 0 \text{ to } V_{CC}$ .

## Bilateral switch

## 74HC1G66; 74HCT1G66

## AC CHARACTERISTICS

## Type 74HC1G66

GND = 0 V;  $t_r = t_f = 6$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)					UNIT
		WAVEFORMS	V <sub>CC</sub> (V)	-40 to +85			-40 to +125		
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF; see Fig.12	2.0	–	8	75	–	90	ns
			4.5	–	3	15	–	18	ns
			6.0	–	2	13	–	15	ns
			9.0	–	1	10	–	12	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	turn-on time E to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figs 13 and 14	2.0	–	50	125	–	150	ns
			4.5	–	16	25	–	30	ns
			6.0	–	13	21	–	26	ns
			9.0	–	9	16	–	20	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	turn-off time E to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figs 13 and 14	2.0	–	27	190	–	225	ns
			4.5	–	16	38	–	45	ns
			6.0	–	14	33	–	38	ns
			9.0	–	12	16	–	20	ns

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Type 74HCT1G66

GND = 0 V;  $t_r = t_f = 6$  ns; V<sub>is</sub> is the input voltage at pins Y or Z, whichever is assigned as an input. V<sub>os</sub> is the output voltage at pins Y or Z, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)					UNIT
		WAVEFORMS	V <sub>CC</sub> (V)	-40 to +85			-40 to +125		
				MIN.	TYP. <sup>(1)</sup>	MAX.	MIN.	MAX.	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay V <sub>is</sub> to V <sub>os</sub>	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF; see Fig.12.	4.5	–	3	15	–	18	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	turn-on time E to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figs 15 and 16.	4.5	–	15	30	–	36	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	turn-off time E to V <sub>os</sub>	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF; see Figs 15 and 16.	4.5	–	13	44	–	53	ns

## Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

## Bilateral switch

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**Type 74HC1G66 and 74HCT1G66**

At recommended conditions and typical values. GND = 0 V;  $t_r = t_f = 6.0$  ns.  $V_{is}$  is the input voltage at pins Y or Z, whichever is assigned as an input;  $V_{os}$  is the output voltage at pins Y or Z, whichever is assigned as an output.

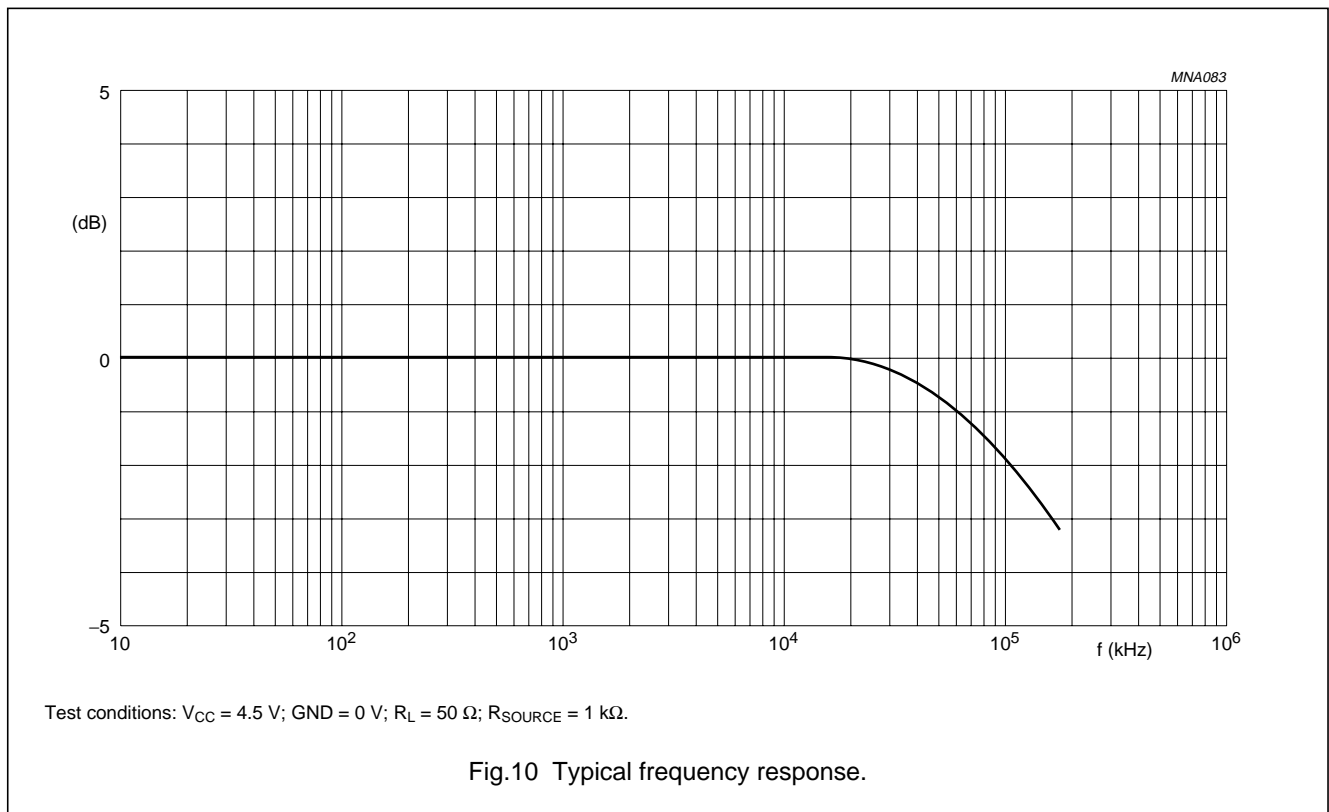
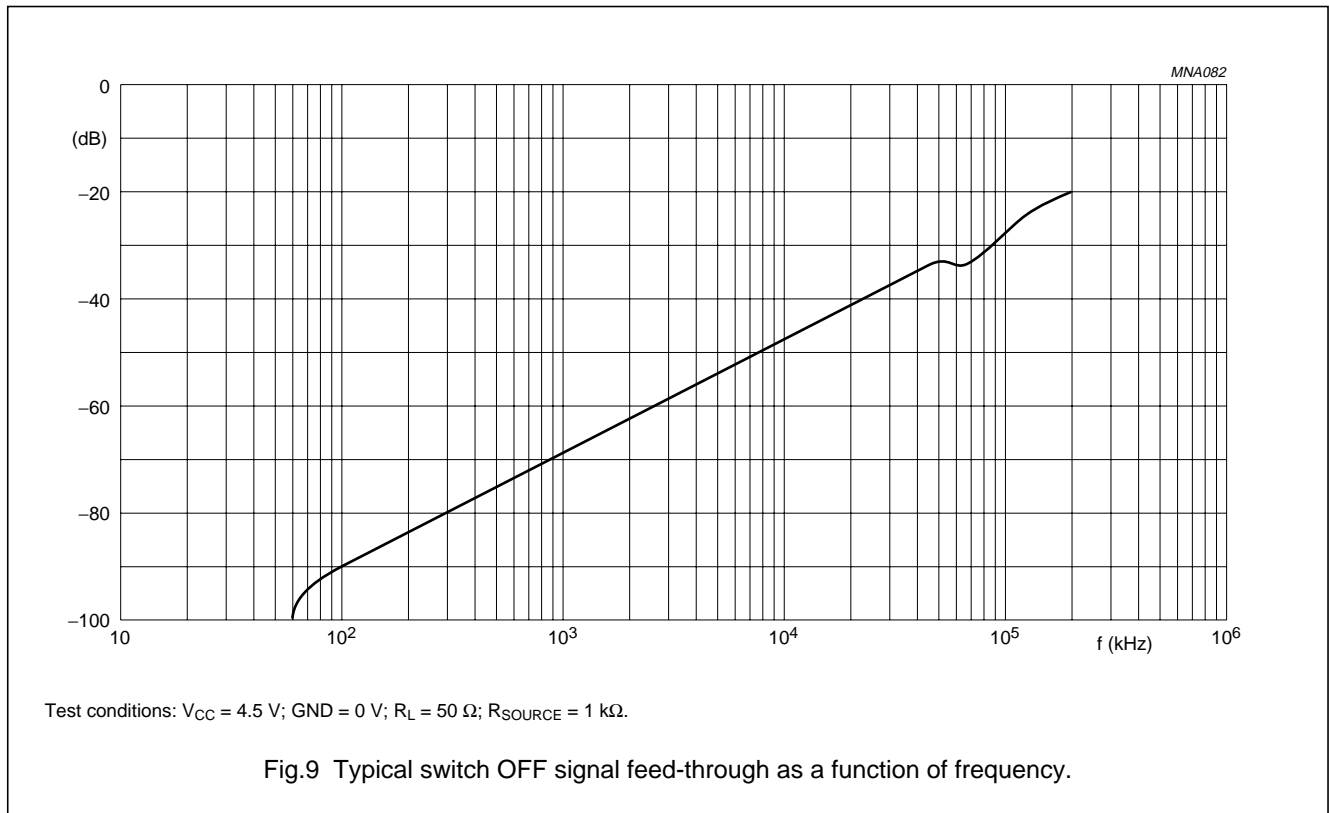
SYMBOL	PARAMETER	TEST CONDITIONS	$V_{is(p-p)}$ (V)	$V_{CC}$ (V)	TYP.	UNIT
	sine-wave distortion $f = 1$ kHz	$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; see Fig.12	4.0	4.5	0.04	%
			8.0	9.0	0.02	%
	sine-wave distortion $f = 10$ kHz	$R_L = 10$ k $\Omega$ ; $C_L = 50$ pF; see Fig.12	4.0	4.5	0.12	%
			8.0	9.0	0.06	%
	switch OFF signal feed-through	$R_L = 600$ $\Omega$ ; $C_L = 50$ pF; $f = 1$ MHz; see Figs 9 and 13	note 1	4.5	-50	dB
				9.0	-50	dB
$f_{max}$	minimum frequency response (-3 dB)	$R_L = 50$ $\Omega$ ; $C_L = 10$ pF; see Figs 10 and 11	note 2	4.5	180	MHz
				9.0	200	MHz
$C_S$	maximum switch capacitance				8	pF

**Notes**

1. Adjust input voltage  $V_{is}$  is 0 dBm level (0 dBm = 1 mW into 600  $\Omega$ ).
2. Adjust input voltage  $V_{is}$  is 0 dBm level at  $V_{os}$  for 1 MHz (0 dBm = 1 mW into 50  $\Omega$ ).

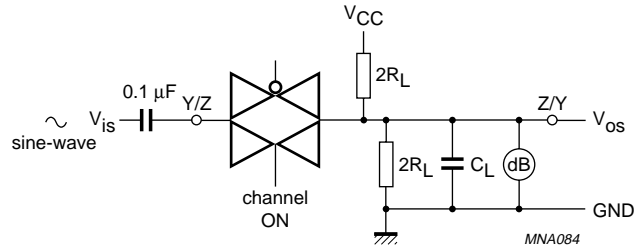
Bilateral switch

74HC1G66; 74HCT1G66



Bilateral switch

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Adjust input voltage to obtain 0 dBm at  $V_{os}$  when  $f_{in} = 1$  MHz.  
 After set-up, frequency of  $f_{in}$  is increased to obtain a reading of  $-3$  db at  $V_{os}$ .

Fig.11 Test circuit for measuring minimum frequency response.

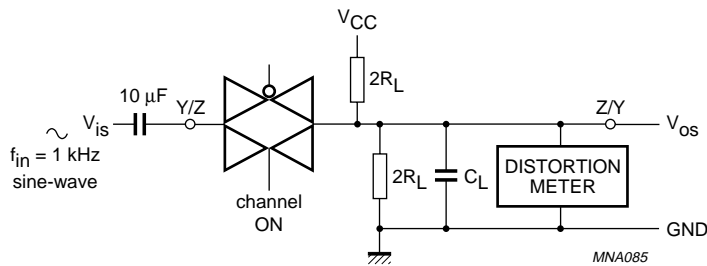


Fig.12 Test circuit for measuring sine-wave distortion.

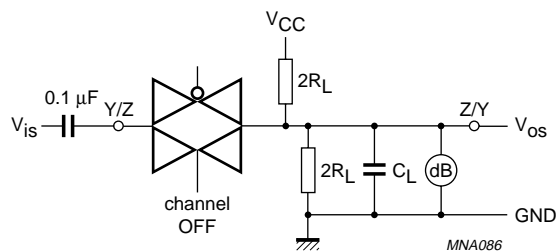
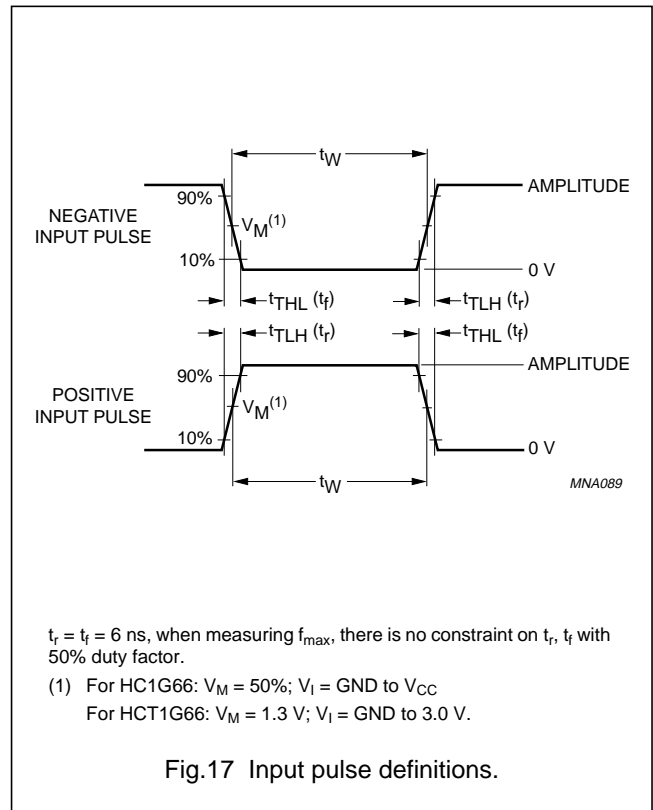
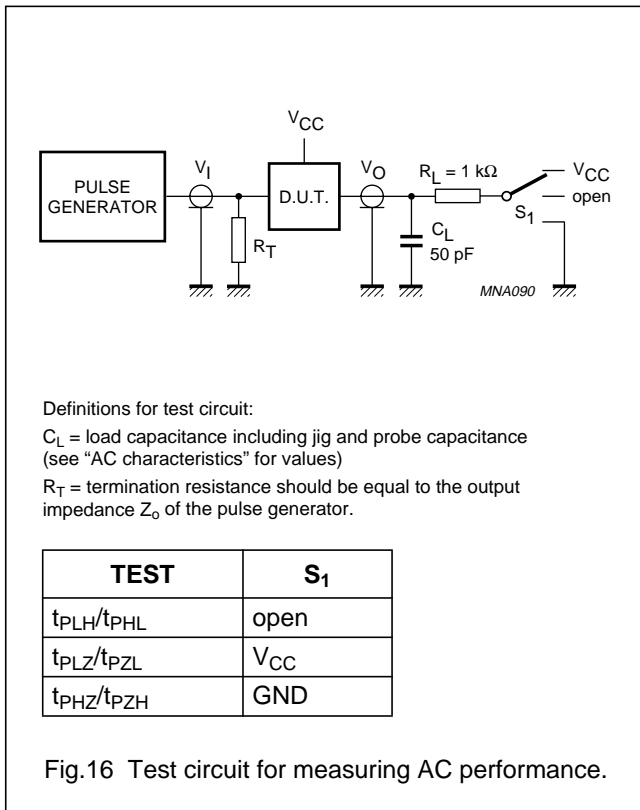
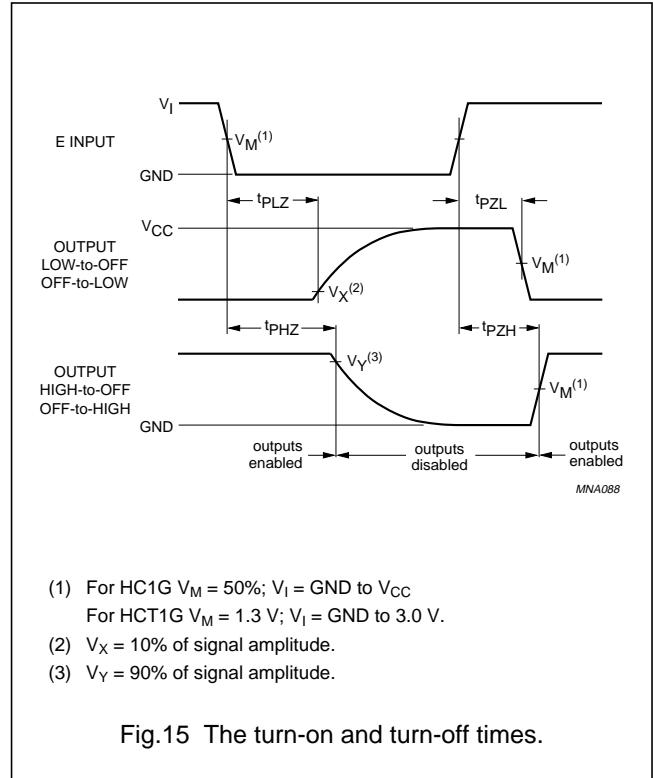
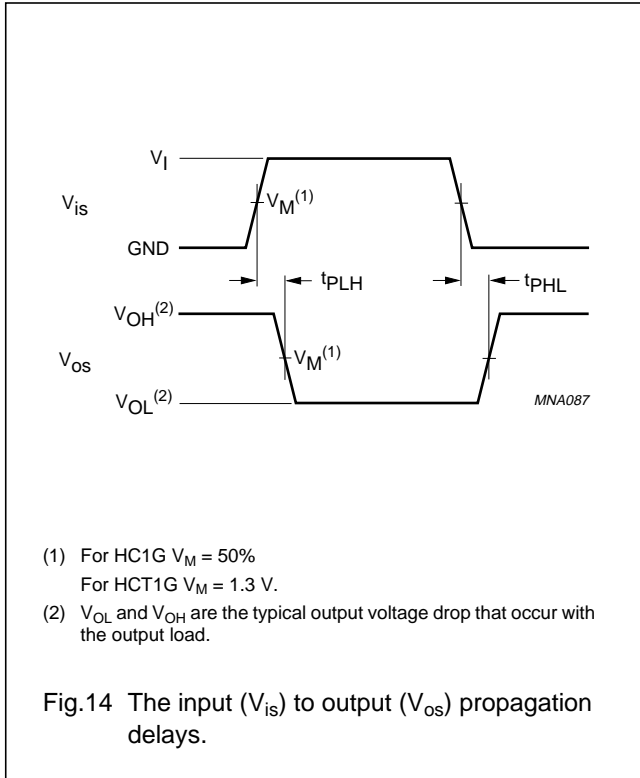


Fig.13 Test circuit for measuring switch OFF signal feed-through.

Bilateral switch

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AC WAVEFORMS



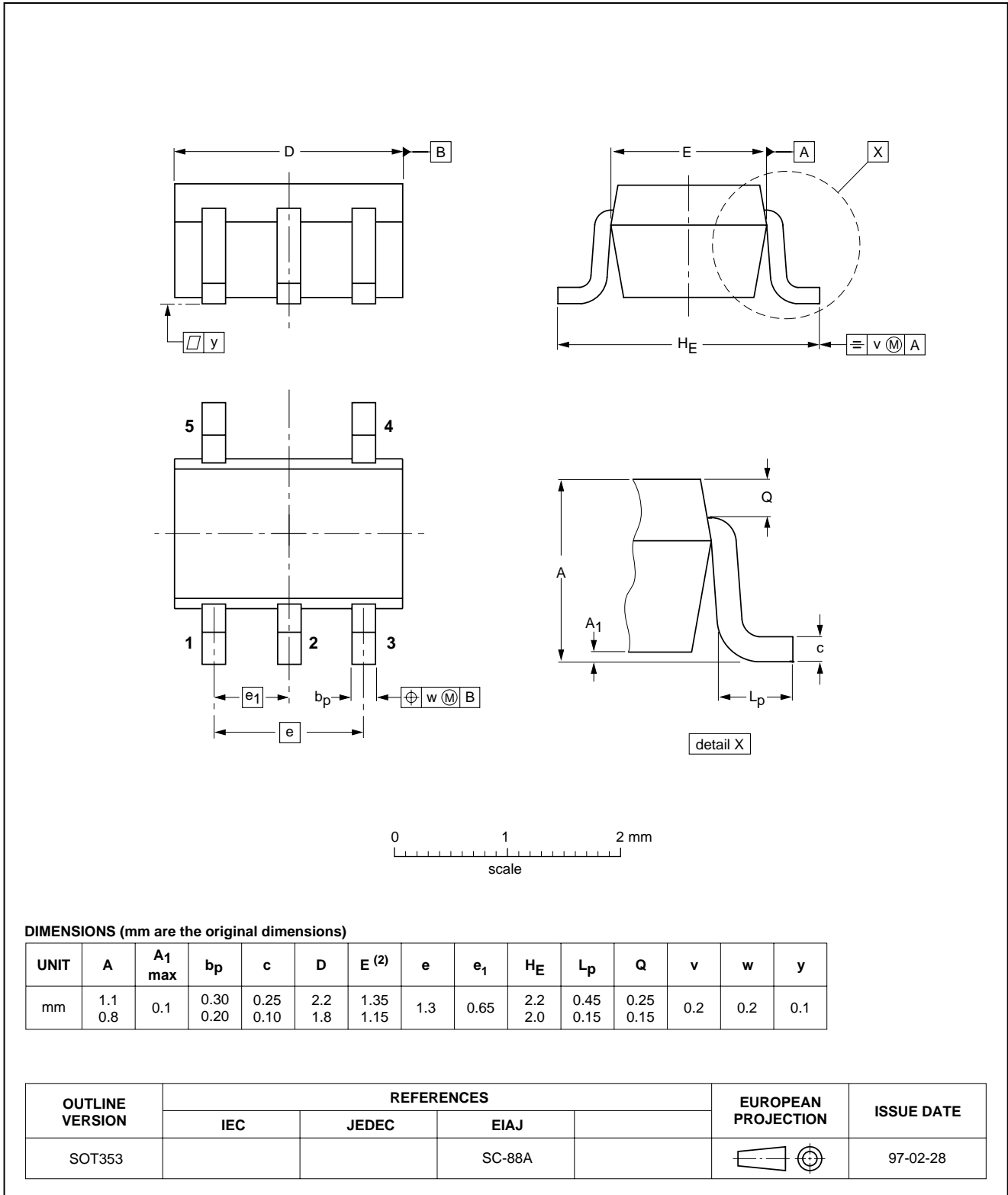
Bilateral switch

74HC1G66; 74HCT1G66

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353

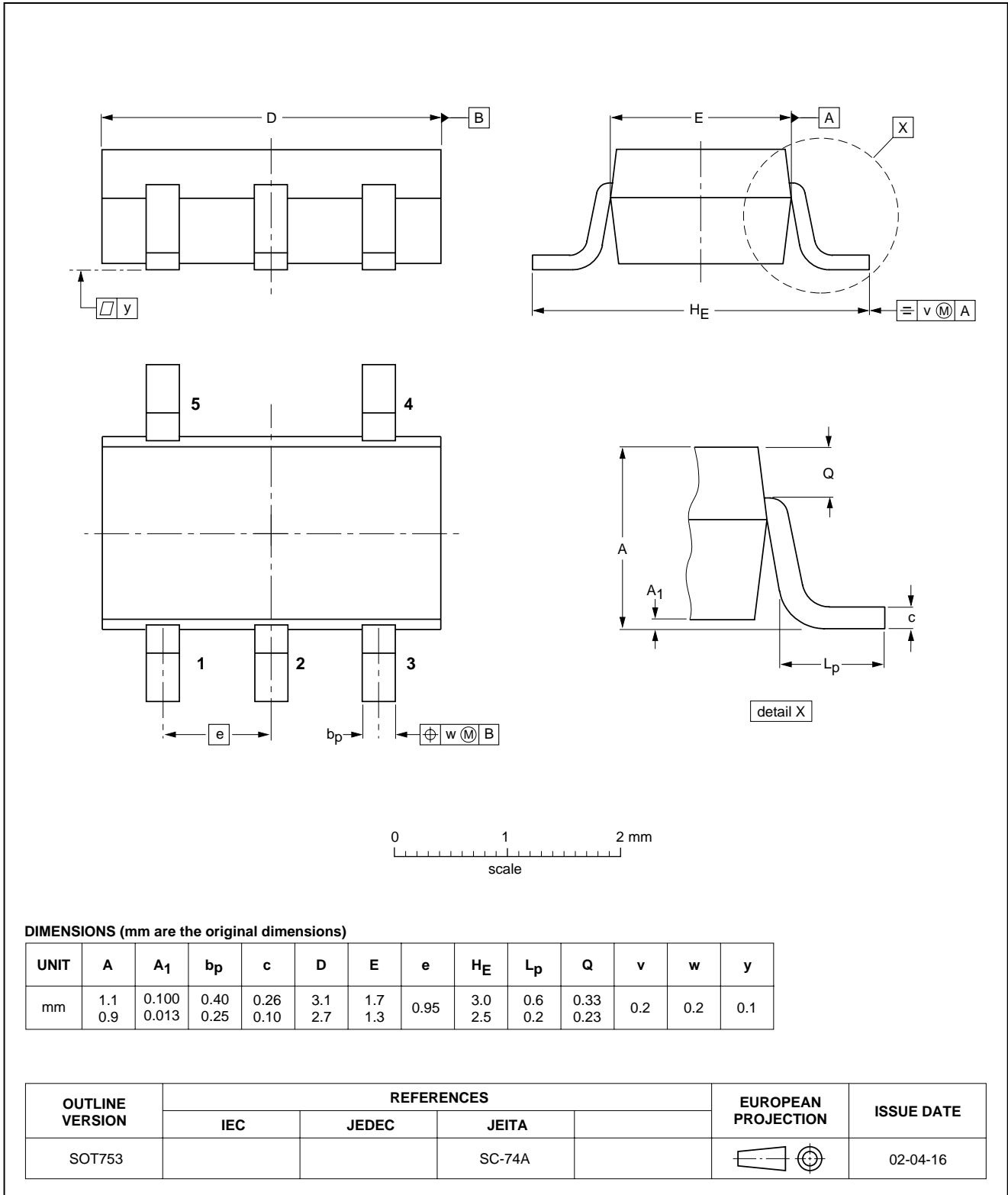


Bilateral switch

74HC1G66; 74HCT1G66

Plastic surface mounted package; 5 leads

SOT753



## Bilateral switch

## 74HC1G66; 74HCT1G66

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Bilateral switch

## 74HC1G66; 74HCT1G66

## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(3)</sup>	suitable
PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(6)</sup>	suitable

## Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## Bilateral switch

## 74HC1G66; 74HCT1G66

## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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## Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Bilateral switch

74HC1G66; 74HCT1G66

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**NOTES**

# ***Philips Semiconductors – a worldwide company***

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Printed in The Netherlands

613508/03/pp20

Date of release: 2002 May 15

Document order number: 9397 750 09723

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