

DATA SHEET

74HC1GU04 Inverter

Product specification
Supersedes data of 2002 May 13

2002 May 27

Inverter

74HC1GU04

FEATURES

- Wide operating voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard.

DESCRIPTION

The 74HC1GU04 is a high-speed Si-gate CMOS device. The 74HC1GU04 provides the inverting single stage function. The standard output currents are $\frac{1}{2}$ compared to the 74HCU04.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6.0\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A to Y	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	5	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance	notes 1 and 2	14	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

2. The condition is $V_I = \text{GND to } V_{CC}$.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	Y
L	H
H	L

Note

1. H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

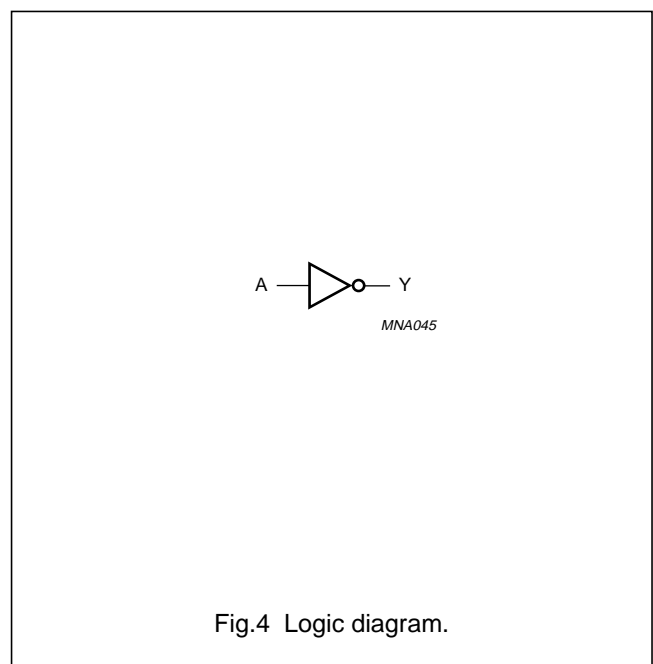
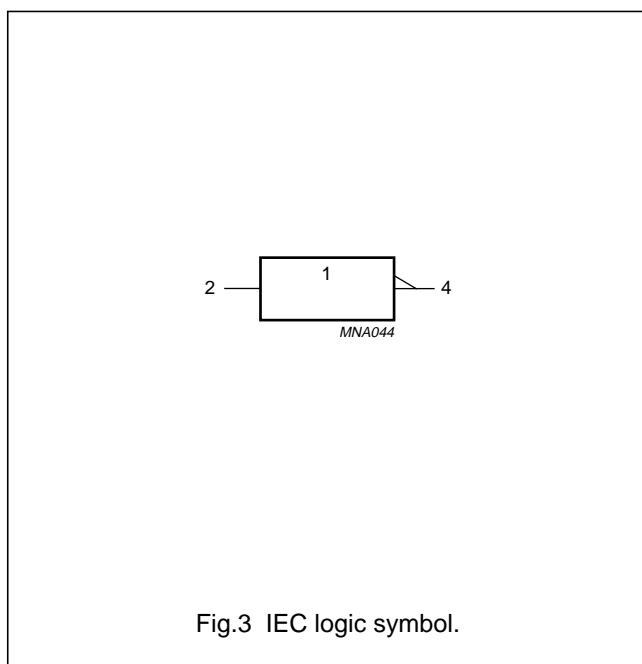
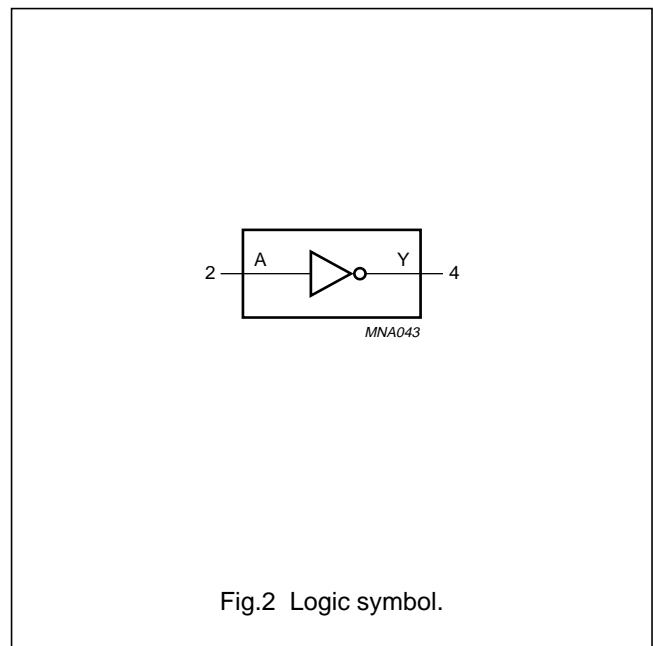
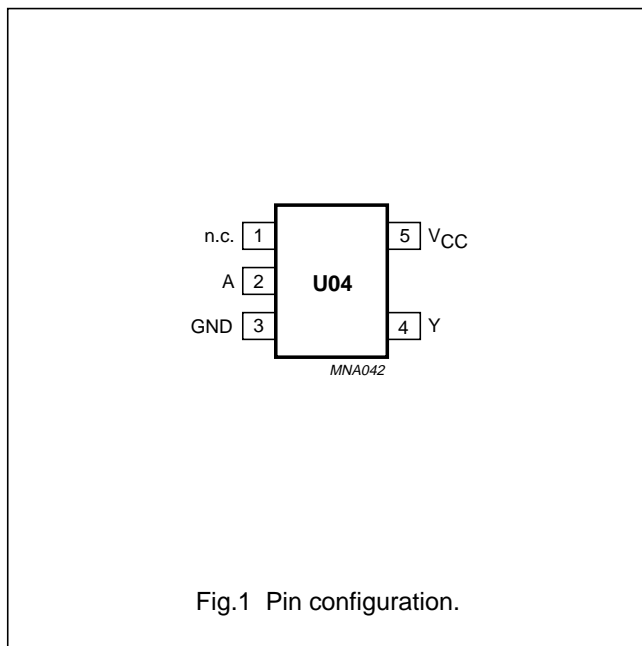
TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC1GU04GW	-40 to +125 $^{\circ}\text{C}$	5	SC-88A	plastic	SOT353	HD
74HC1GU04GV	-40 to +125 $^{\circ}\text{C}$	5	SC-74A	plastic	SOT753	HU4

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PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V _{CC}	supply voltage



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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC1G			UNIT
			MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	ns
		$V_{CC} = 4.5\text{ V}$	–	–	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$; note 1	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$; note 1	–	±20	mA
I_O	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$; note 1	–	±12.5	mA
I_{CC}	V_{CC} or GND current	note 1	–	±25	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C; note 2	–	200	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P_D derates linearly with 2.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)					UNIT
		OTHER	V _{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.	
V _{IH}	HIGH-level input voltage		2.0	1.7	1.4	–	1.7	–	V
			4.5	3.6	2.6	–	3.6	–	V
			6.0	4.8	3.4	–	4.8	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.6	0.3	–	0.3	V
			4.5	–	1.9	0.9	–	0.9	V
			6.0	–	2.6	1.2	–	1.2	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = –20 μA	2.0	1.8	2.0	–	1.8	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –20 μA	4.5	4.0	4.5	–	4.0	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –20 μA	6.0	5.5	6.0	–	5.5	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –2.0 mA	4.5	4.13	4.32	–	3.7	–	V
		V _I = V _{IH} or V _{IL} ; I _O = –2.6 mA	6.0	5.63	5.81	–	5.2	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; I _O = 20 μA	2.0	–	0	0.2	–	0.2	V
		V _I = V _{IH} or V _{IL} ; I _O = 20 μA	4.5	–	0	0.5	–	0.5	V
		V _I = V _{IH} or V _{IL} ; I _O = 20 μA	6.0	–	0	0.5	–	0.5	V
		V _I = V _{IH} or V _{IL} ; I _O = 2.0 mA	4.5	–	0.15	0.33	–	0.4	V
		V _I = V _{IH} or V _{IL} ; I _O = 2.6 mA	6.0	–	0.16	0.33	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	1.0	–	1.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	10	–	20	μA

Note1. All typical values are measured at T_{amb} = 25 °C.

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AC CHARACTERISTICS

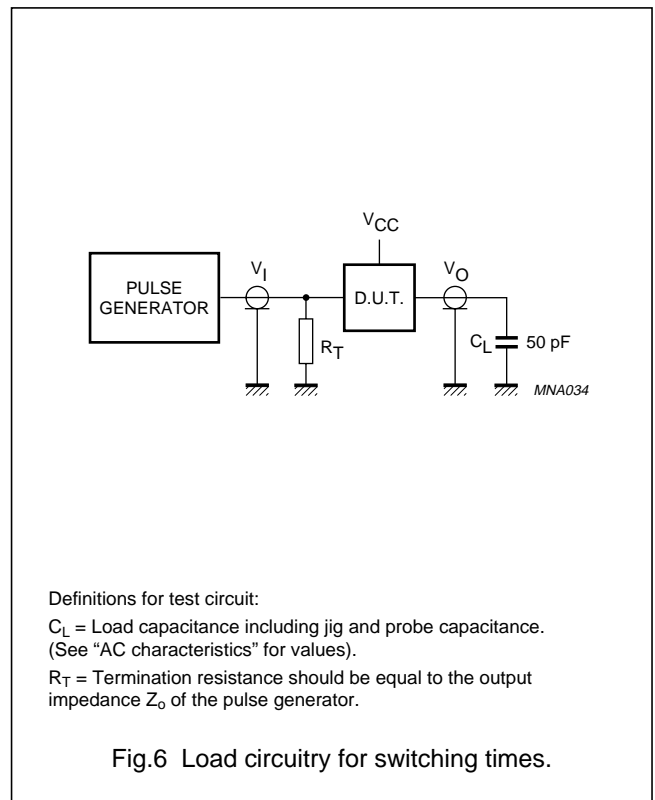
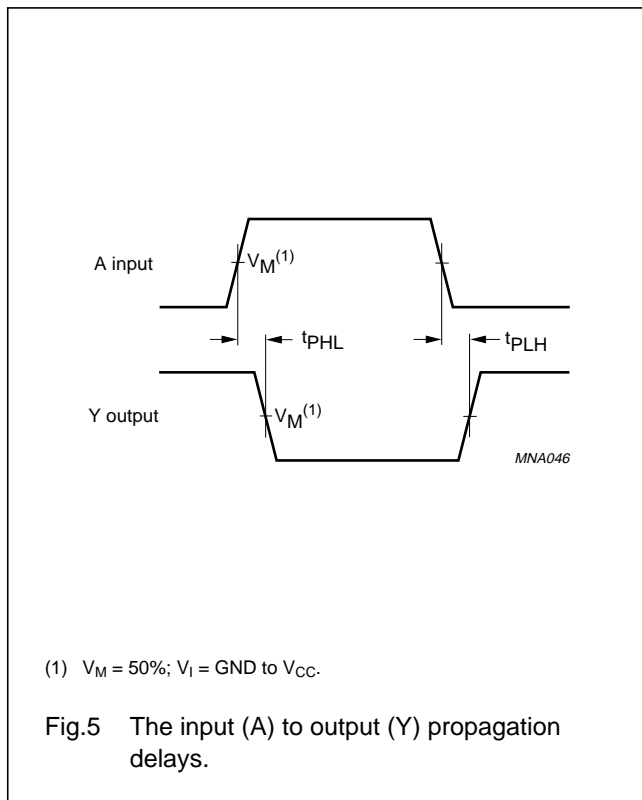
GND = 0 V; $t_r = t_f = 6.0$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} (°C)					UNIT	
			WAVEFORMS	V_{CC} (V)	-40 to +85		-40 to +125		
					MIN.	TYP. ⁽¹⁾	MAX.		MIN.
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	2.0	–	10	90	–	105	ns
			4.5	–	7	18	–	21	ns
			6.0	–	6	15	–	18	ns

Note

- All typical values are measured at $T_{amb} = 25$ °C.

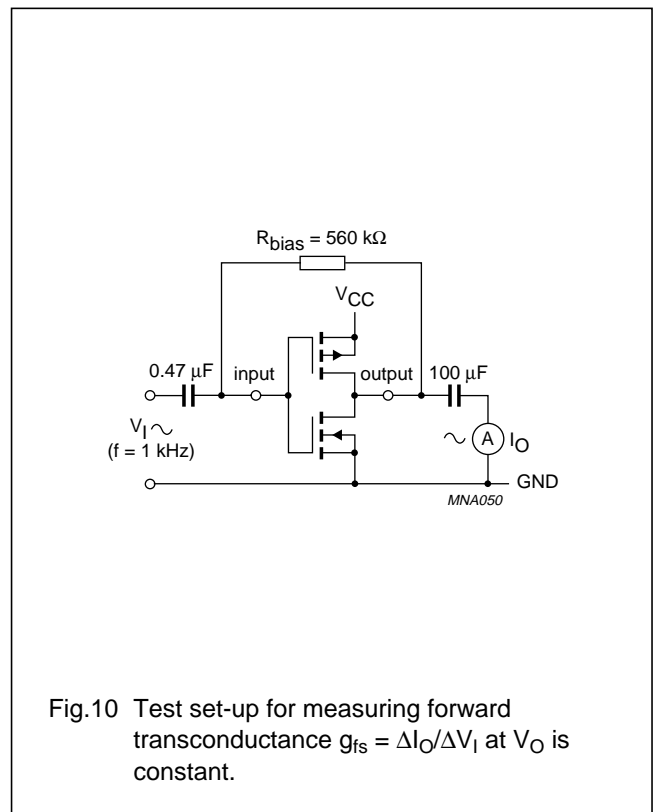
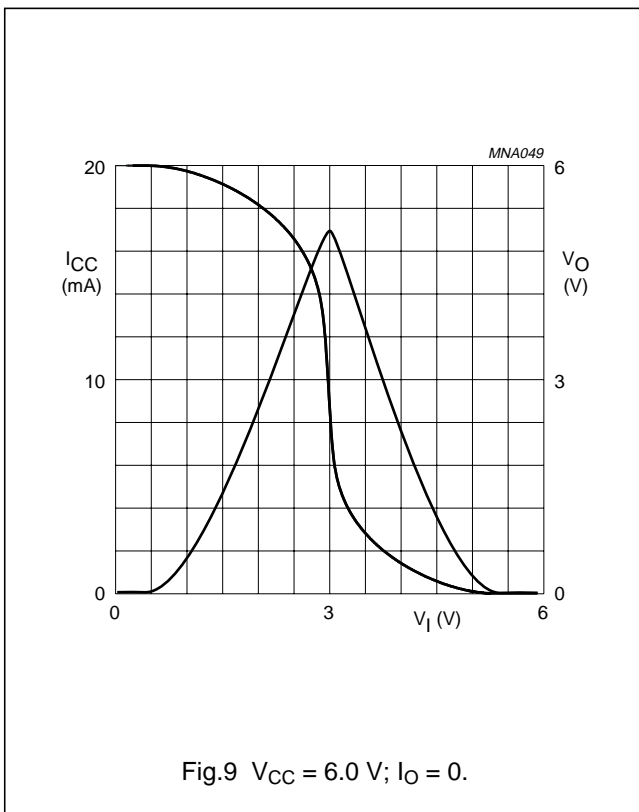
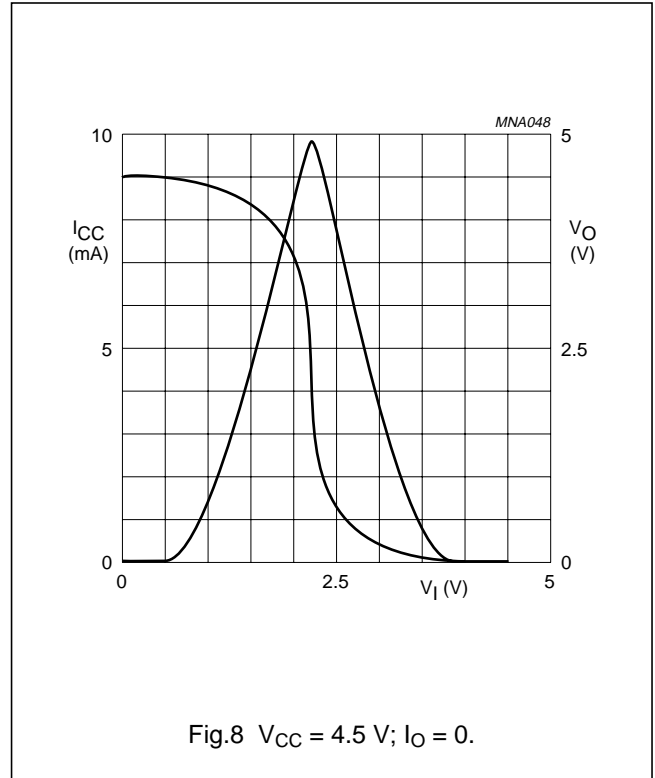
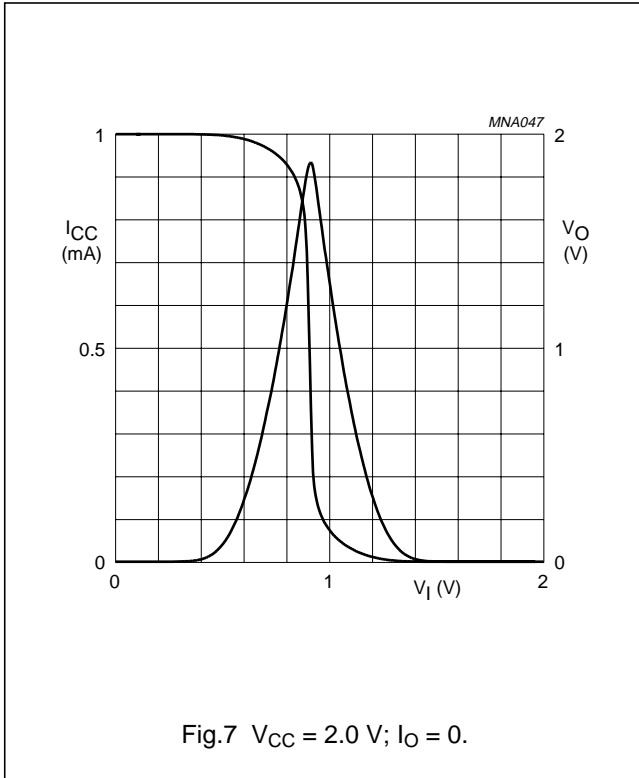
AC WAVEFORMS



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TYPICAL TRANSFER CHARACTERISTICS



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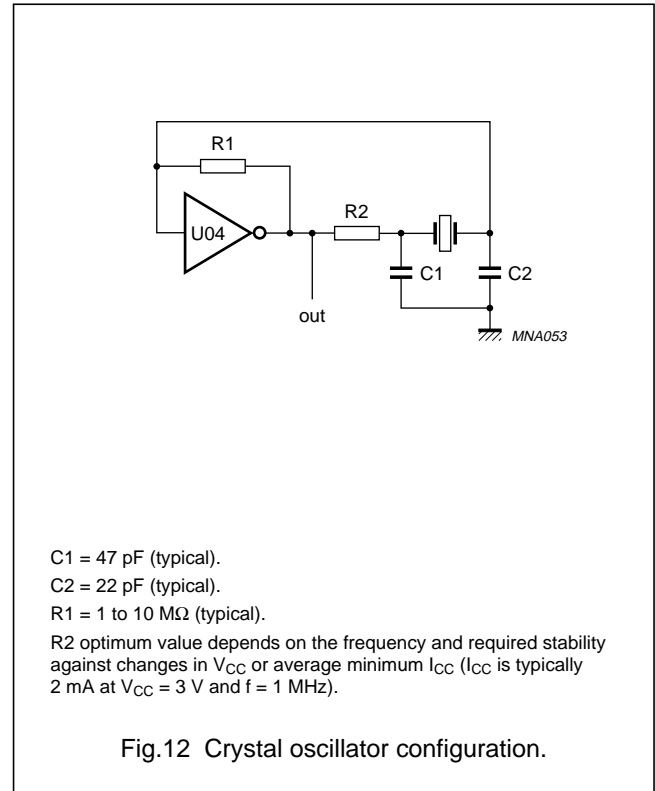
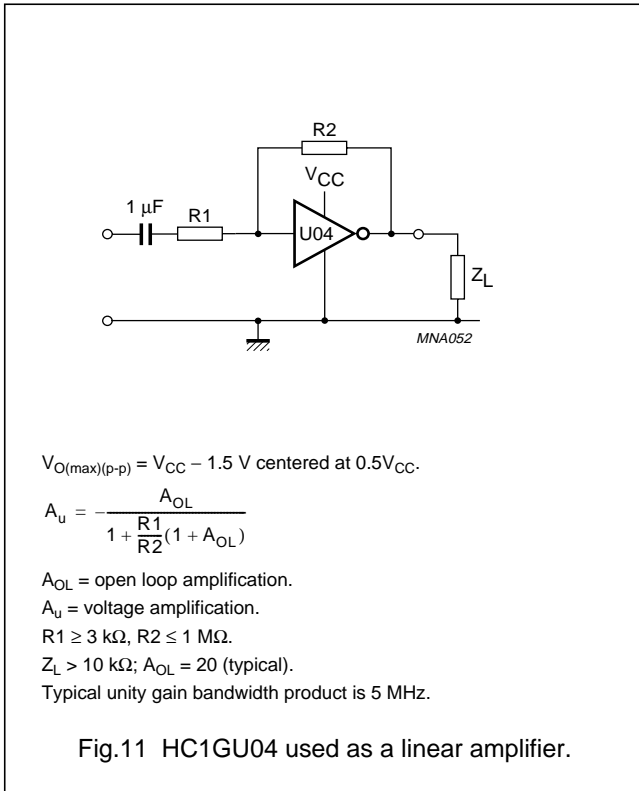
APPLICATION INFORMATION

Some applications are:

- Linear amplifier (see Fig.11)
- In crystal oscillator design (see Fig.12).

Note to the application information.

All values given are typical unless otherwise specified.



External components for resonator (f < 1 MHz)

FREQUENCY (kHz)	R1 (MΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)
10 to 15.9	2.2	220	56	20
16 to 24.9	2.2	220	56	10
25 to 54.9	2.2	100	56	10
55 to 129.9	2.2	100	47	5
130 to 199.9	2.2	47	47	5
200 to 349.9	2.2	47	47	5
350 to 600	2.2	47	47	5

Where:

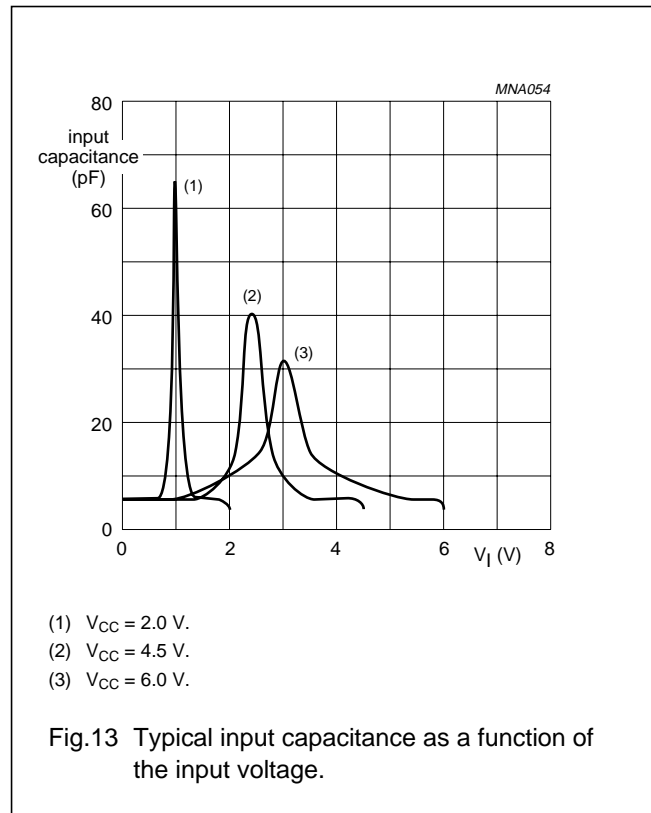
All values given are typical and must be used as an initial set-up.

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Optimum value for R2

FREQUENCY (MHz)	R2 (kΩ)	OPTIMUM FOR
3	2.0	minimum required I _{CC}
	8.0	minimum influence due to change in V _{CC}
6	1.0	minimum required I _{CC}
	4.7	minimum influence by V _{CC}
10	0.5	minimum required I _{CC}
	2.0	minimum influence by V _{CC}
14	0.5	minimum required I _{CC}
	1.0	minimum influence by V _{CC}
>14	–	replace R2 by C3 with a typical value of 35 pF



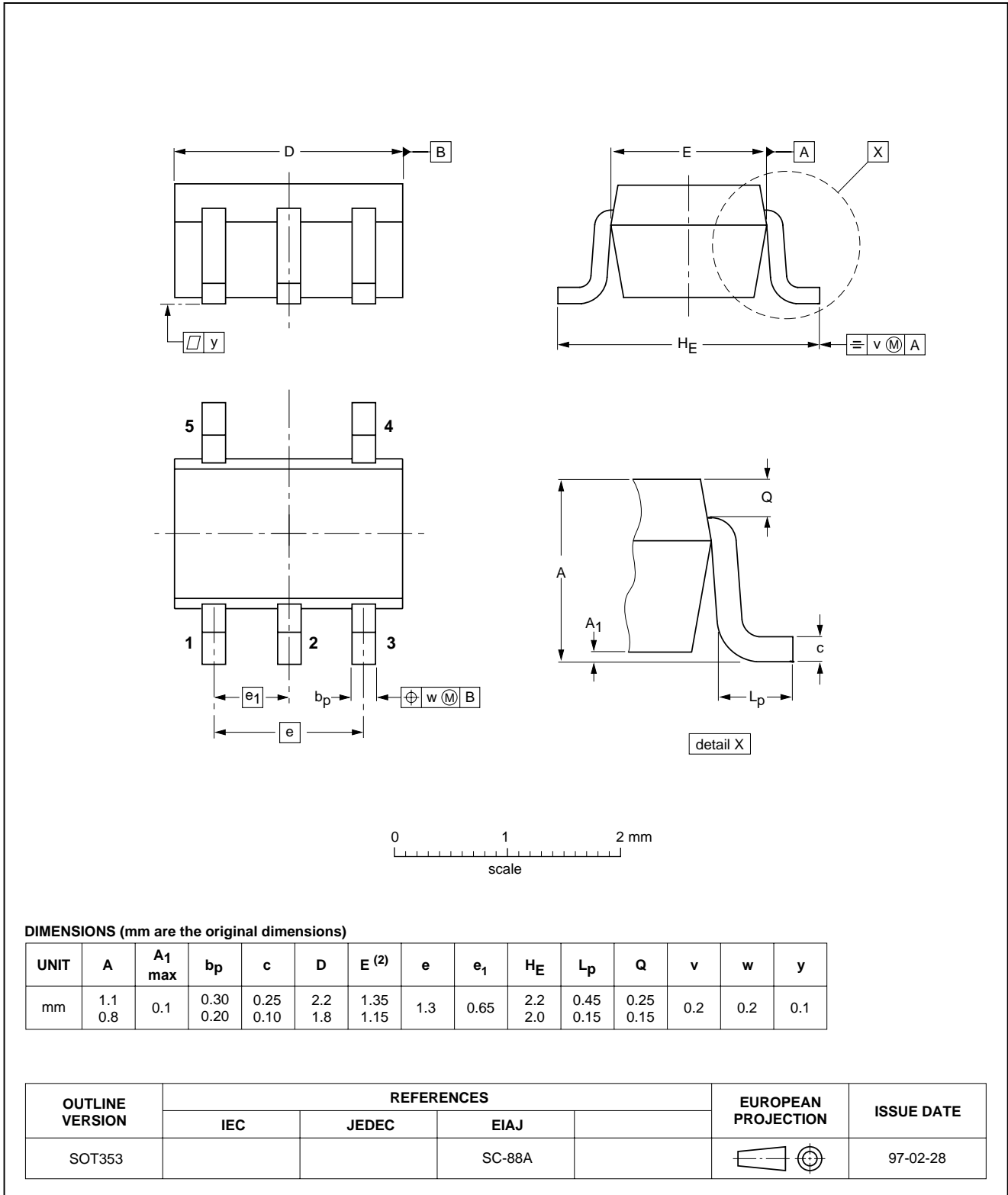
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PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353

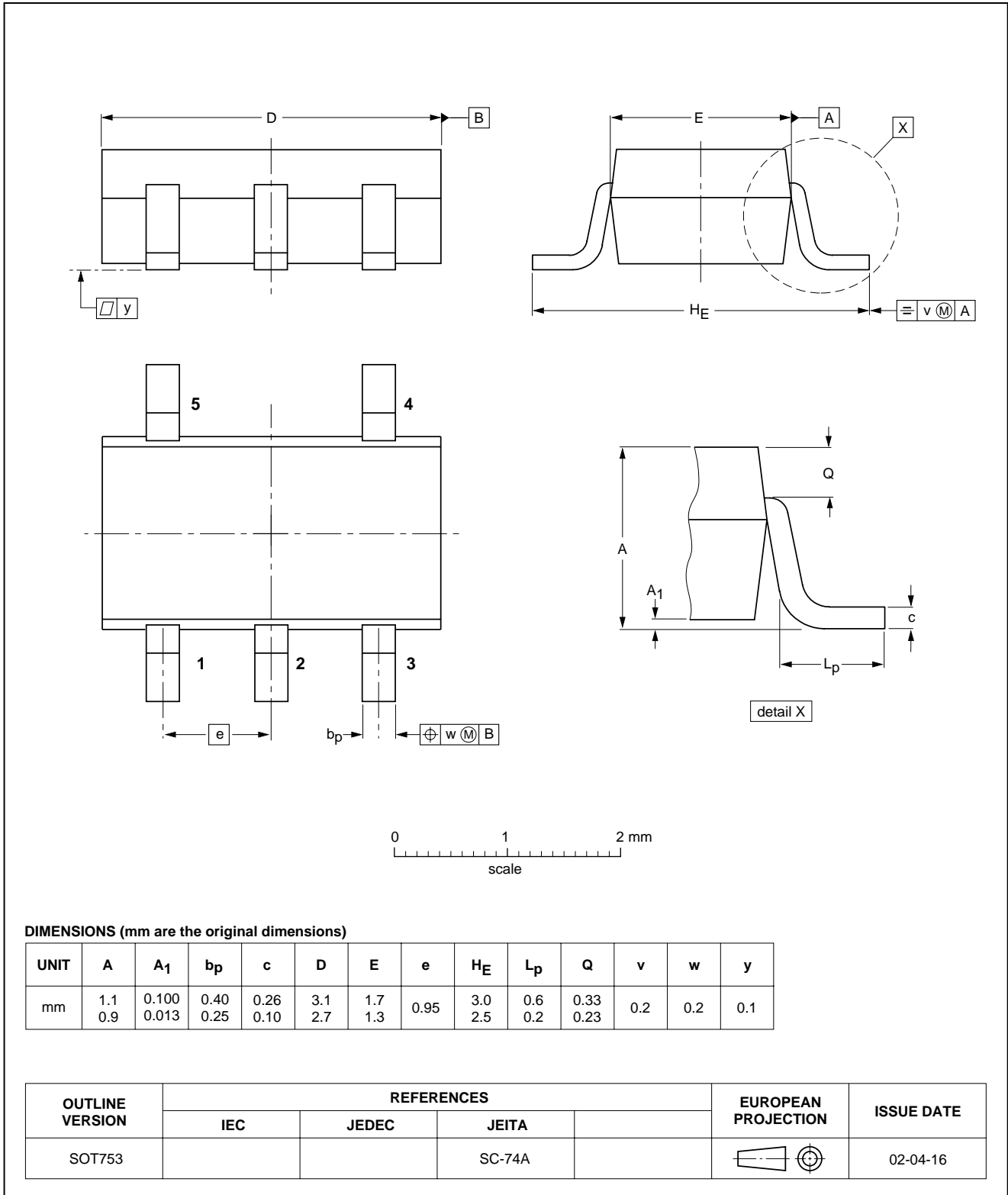


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Plastic surface mounted package; 5 leads

SOT753



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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable

Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Contact information

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