

74HC03; 74HCT03

Quad 2-input NAND gate

Rev. 3 — 27 June 2013

Product data sheet

1. General description

The 74HC03; 74HCT03 is a quad 2-input NAND gate with open-drain outputs. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Input levels:
 - ◆ For 74HC03: CMOS level
 - ◆ For 74HCT03: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

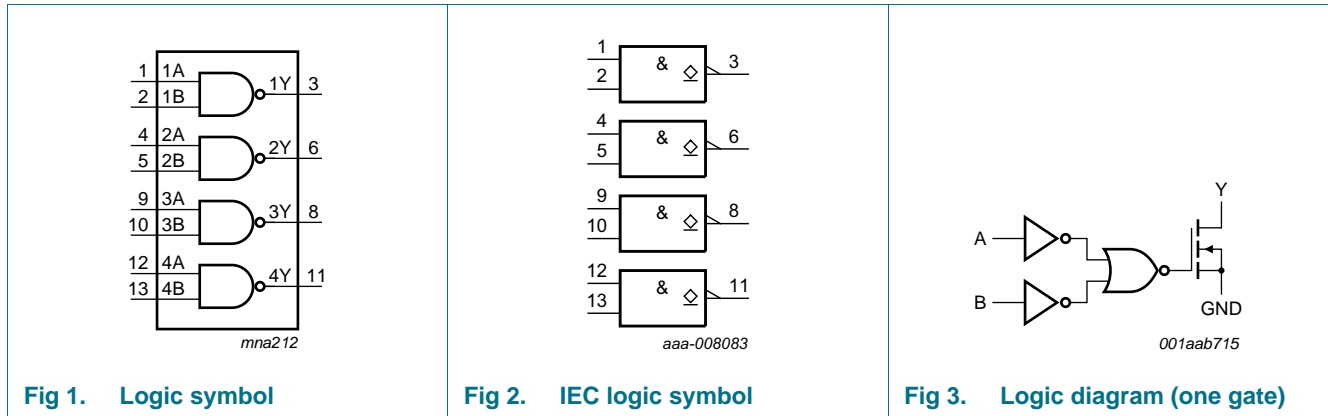
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC03N	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT03N				
74HC03D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT03D				
74HC03DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT03DB				
74HC03PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT03PW				

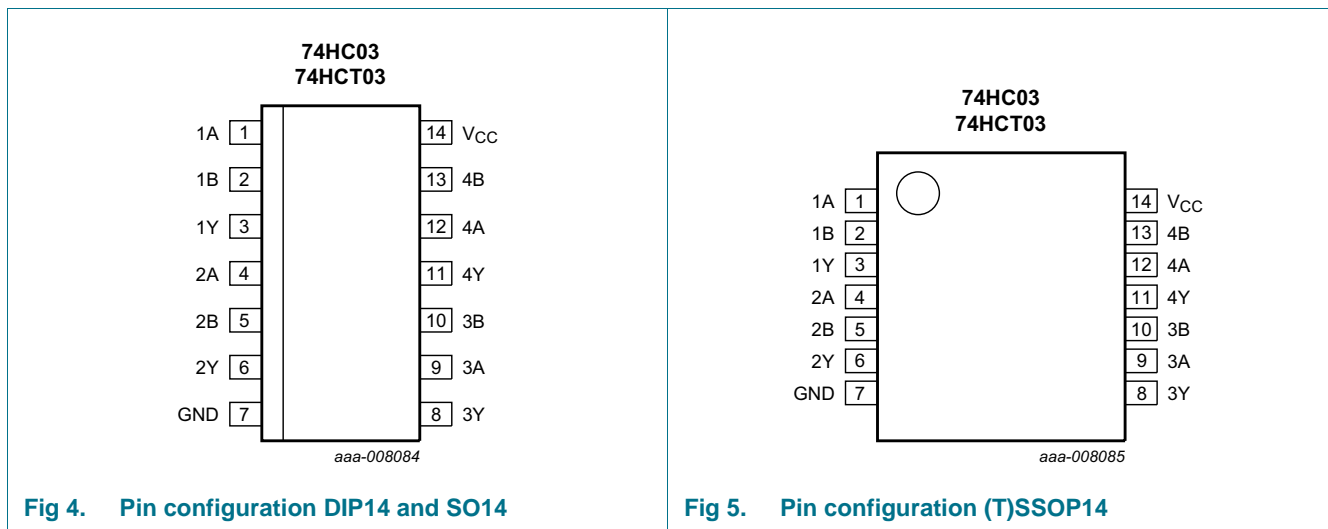


4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
V_O	output voltage		[1] -0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1] -	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$	[1] -	-20	mA
I_O	output current	$-0.5\text{ V} < V_O$	-	-25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14 and (T)SSOP14 packages		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC03			74HCT03			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

Table 5. Recommended operating conditions ...continued
Voltages are referenced to GND (ground = 0 V) ...continued

Symbol	Parameter	Conditions	74HC03			74HCT03			Unit
			Min	Typ	Max	Min	Typ	Max	
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC03										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\ \mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
	$I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	0.1	-	-	± 1	-	± 1	μA
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{IL}$; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; $V_{CC} = 6.0\text{ V}$; $I_O = 0\text{ A}$	-	-	± 0.5	-	± 5.0	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$	-	2.0	-	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT03										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5\text{ V}$								
		$I_O = 20\ \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$	-	0.15	0.26	-	0.33	-	0.4	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I _{OZ}	OFF-state output current	per input pin; V _I = V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V	-	100	360	-	450	-	490	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for load circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	

74HC03

t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V _{CC} = 2.0 V	-	28	95	120	145	ns	
		V _{CC} = 4.5 V	-	10	19	24	29	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	-	8	-	-	-	ns	
t _t	transition time	see Figure 6	[2]						
		V _{CC} = 2.0 V	-	19	75	95	110	ns	
		V _{CC} = 4.5 V	-	7	15	19	22	ns	
		V _{CC} = 6.0 V	-	6	13	16	19	ns	
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	[3]	-	4	-	-	-	pF

Table 7. Dynamic characteristics ...continued
 GND = 0 V; C_L = 50 pF; for load circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
74HCT03									
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V _{CC} = 4.5 V	-	12	24	30	36	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	-	10	-	-	-	ns	
t _t	transition time	V _{CC} = 4.5 V; see Figure 6	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} - 1.5 V	[3]	-	4	-	-	-	pF

- [1] t_{pd} is the same as t_{PLZ} and t_{PZL}.
- [2] t_t is the same as t_{THL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

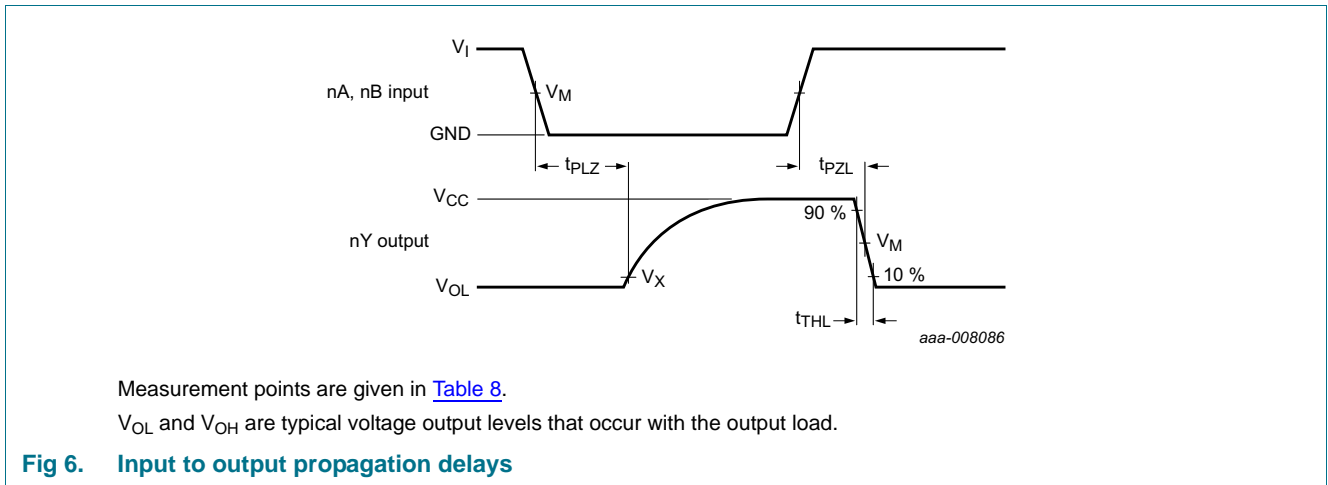


Table 8. Measurement points

Type	Input		Output	
	V _M	V _X	V _M	V _X
74HC03	0.5V _{CC}	0.1V _{CC}	0.5V _{CC}	0.1V _{CC}
74HCT03	1.3 V	0.1V _{CC}	1.3 V	0.1V _{CC}

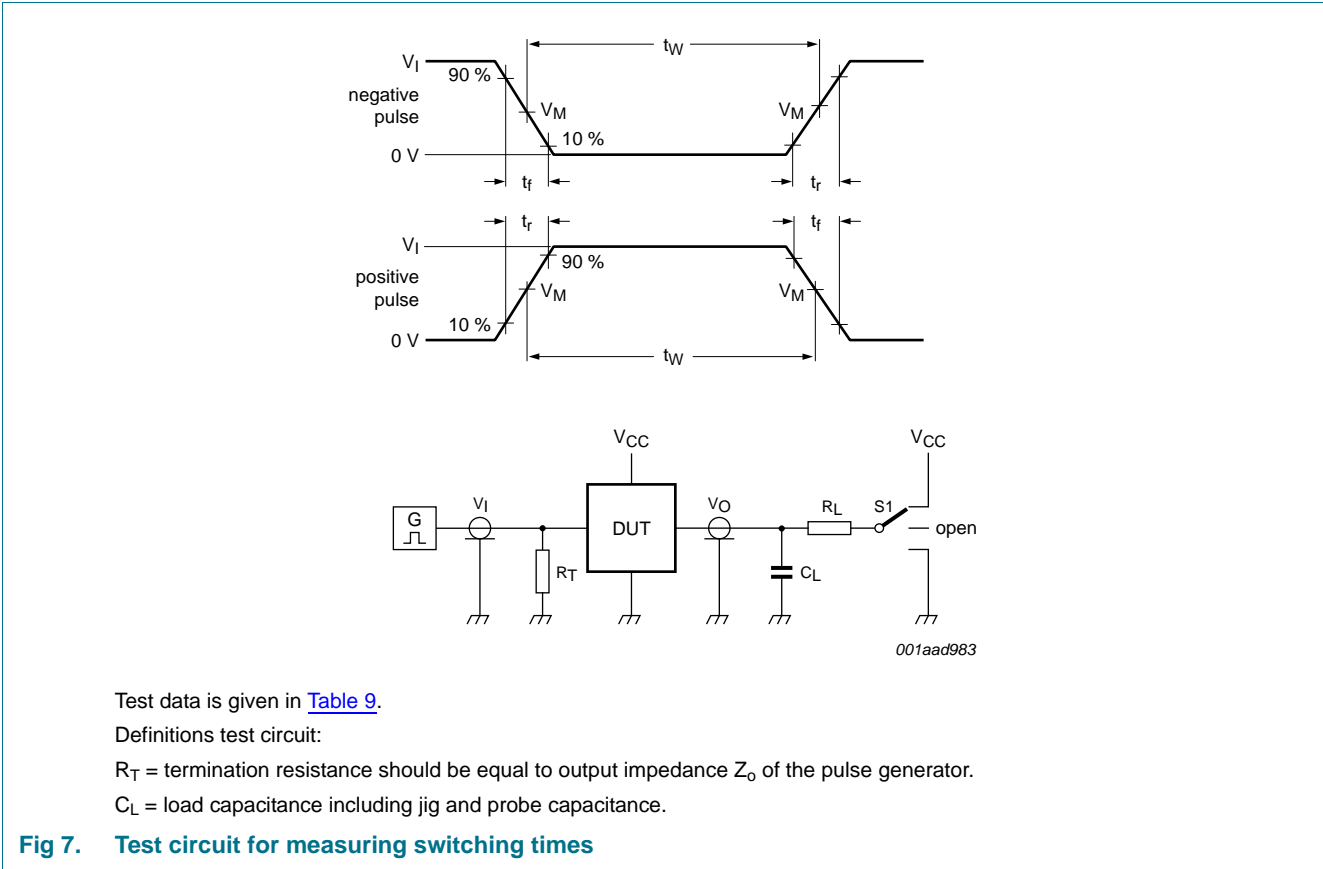


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
74HC03	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	V_{CC}
74HCT03	3.0 V	6 ns	15 pF, 50 pF	1 k Ω	V_{CC}

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

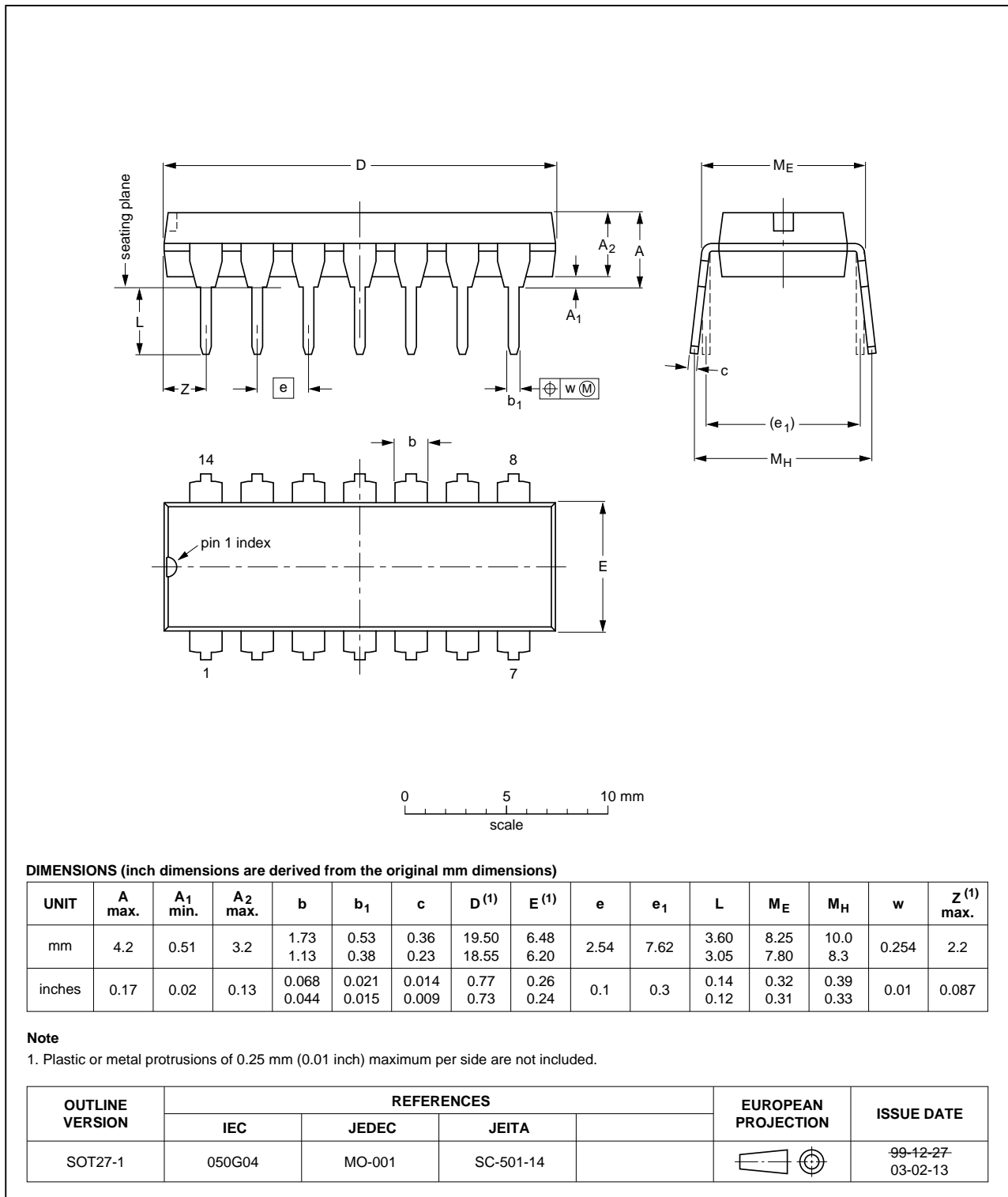


Fig 8. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

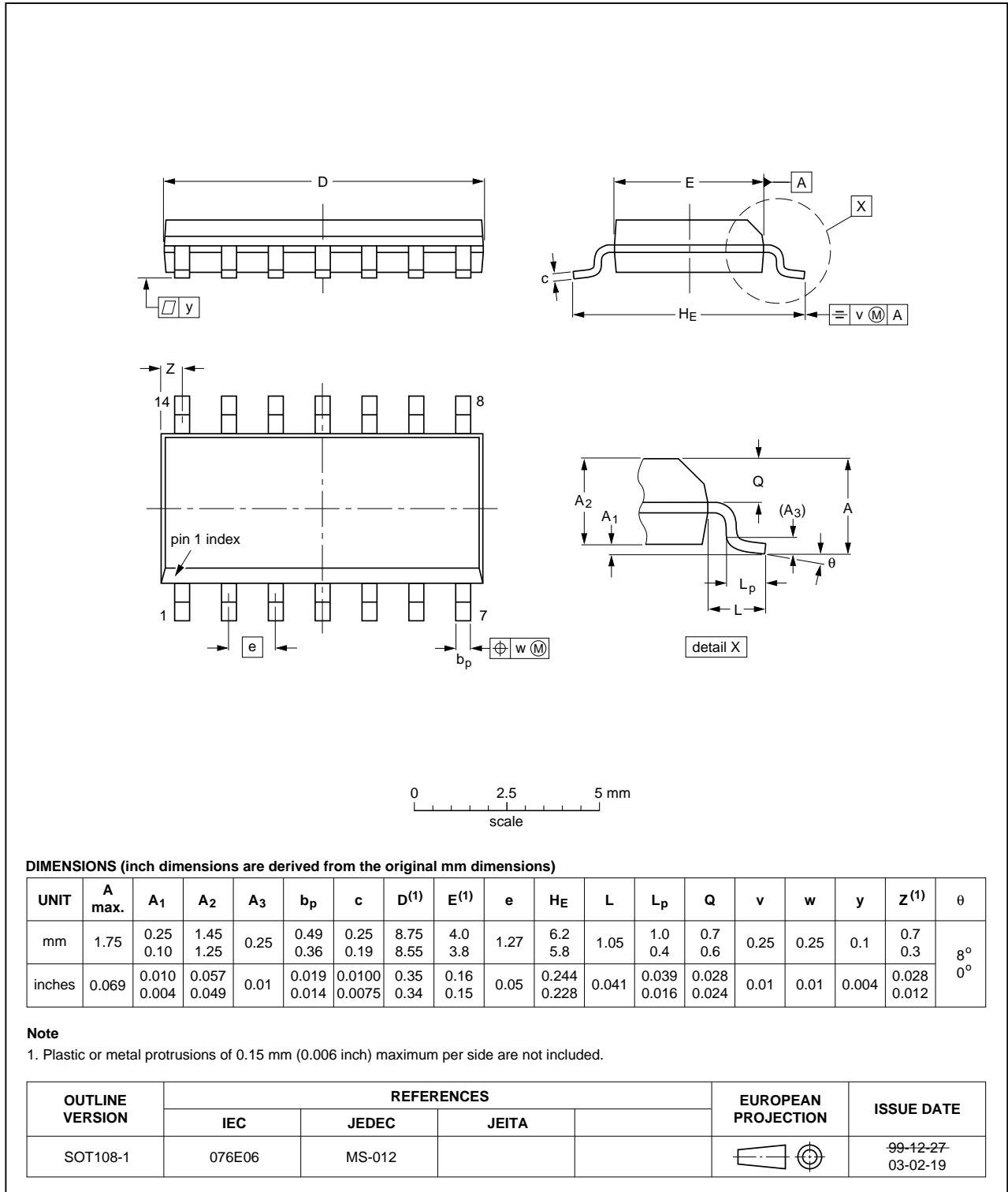


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

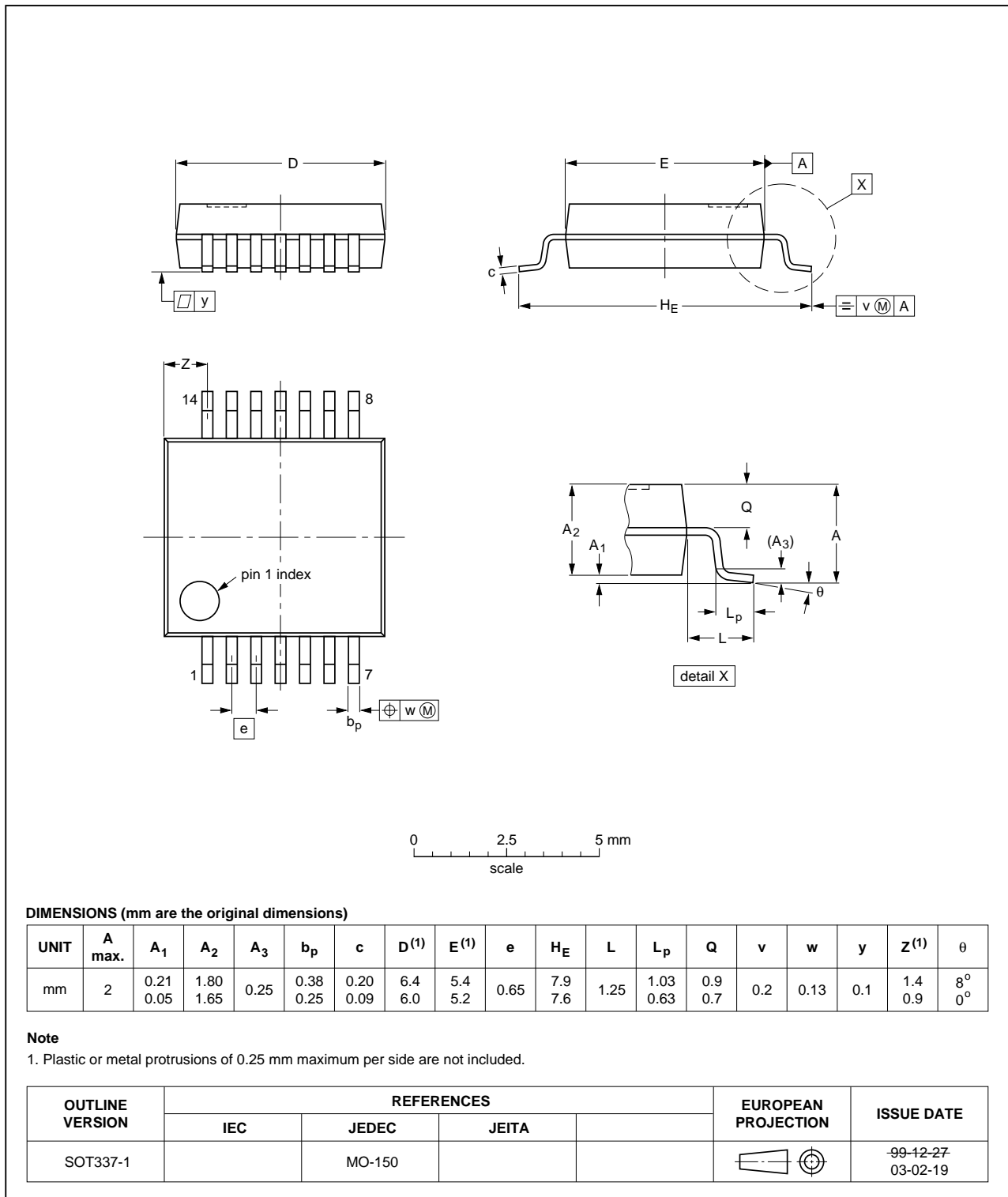


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

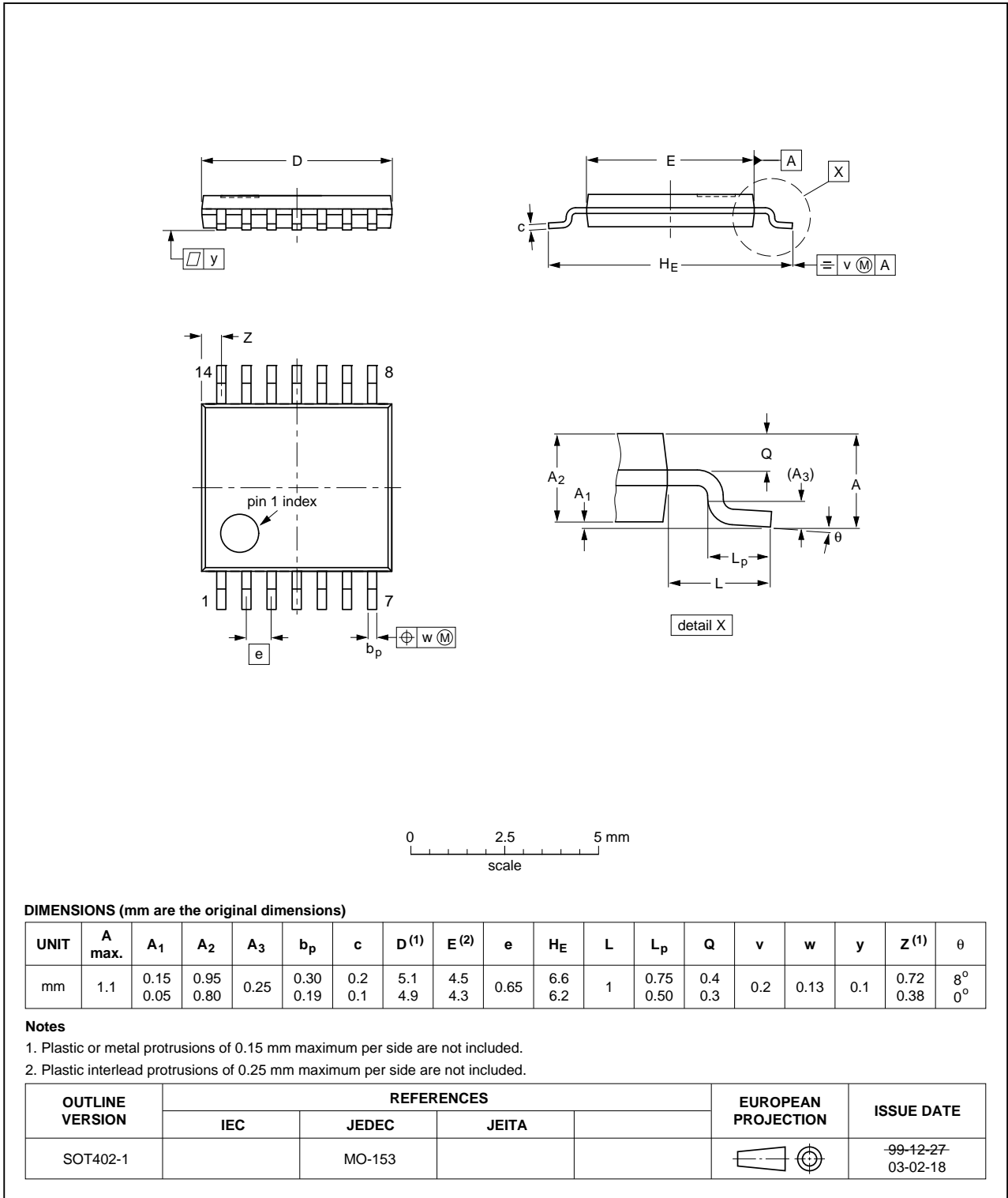


Fig 11. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT03 v.3	20130627	Product data sheet	-	74HC_HCT03_CNV v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT03_CNV v.2	19970827	Product specification	-	-

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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