

Octal latched bidirectional Futurebus transceivers (3-State + open-collector)

74F8960/74F8961

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE futurebus standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/down operation

DESCRIPTION

The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

Incident switching is employed, therefore BTL propagation delays are short. Although the

voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8960 and 74F8961 A ports have TTL 3-state drivers and TTL receivers with a latch function. A separate High-level control input (VX) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, VX is simply tied to VCC.

The 74F8961 is the non-inverting version of 74F8960.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F8960	6.5ns	80mA
74F8961	6.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
28-pin plastic DIP (300 mil) ¹	N74F8960N, N748961N
28-pin PLCC ¹	N74F8960A, N74F8961A

NOTE: Thermal mounting techniques are recommended.

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	PNP latched inputs	3.5/0.117	70μA/70μA
B0 – B8	Data inputs with threshold circuitry	5.0/0.167	100μA/100μA
OEA	A output enable input (active high)	1.0/0.033	20μA/20μA
$\overline{OEB0}$, $\overline{OEB1}$	B output enable inputs (active low)	1.0/0.033	20μA/20μA
\overline{LE}	Latch enable input (active low)	1.0/0.033	20μA/20μA
A0 – A7	3-state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

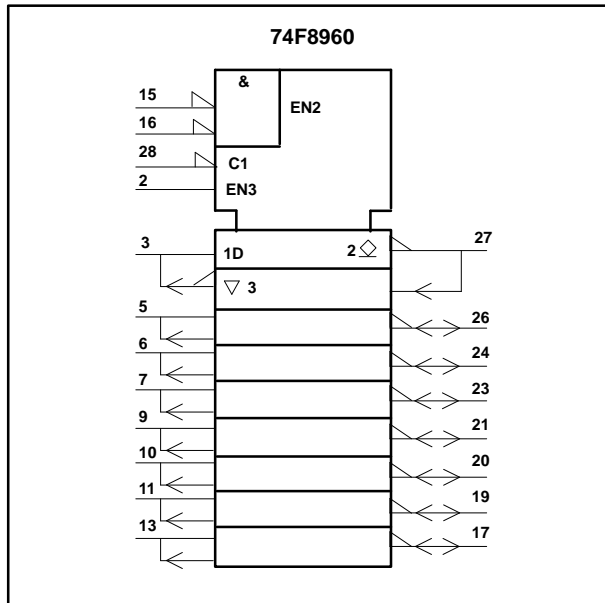
NOTES:

1. One (1.0) FAST unit load is defined as: 20μA in the high state and 0.6mA in the low state.
2. OC = Open collector.

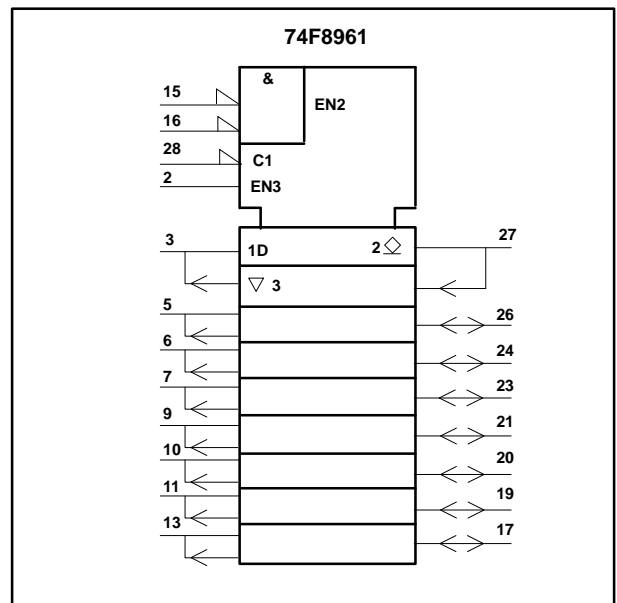
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IEC/IEEE SYMBOL FOR 74F8960



IEC/IEEE SYMBOL FOR 74F8961



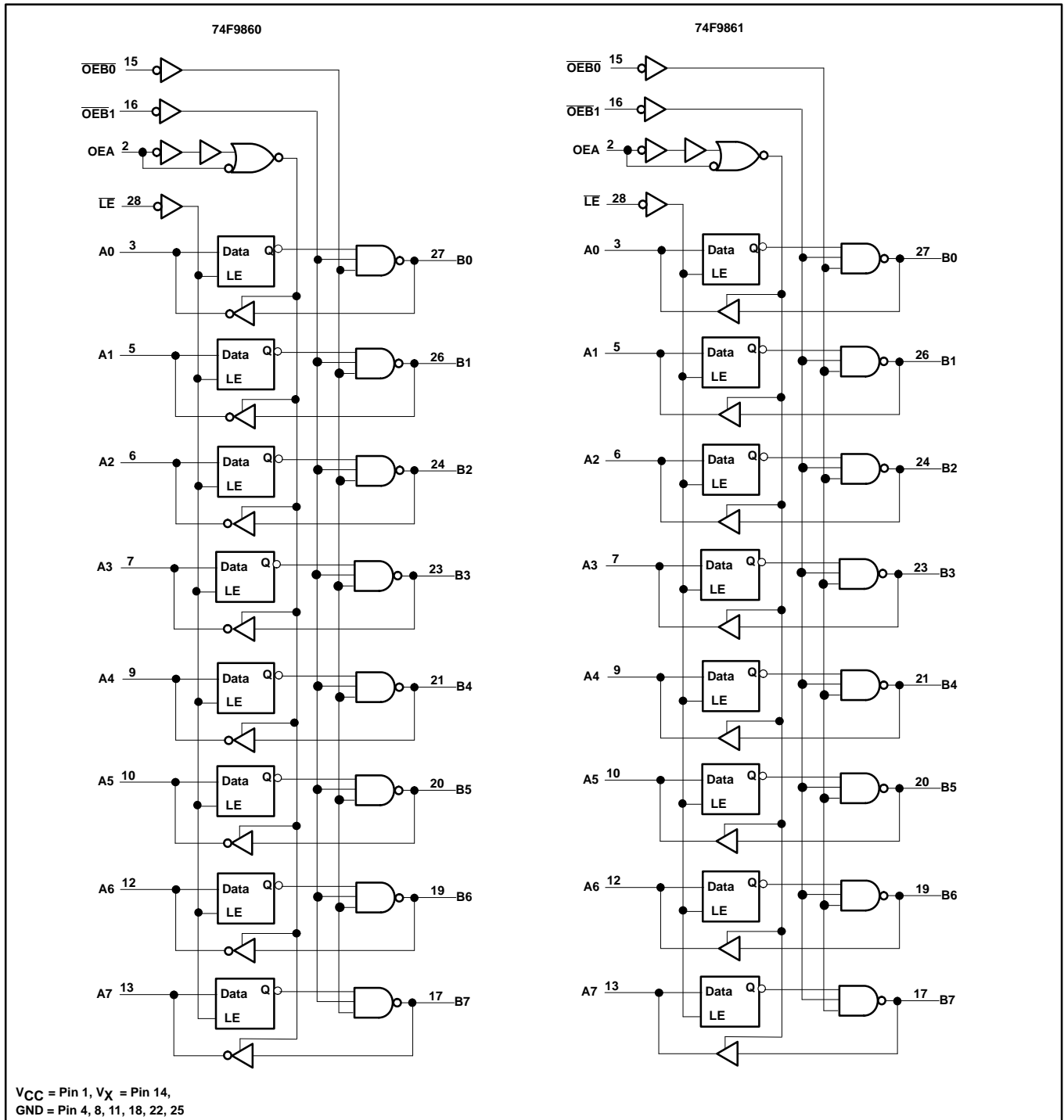
PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V_X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{OE}B0$	15	Input	Enables the B outputs when both pins are low
$\overline{OE}B1$	16	Input	Enables the A outputs when high
\overline{LE}	28	Input	Latched when high (a special feature is built in for proper enabling times)
V_X	14	Input	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

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LOGIC DIAGRAM



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FUNCTION TABLE FOR 74F8960

INPUTS						LATCH STATE	OUTPUTS		OPERATING MODE
An	Bn*	LE	OEA	OEB ₀	OEB ₁		An	Bn	
H	X	L	L	L	L	H	Z	L	A 3-state, data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Qn	Z	\bar{Q}_n	A 3-state, latched data to B
-	-	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
-	L	H	H	L	L	H (2)	L	Z(2)	
-	-	H	H	L	L	Qn	\bar{Q}_n	\bar{Q}_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
-	H	L	H	H	X	H	H	Z	B 3-state, data from B to A
-	L	L	H	H	H	L	L	Z	
-	H	H	H	H	H	Qn	H	Z	
-	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
-	H	L	H	X	H	H	H	Z	B 3-state, data from B to A
-	L	L	H	X	H	L	L	Z	
-	H	H	H	X	H	Qn	H	Z	
-	L	H	H	X	H	Qn	L	Z	

NOTES:

1. H = High-voltage level
2. L = Low-voltage level
3. X = Don't care
4. - = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or low voltage level one setup time prior to the low-to-high $\bar{L}\bar{E}$ transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconditioned such that B inputs may assume a high or low level while $\bar{O}E\bar{B}_0$ and $\bar{O}E\bar{B}_1$ are low and $\bar{L}\bar{E}$ is high.
9. H** = Goes to level of pullup voltage.
10. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

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FUNCTION TABLE FOR 74F8961

INPUTS						LATCH STATE	OUTPUTS		OPERATING MODE
An	Bn*	LE	OEA	OEB ₀	OEB ₁		An	Bn	
H	X	L	L	L	L	H	Z	H**	A 3-state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3-state, latched data to B
-	-	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
-	L	H	H	L	L	H (2)	L	Z(2)	
-	-	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
-	H	L	H	H	X	H	H	Z	B 3-state, data from B to A
-	L	L	H	H	H	L	L	Z	
-	H	H	H	H	H	Qn	H	Z	
-	L	H	H	H	H	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
-	H	L	H	X	H	H	H	Z	B 3-state, data from B to A
-	L	L	H	X	H	L	L	Z	
-	H	H	H	X	H	Qn	H	Z	
-	L	H	H	X	H	Qn	L	Z	

NOTES:

1. H = High-voltage level
2. L = Low-voltage level
3. X = Don't care
4. - = Input not externally driven
5. Z = High impedance (off) state
6. Q_n = High or low-voltage level one setup time prior to the low-to-high LE transition.
7. (1) = Condition will cause a feedback loop path: A to B and B to A.
8. (2) = The latch must be preconditioned such that B inputs may assume a high or low level while OEB₀ and OEB₁ are low and LE is high.
9. H** = Goes to level of pullup voltage.
10. B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _X	Threshold control		-0.5 to +7.0	V
V _{IN}	Input voltage	OE \bar{B} , OEA, LE	-0.5 to +7.0	V
		A0 – A7, B0 – B7	-0.5 to +5.5	V
I _{IN}	Input current		-40 to +5	mA
V _{OUT}	Voltage applied to output in high output state		-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T _{amb}	Operating free air temperature range		0 to +70	°C
T _{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	High-level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V _{IL}	Low-level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.475	V
I _{Ik}	Input clamp current	Except A0 – A7			-18	mA
		A0 – A7			-40	mA
I _{OH}	High-level output current	A0 – A7			-3	mA
I _{OL}	Low-level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T _{amb}	Operating free air temperature		0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST	LIMITS			UNIT	
				MIN.	TYP. ²	MAX.		
I_{OH}	High-level output current	B0 – B7	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
I_{OFF}	Power-off output current	B0 – B7	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
V_{OH}	High-level output voltage	A0 – A7 ⁴	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}, V_X = V_{CC}$	2.5		V_{CC}	V
				$I_{OH} = -4\text{mA},$ $V_X = 3.13\text{V and } 3.47\text{V}$	2.5			V
V_{OL}	Low-level output voltage	A0 – A7 ⁴	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}$	$I_{OL} = 20\text{mA}, V_X = V_{CC}$			0.50	V
		B0 – B7 ⁸	$V_{IH} = \text{MIN}$	$I_{OL} = 100\text{mA}$			1.15	V
					$I_{OL} = 4\text{mA}$	0.40		
V_{IK}	Input clamp voltage	A0 – A7	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.5	V	
		Except A0 – A7	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.2	V	
I_I	Input current at maximum input voltage	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA	
		A0–A7, B0 – B7	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1	mA	
I_{IH}	High-level input current	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
		B0–B7	$V_{CC} = \text{MAX}, V_I = 2.1\text{V}, B_n - A_n = 0\text{V}$			100	μA	
I_{IL}	Low-level input current	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-20	μA	
		B0 – B7	$V_{CC} = \text{MAX}, V_I = 0.3\text{V}$			-100	μA	
$I_{OZH} + I_{IH}$	Off-state output current, high-level current applied	A0 – A7	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$			70	μA	
$I_{OZL} + I_{IL}$	Off-state output current, low-level voltage applied	A0 – A7	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-70	μA	
I_X	High-level control current		$V_{CC} = \text{MAX}, V_X = V_{CC}, \overline{LE} = OEA = \overline{OE}B_n = 2.7\text{V}, A0 - A7 = 2.7\text{V}, B0 - B7 = 2.0\text{V},$	-100		100	μA	
			$V_{CC} = \text{MAX}, V_X = 3.13 \text{ \& } 3.47\text{V}, \overline{LE} = OEA = \overline{OE}B_n = A0 - A7 = 2.7\text{V}, B0 - B7 = 2.0\text{V},$	-10		10	μA	
I_{OS}	Short circuit output current ³	A0–A7	$V_{CC} = \text{MAX}, B_n = 1.3\text{V}, OEA = 2.0\text{V}, \overline{OE}B_n = 2.7\text{V}$	-60		-150	mA	
		only						$V_{CC} = \text{MAX}, B_n = 1.8\text{V}, OEA = 2.0\text{V}, \overline{OE}B_n = 2.7\text{V}$
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		65	100	mA	
		I_{CCL}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		100	145	mA	
		I_{CCZ}			75	100	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Due to test equipment limitations, actual test conditions are for $V_{IH} = 1.8\text{V}$ and $V_{IL} = 1.3\text{V}$.

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(3-State + open-collector)

74F8960/74F8961

AC ELECTRICAL CHARACTERISTICS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50p, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay B _n to A _n	Waveform 1, 2	4.5 6.0	6.0 10.0	8.5 13.5	3.5 7.5	9.5 14.5	ns
t _{PZH} t _{PZL}	Output enable time to high or low, OEA to A _n	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.5	15.0 16.0	ns
t _{PHZ} t _{PLZ}	Output enable time from high or low, OEA to A _n	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _D = 50pF, R _U = 9Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _D = 50pF, R _L = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n	Waveform 1, 2	3.5 3.5	5.5 5.0	8.0 8.0	2.0 3.0	9.5 9.0	ns
t _{PLH} t _{PHL}	Propagation delay LE to B _n	Waveform 1, 2	3.5 4.0	5.5 6.5	8.5 9.0	2.5 3.0	9.5 10.5	ns
t _{PLH} t _{PHL}	Output enable/disable time OE _{Bn} to B _n	Waveform 1, 2	2.5 3.5	4.5 5.5	7.5 8.5	1.5 3.5	8.0 9.0	ns
t _{TLH} t _{THL}	Transition time, B _n port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 6.0	ns

AC SETUP REQUIREMENTS FOR 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{SU(H)} t _{SU(L)}	Setup time, high or low A _n to LE	Waveform 3	5.0 3.0			5.0 5.0		ns
t _{H(H)} t _{H(L)}	Hold time, high or low A _n to LE	Waveform 3	0.0 0.0			0.0 0.0		ns
t _{W(L)}	LE pulse width, low	Waveform 3	4.5			5.0		ns

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AC ELECTRICAL CHARACTERISTICS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50p, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay B _n to A _n	Waveform 1, 2	5.5 4.5	8.0 6.0	12.0 9.0	5.5 4.5	12.0 9.0	ns
t _{PZH} t _{PZL}	Output enable time to high or low, OEA to A _n	Waveform 4 Waveform 5	8.0 8.5	10.5 11.0	13.5 13.5	7.5 8.0	15.0 15.5	ns
t _{PHZ} t _{PLZ}	Output enable time from high or low, OEA to A _n	Waveform 4 Waveform 5	2.0 2.0	3.5 4.5	6.0 7.0	1.5 2.0	6.5 7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _D = 50pF, R _U = 9Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _D = 50pF, R _U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay A _n to B _n	Waveform 1, 2	3.0 3.0	5.0 4.5	7.0 7.5	2.5 2.5	8.0 8.5	ns
t _{PLH} t _{PHL}	Propagation delay LE to B _n	Waveform 1, 2	3.5 3.5	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t _{PLH} t _{PHL}	Output enable/disable time OE _{Bn} to B _n	Waveform 1, 2	3.0 3.5	4.5 5.5	7.0 9.0	2.5 3.5	8.0 10.0	ns
t _{TLH} t _{THL}	Transition time, B _n port 1.3V to 1.7V, 1.7V to 1.3V	Test circuit and waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	5.0 4.5	ns

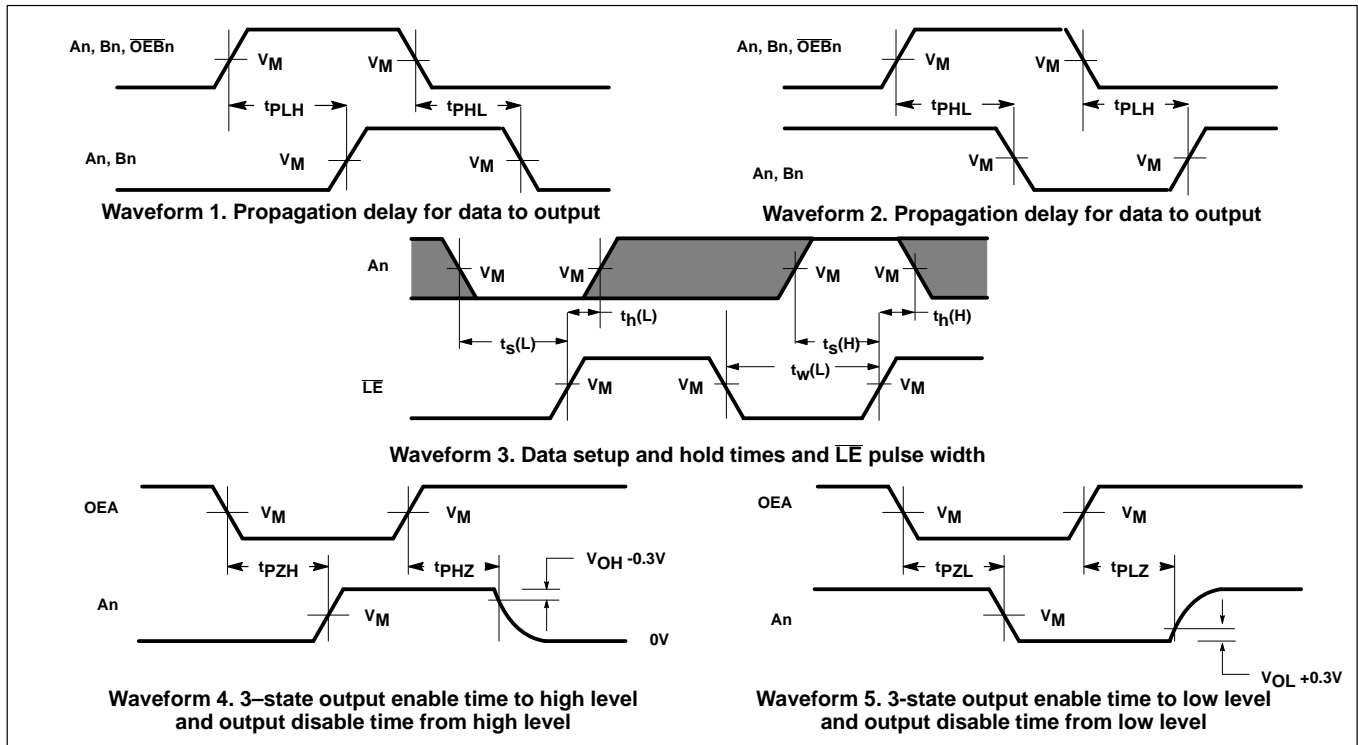
AC SETUP REQUIREMENTS FOR 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{SU(H)} t _{SU(L)}	Setup time, high or low A _n to LE	Waveform 3	3.5 4.5			4.5 5.0		ns
t _{H(H)} t _{H(L)}	Hold time, high or low A _n to LE	Waveform 3	0.0 0.0			0.0 0.0		ns
t _{W(L)}	LE pulse width, low	Waveform 3	4.0			5.0		ns

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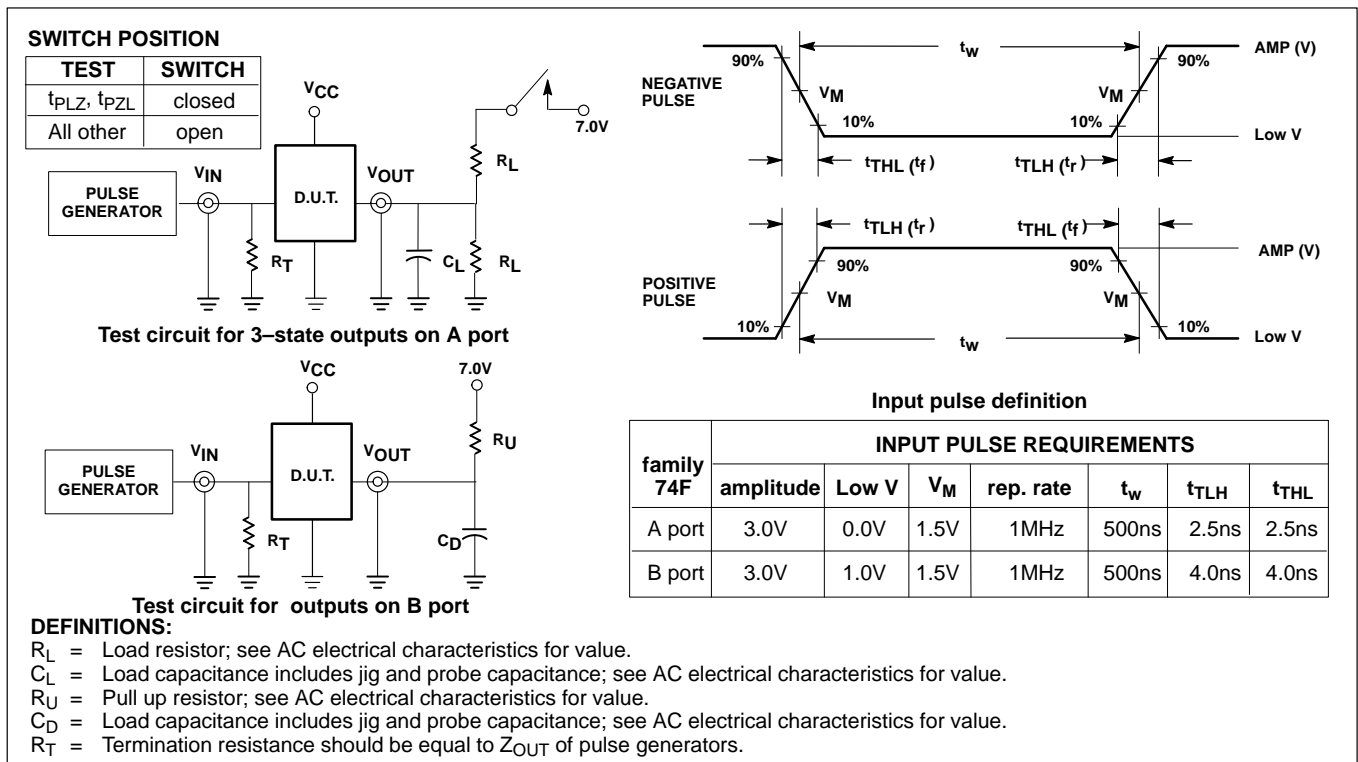
AC WAVEFORMS



NOTES:

1. For all waveforms, $V_M = 1.5V$.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS





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