

DATA SHEET

74F821/822/823/824/825/826

Bus interface registers

Product specification

1996 Jan 05

IC15 Data Handbook

Bus interface registers

74F821/822/823/824/825/826

74F821 10-bit bus interface register, non-inverting (3-State)
 74F822 10-bit bus interface register, inverting (3-State)
 74F823 9-bit bus interface register, non-inverting (3-State)
 74F824 9-bit bus interface register, inverting (3-State)
 74F825 8-bit bus interface register, non-inverting (3-State)
 74F826 8-bit bus interface register, inverting (3-State)

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- High performance bus interface buffering for wide data/address paths or busses carrying parity
- High impedance PNP base inputs for reduced loading (20µA in high and low states)
- I_{IL} is 20µA vs 1000µA for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessor
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821-29826 series
- Outputs sink 64mA and source 24mA
- Industrial temperature range available (−40°C to +85°C) for 74F823

DESCRIPTION

The 74F821 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 74F821/74F822 are buffered 10-bit wide versions of the popular 74F374/74F534 functions.

The 74F822 is the inverted output version of 74F821.

The 74F823 and 74F824 are 9-bit wide buffered registers with clock enable ($\overline{CE}$) and master reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The 74F824 is the inverted version of 74F823.

The 74F825 and 74F826 are 8-bit buffered registers with all the 74F823/74F824 controls plus output enable ($\overline{OE0}$, $\overline{OE1}$, $\overline{OE2}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/ $\overline{WR}$. They are ideal for uses as an output port requiring high I_{OL}/I_{OH} .

The 74F826 is the inverted version of 74F825.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG. DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
24-pin plastic slim DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N	I74F823N	SOT222-1
24-pin plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D	I74F823D	SOT137-1

Bus interface registers

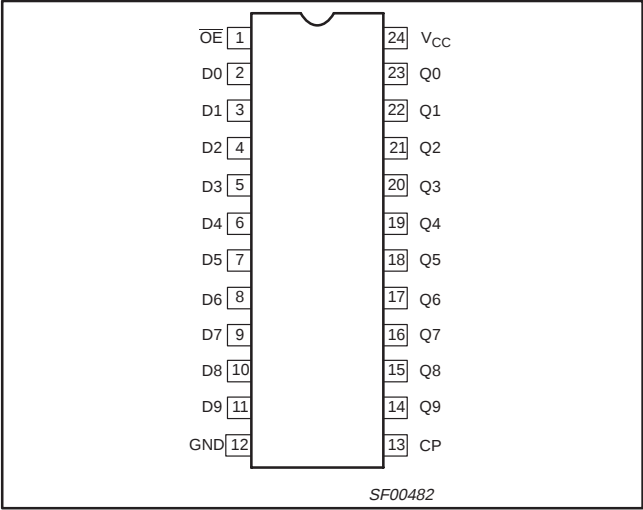
74F821/822/823/824/825/826

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

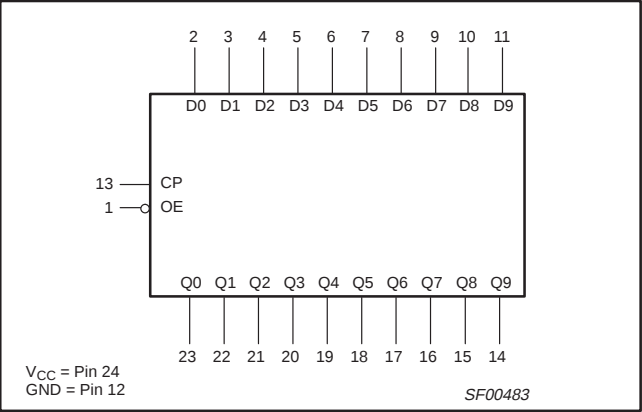
PINS		DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F821 74F822	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F823 74F824	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA
74F825 74F826	Dn	Data inputs	1.0/1.0	20µA/0.6mA
	CP	Clock input	1.0/1.0	20µA/0.6mA
	$\overline{CE}$	Clock enable input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{MR}$	Master reset input (active low)	1.0/3.0	20µA/1.8mA
	$\overline{OE}$	Output enable input (active low)	1.0/3.0	20µA/1.8mA
	Qn, $\overline{Qn}$	Data outputs	1200/106.7	24mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

PIN CONFIGURATION – 74F821



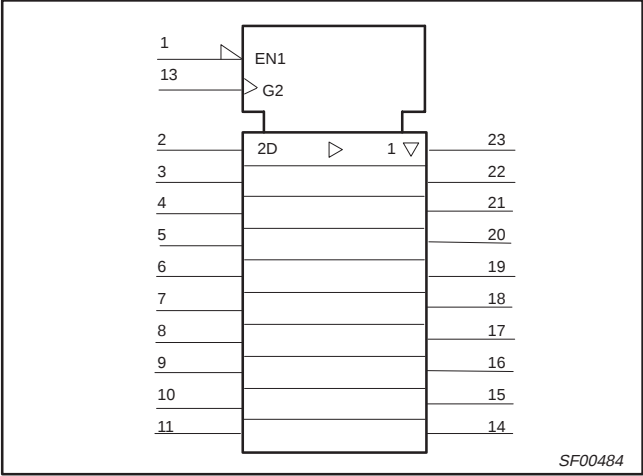
LOGIC SYMBOL – 74F821



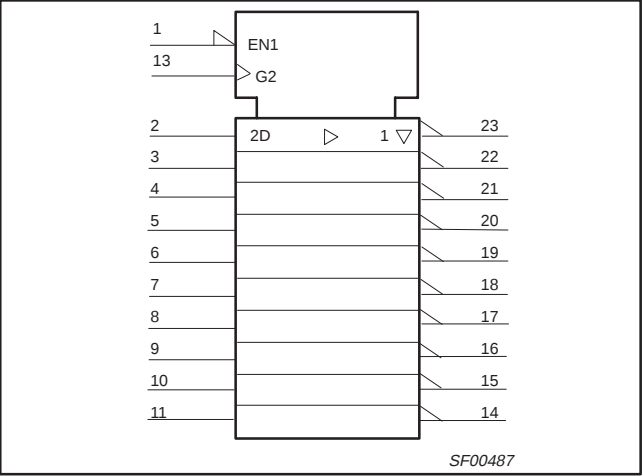
Bus interface registers

74F821/822/823/824/825/826

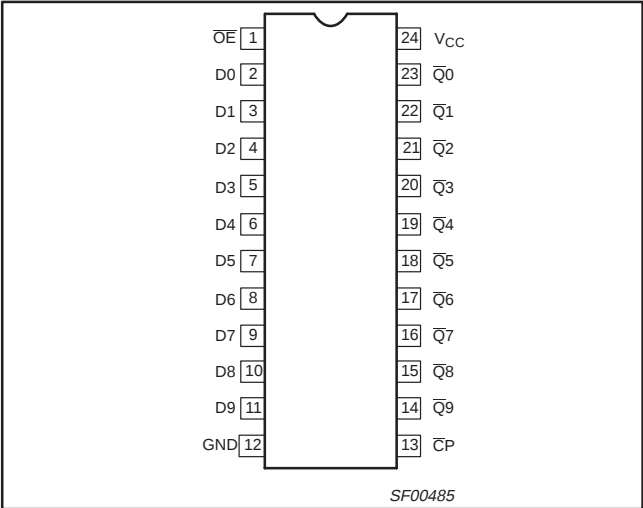
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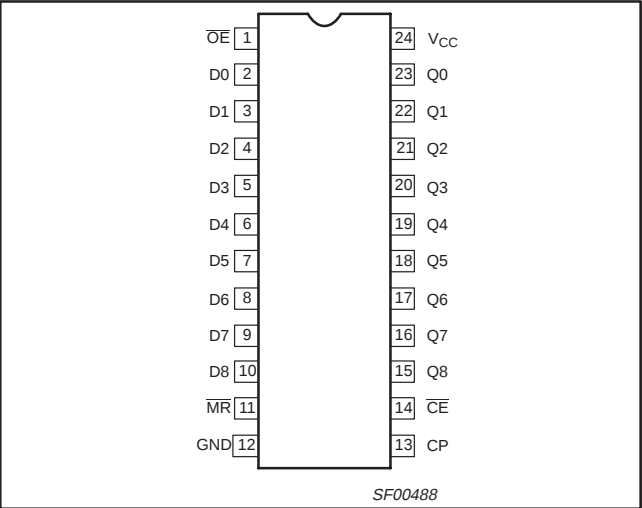
IEC/IEEE SYMBOL – 74F822



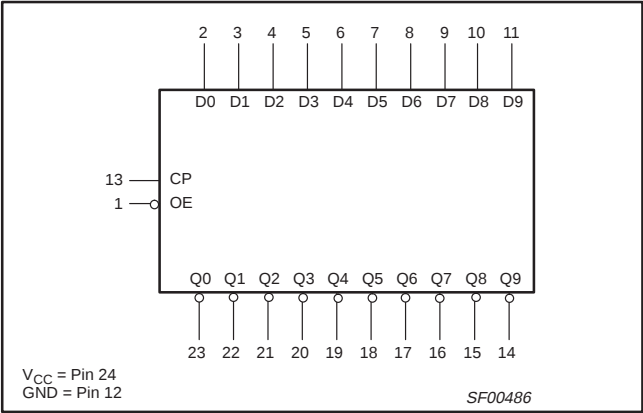
PIN CONFIGURATION – 74F822



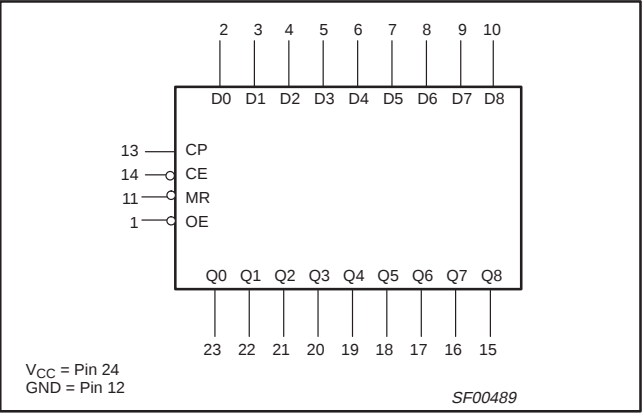
PIN CONFIGURATION – 74F823



LOGIC SYMBOL – 74F822



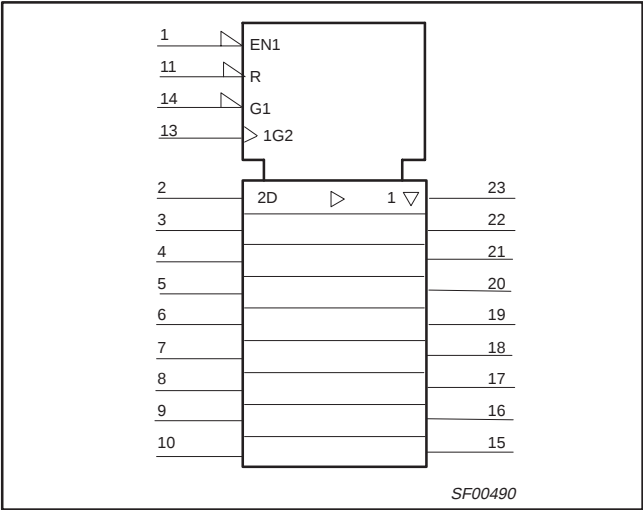
LOGIC SYMBOL – 74F823



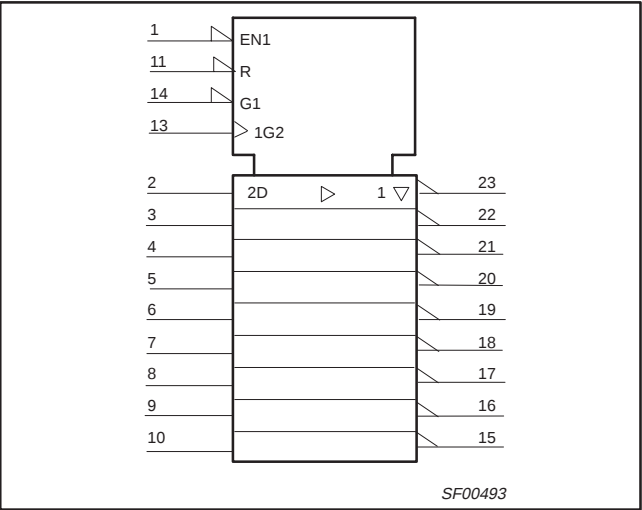
Bus interface registers

74F821/822/823/824/825/826

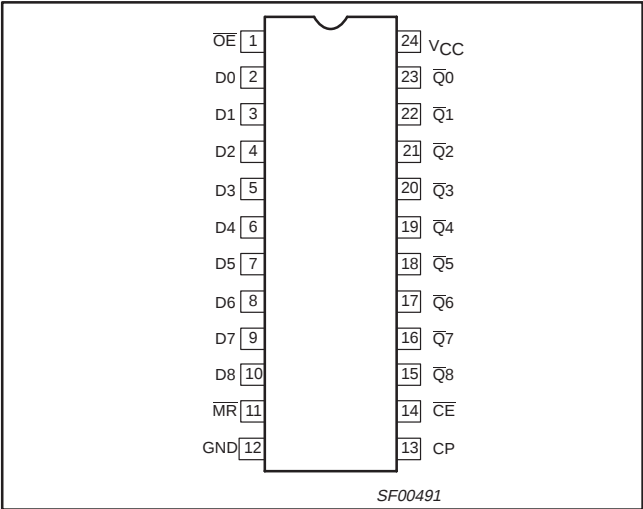
IEC/IEEE SYMBOL – 74F823



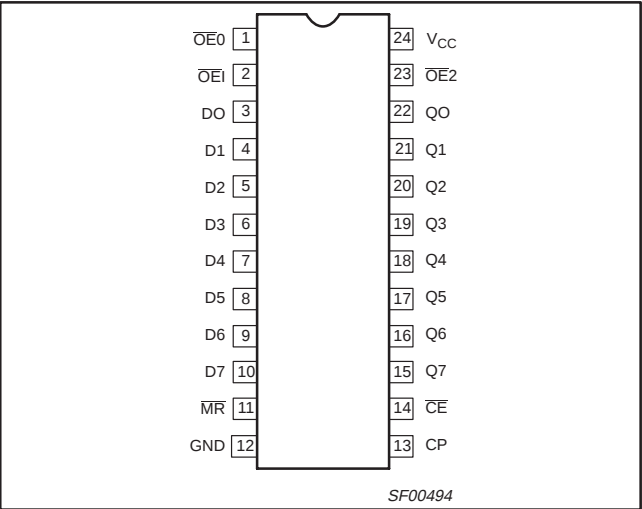
IEC/IEEE SYMBOL – 74F824



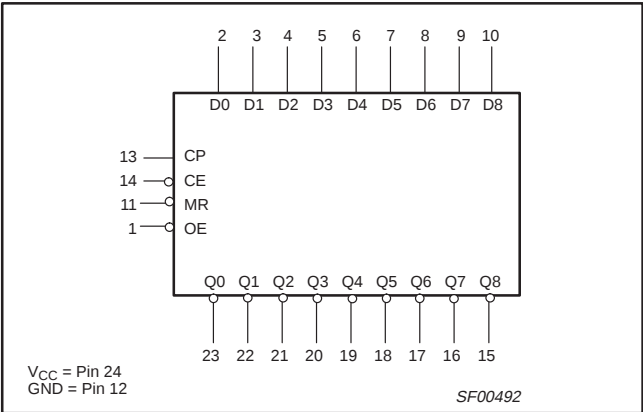
PIN CONFIGURATION – 74F824



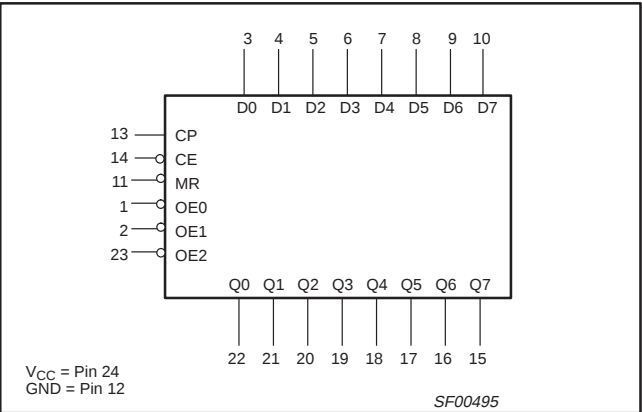
PIN CONFIGURATION – 74F825



LOGIC SYMBOL – 74F824

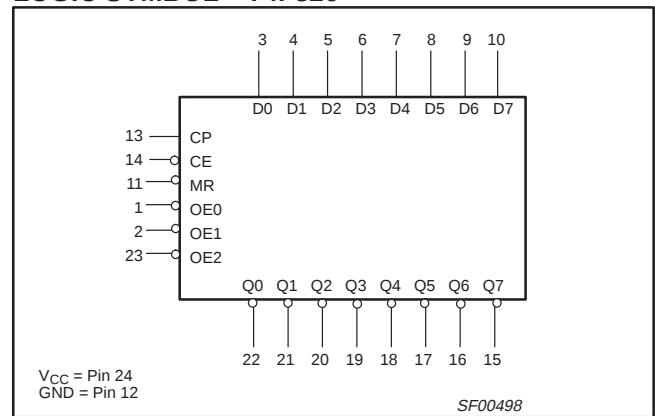


LOGIC SYMBOL – 74F825

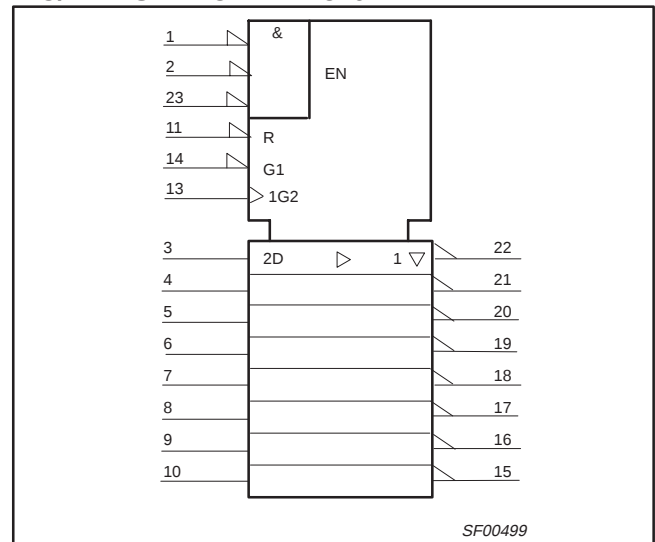


74F821/822/823/824/825/826

LOGIC SYMBOL – 74F826



IEC/IEEE SYMBOL – 74F826

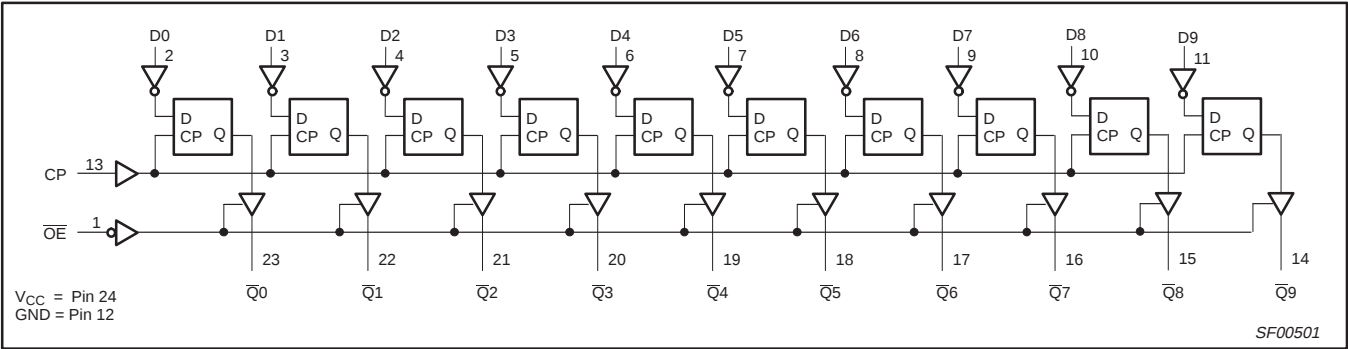


The diagram illustrates a 10-bit shift register (SF00500) implemented using ten D-type flip-flops. Each flip-flop has a clock input (CP), a data input (D), and a data output (Q). The clock inputs of all flip-flops are connected to a common clock line (CP, pin 13). The output enable input (OE, pin 1) is connected to the output of the first flip-flop (Q0, pin 23) and to the OE input of all other flip-flops. The data output of each flip-flop is connected to the next flip-flop's data input, forming a serial chain. The outputs are labeled Q0 through Q9, corresponding to pins 23 through 14. The inputs D0 through D9 are connected to pins 2 through 11. The power supply is V_{CC} = Pin 24 and GND = Pin 12.

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LOGIC DIAGRAM FOR 74F822

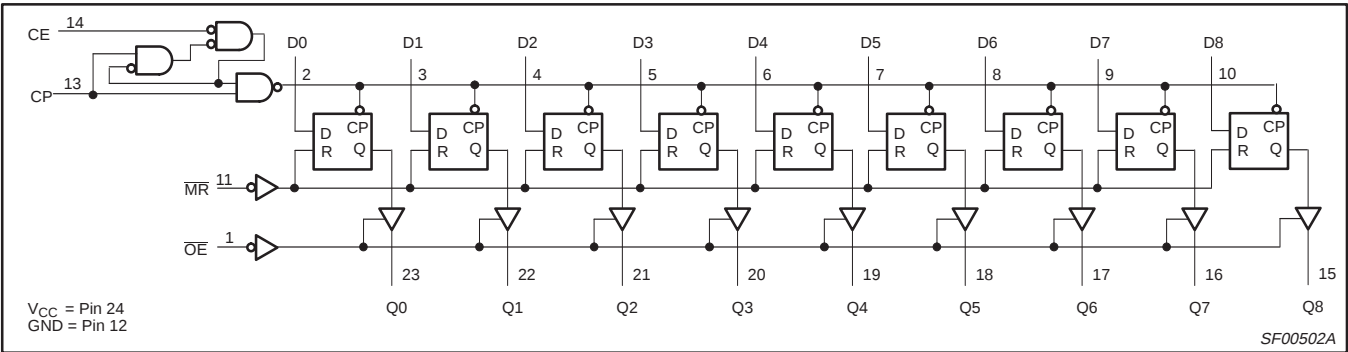


FUNCTION TABLE FOR 74F821 AND 74F822

INPUTS			OUTPUTS		OPERATING MODE
			74F821	74F822	
OE	CP	Dn	Q	Q̄	
L	↑	l	L	H	Load and read data
L	↑	h	H	L	
L	↑̄	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-high clock transition
↑̄ = Not low-to-high clock transition

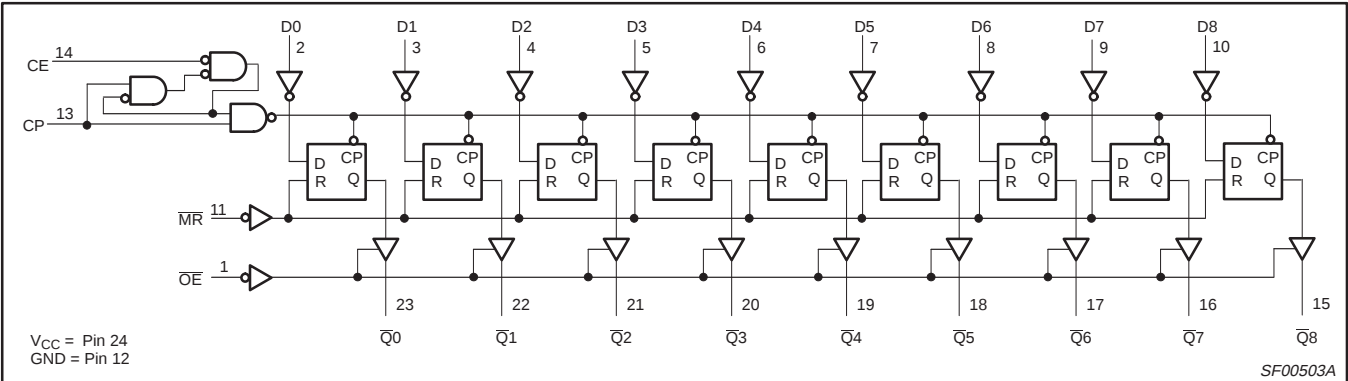
LOGIC DIAGRAM FOR 74F823



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F824

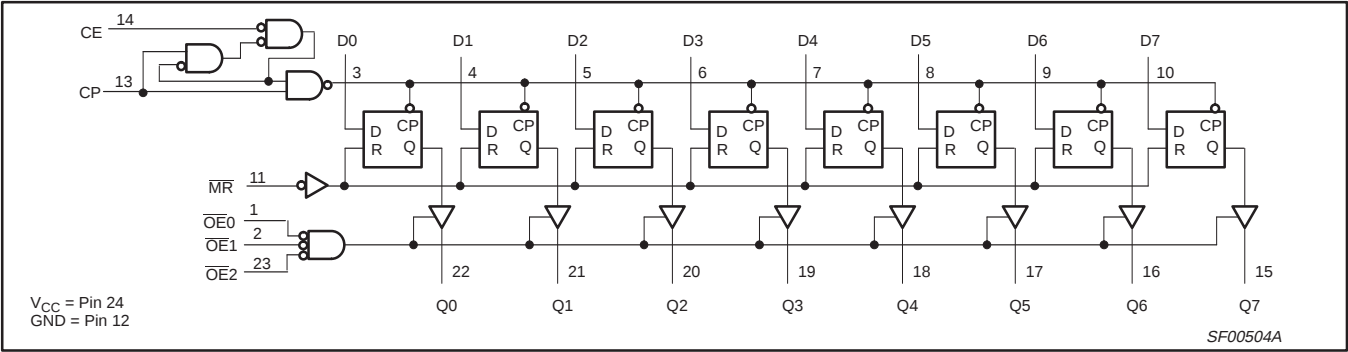


FUNCTION TABLE for 74F823 and 74F824

INPUTS					OUTPUTS		OPERATING MODE
					74F823	74F824	
OE	MR	CE*	CP	Dn	Q	Q̄	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
* = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
↑ = Low-to-high clock transition

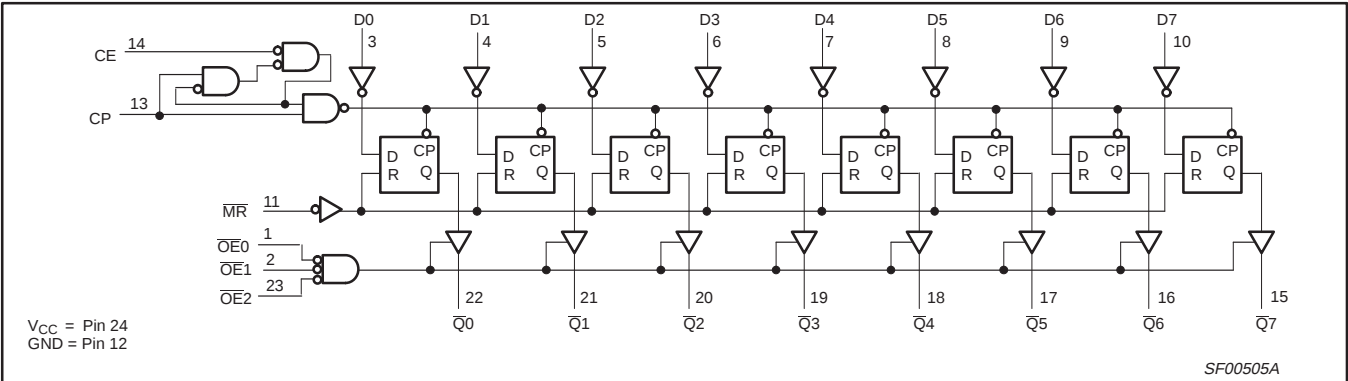
LOGIC DIAGRAM FOR 74F825



Bus interface registers

74F821/822/823/824/825/826

LOGIC DIAGRAM FOR 74F826



FUNCTION TABLE FOR 74F825 AND 74F826

INPUTS					OUTPUTS		OPERATING MODE
					74F825	74F826	
OE _n	MR	CE*	CP	D _n	Q	Q̄	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	X	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
* = Since CE input is sensitive to very short (<3ns) high-to-low-to-high going spikes while CP is high, users should avoid the use of decoders or other potentially glitch prone device on the CE input.
↑ = Low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		−0.5 to +7.0	V
V _{IN}	Input voltage		−0.5 to +7.0	V
I _{IN}	Input current		−30 to +5	mA
V _{OUT}	Voltage applied to output in high output state		−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state		128	mA
T _{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T _{stg}	Storage temperature range		−65 to +150	°C

Bus interface registers

74F821/822/823/824/825/826

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS ¹	LIMITS			UNIT
					MIN	TYP ²	MAX	
V_{OH}	High-level output voltage			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$\pm 10\%V_{CC}$	2.4		V
					$\pm 5\%V_{CC}$	2.4		V
				$I_{OH} = -24\text{mA}$	$\pm 10\%V_{CC}$	2.0		V
					$\pm 5\%V_{CC}$	2.0		V
V_{OL}	Low-level output voltage			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$\pm 10\%V_{CC}$		0.55	V
					$\pm 5\%V_{CC}$		0.42	V
V_{IK}	Input clamp voltage			$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
I_I	Input current at maximum input voltage			$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$			100	μA
I_{IH}	High-level input current			$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA
I_{IL}	Low-level input current			$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-20	μA
I_{OZH}	Off-state output current, high-level voltage applied			$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$			-50	μA
I_{OS}	Short-circuit output current ³			$V_{CC} = \text{MAX}$	-100		-225	mA
I_{CC}	Supply current (total)	74F821, 74F822	I_{CCH}	$V_{CC} = \text{MAX}$		75	105	mA
			I_{CCL}			75	105	mA
			I_{CCZ}			75	115	mA
		74F823, 74F824	I_{CCH}	$V_{CC} = \text{MAX}$		65	100	mA
			I_{CCL}			70	105	mA
			I_{CCZ}			75	110	mA
		74F825, 74F826	I_{CCH}	$V_{CC} = \text{MAX}$		60	85	mA
			I_{CCL}			60	90	mA
			I_{CCZ}			65	95	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Bus interface registers

74F821/822/823/824/825/826

AC ELECTRICAL CHARACTERISTICS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f _{max}	Maximum clock frequency		Waveform 1	150	180		140		ns
t _{PLH} t _{PHL}	Propagation delay CP to Q _n or Q̄ _n	74F821, 74F825, 74F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t _{PLH} t _{PHL}	Propagation delay CP to Q̄ _n	74F822, 74F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t _{PHL}	Propagation delay MR to Q _n or Q̄ _n	74F824 74F825, 74F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t _{PZH} t _{PZL}	Output enable time OEn to Q _n or Q̄ _n		Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t _{PHZ} t _{PLZ}	Output disable time OEn to Q _n or Q̄ _n		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

AC SETUP REQUIREMENTS FOR 74F821/74F822/74F824/74F825/74F826

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, high or low Dn to CP		Waveform 3	1.0 1.0			1.0 1.0		ns
t _h (H) t _h (L)	Hold time, high or low Dn to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
t _w (H) t _w (L)	CP Pulse width, high or low		Waveform 1	3.5 3.5			4.0 4.0		ns
t _{su} (H) t _{su} (L)	Setup time, high or low, CE to CP	74F824, 74F825, 74F826	Waveform 3	0.0 2.0			0.0 2.0		ns
t _h (H) t _h (L)	Hold time, high or low CE to CP		Waveform 3	0.0 3.0			0.0 3.5		ns
t _w (L)	MR Pulse width, low		Waveform 2	4.5			4.5		ns
t _{rec}	Recovery time, MR to CP		Waveform 2	2.5			2.5		ns

Bus interface registers

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AC ELECTRICAL CHARACTERISTICS FOR 74F823

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		T _{amb} = −40°C to +85°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}	Maximum clock frequency	Waveform 1	150	180		140		130		ns	
t _{PLH} t _{PHL}	Propagation delay CP to Q _n or Q̄ _n	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	4.0 3.5	10.0 9.0	ns	
t _{PHL}	Propagation delay MR to Q _n or Q̄ _n	Waveform 2	3.0	5.0	8.0	3.0	8.0	3.0	8.5	ns	
t _{PZH} t _{PZL}	Output enable time OEn to Q _n or Q̄ _n	Waveform 4 Waveform 5	2.0 3.0	4.5 5.0	8.0 8.0	2.0 2.5	9.0 9.0	2.0 2.5	11.0 9.0	ns	
t _{PHZ} t _{PLZ}	Output disable time OEn to Q _n or Q̄ _n	Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	1.5 1.5	8.5 8.5	ns	

AC SETUP REQUIREMENTS FOR 74F823

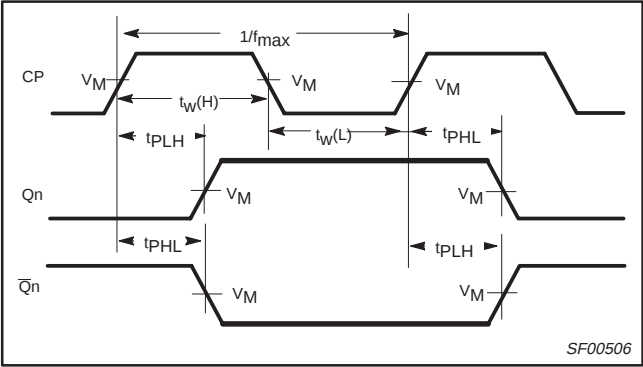
SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω		T _{amb} = −40°C to +85°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _{su} (H) t _{su} (L)	Setup time, high or low Dn to CP	Waveform 3	1.0 1.0			1.0 1.0		2.0 1.5		ns	
t _h (H) t _h (L)	Hold time, high or low Dn to CP	Waveform 3	2.0 2.0			2.0 2.0		2.5 2.0		ns	
t _w (H) t _w (L)	CP Pulse width, high or low	Waveform 1	3.5 3.5			4.0 4.0		4.0 4.0		ns	
t _{su} (H) t _{su} (L)	Setup time, high or low, CE to CP	Waveform 3	0.0 2.0			0.0 2.0		0.0 2.0		ns	
t _h (H) t _h (L)	Hold time, high or low CE to CP	Waveform 3	0.0 3.0			0.0 3.5		1.5 4.0		ns	
t _w (L)	MR Pulse width, low	Waveform 2	4.5			4.5		4.5		ns	
t _{rec}	Recovery time, MR to CP	Waveform 2	2.5			2.5		2.5		ns	

Bus interface registers

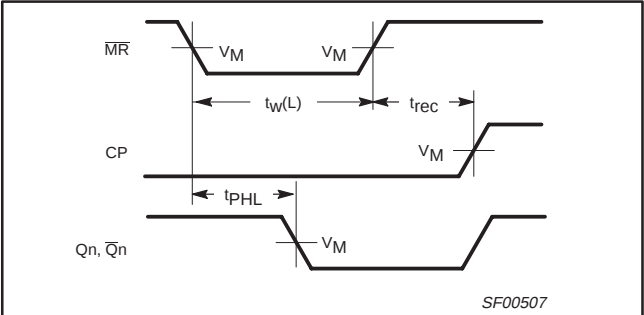
74F821/822/823/824/825/826

AC WAVEFORMS

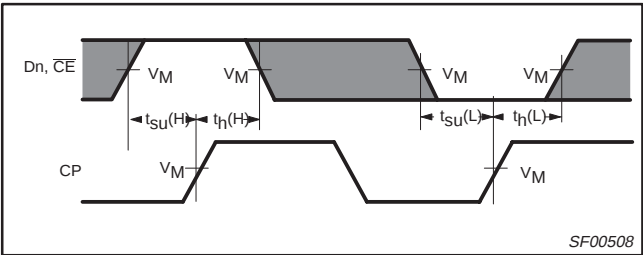
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



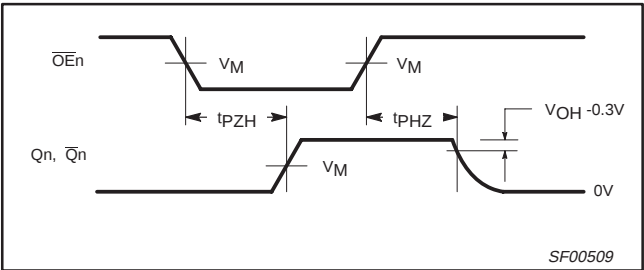
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



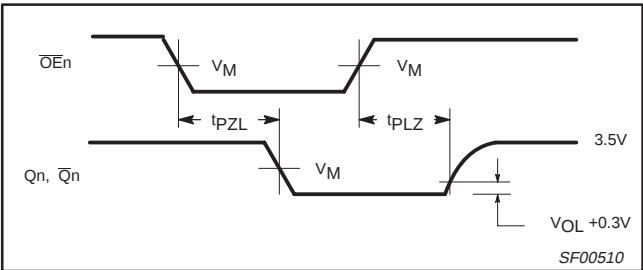
Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time



Waveform 3. Data setup time and hold times



Waveform 4. 3-State output enable time to high level and output disable time from high level

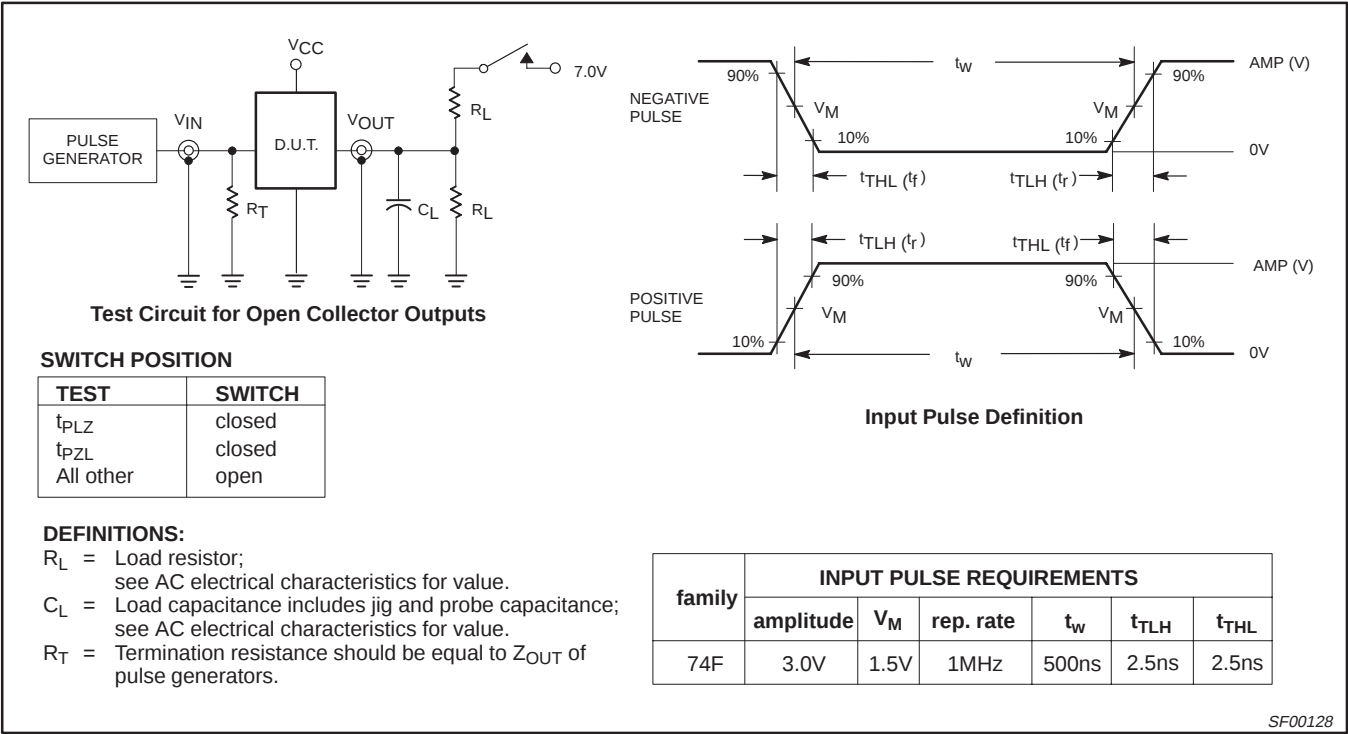


Waveform 5. 3-State output enable time to low level and output disable time from low level

Bus interface registers

74F821/822/823/824/825/826

TEST CIRCUIT AND WAVEFORMS



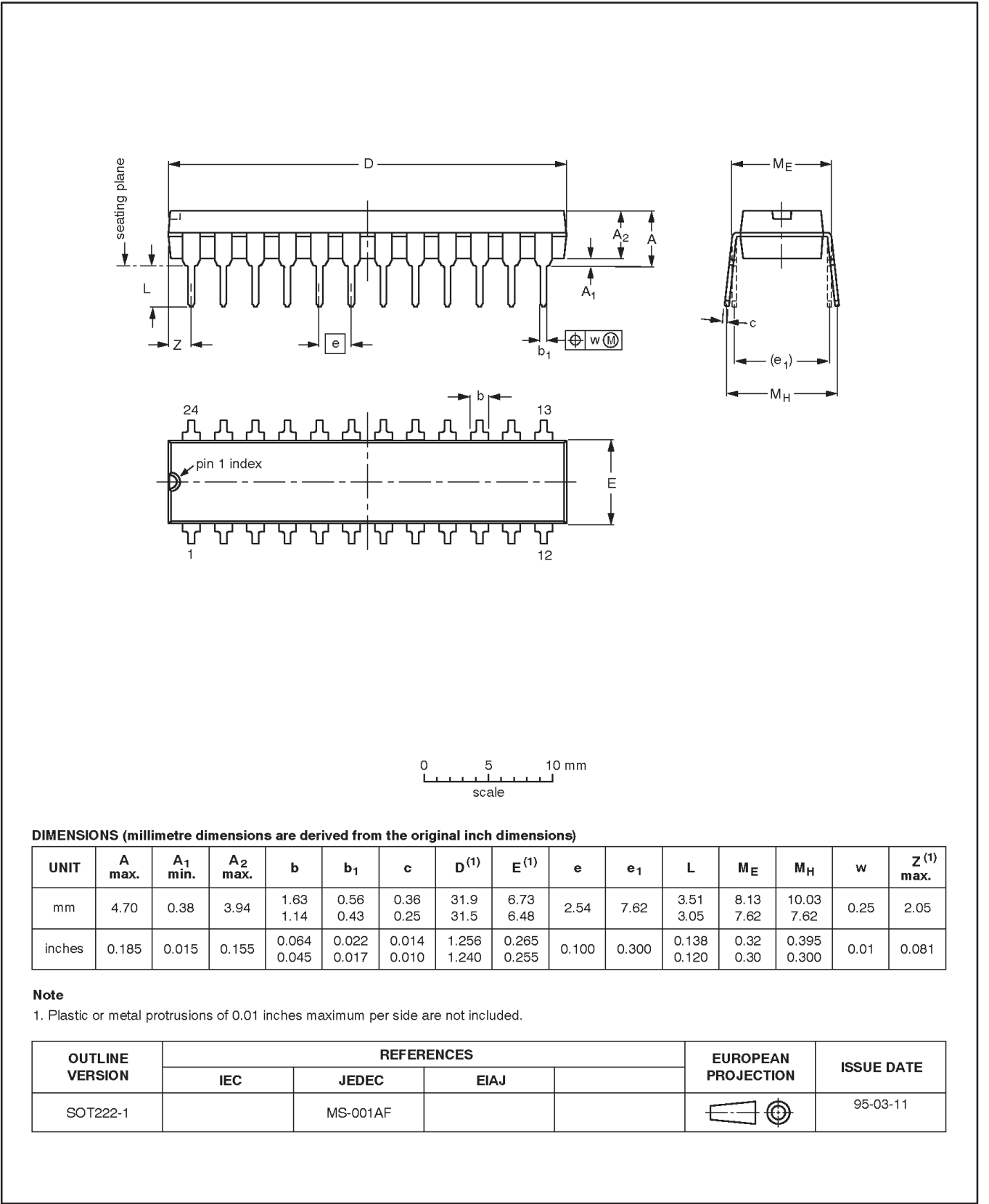
SF00128

Bus interface registers

74F821/822/823/824/825/826

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

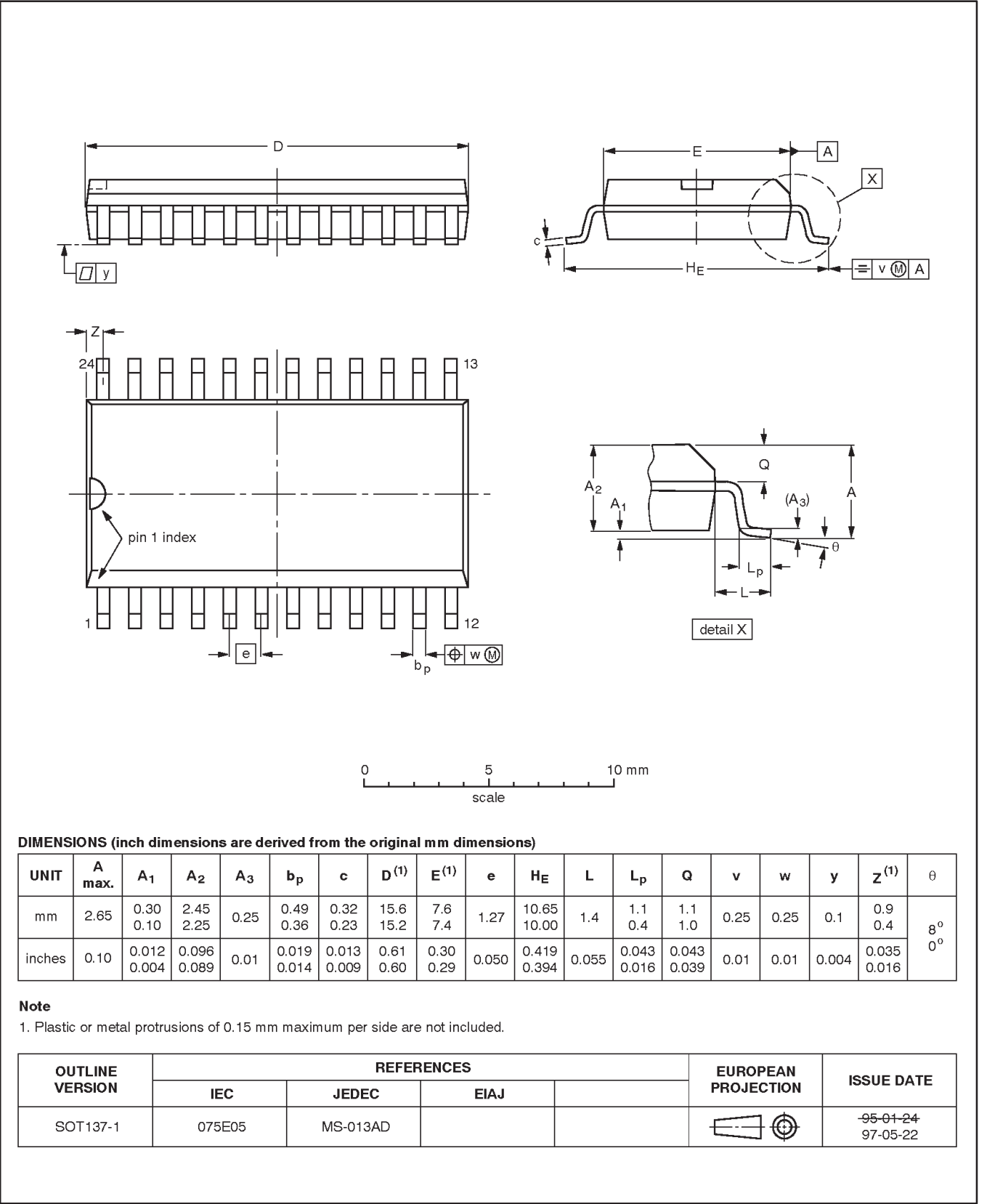


Bus interface registers

74F821/822/823/824/825/826

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



Bus interface registers

74F821/822/823/824/825/826

NOTES

Bus interface registers

74F821/822/823/824/825/826

DEFINITIONS		
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