

# DATA SHEET

## **74F711A, 74F711-1, 74F712A, 74F712-1** Multiplexers

Product specification

1990 Dec 13

IC15 Data Handbook

## Multiplexers

### 74F711A/74F711-1/ 74F712A/74F712-1

74F711A Quint 2-to-1 Data Selector Multiplexer (3-State)

74F711-1 Quint 2-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance (3-State)

74F712A Quint 3-to-1 Data Selector Multiplexer

74F712-1 Quint 3-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance

#### FEATURES for 74F711A/74F711-1

- Consists of five 2-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- Output inverting/non-inverting option
- 30Ω termination impedance on each output – 74F711-1
- Outputs sink 64mA (74F711A only)

#### FEATURES for 74F712A/74F712-1

- Consists of five 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- 30Ω termination impedance on each output – 74F712-1
- Outputs sink 64mA (74F712A only)

#### DESCRIPTION

The 74F711A/74F711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F711A has a common select (S) input, an Output Enable (OE) input and an Output Inverting (INV) input to control the 3-State outputs. The outputs source 15mA and sink 64mA. The 74F711-1 is the same as the 74F711A except that it has a 30Ω termination impedance on each output to reduce line noise and the 3-State outputs sink 5mA.

When the inverting input (INV) is Low, the input data path is inverted.

#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F711A/ 74F711-1	Dna, Dnb	Data inputs	1.0/0.066	20μA/40μA
	S	Select input	1.0/0.033	20μA/20μA
	OE	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	INV	Output inverting input (active Low)	1.0/0.033	20μA/20μA
	Q0 - Q4	Data outputs for 74F711A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F711-1	750/8.33	15mA/5mA
74F712A/ 74F712-1	Dna, Dnb, Dnc	Data inputs	1.0/0.066	20μA/40μA
	S0, S1	Select inputs	1.0/0.033	20μA/20μA
	Q0 - Q4	Data outputs for 74F712A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F712-1	750/8.33	15mA/5mA

**NOTE:** One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

To improve speed and noise immunity, V<sub>CC</sub> and GND side pins are used.

The 74F712A/74F712-1 consist of five 3-to1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F712A has two select (S0, S1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 74F712-1 is the same as the 74F712A except that it has a 30Ω termination impedance on each output to reduce line noise and the outputs sink 5mA.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	6.5ns	25mA
74F712-1	6.5ns	25mA

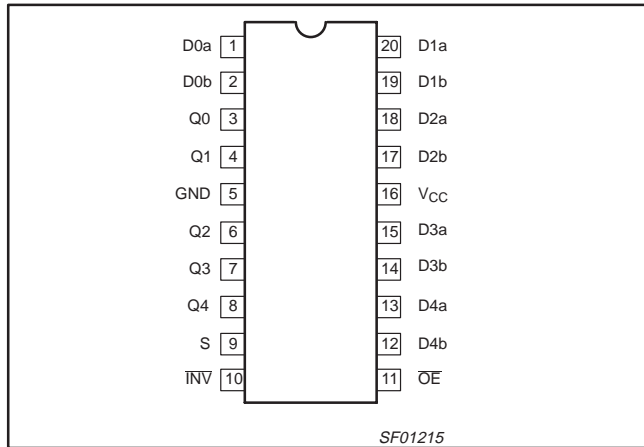
#### ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ± 10% T <sub>amb</sub> = 0° C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F711AN, N74F711-1N	SOT146-1
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N	SOT222-1
20-Pin Plastic SOL	N74F711AD, N74F711-1D	SOT163-1
24-Pin Plastic SOL	N74F712AD, N74F712-1D	SOT137-1

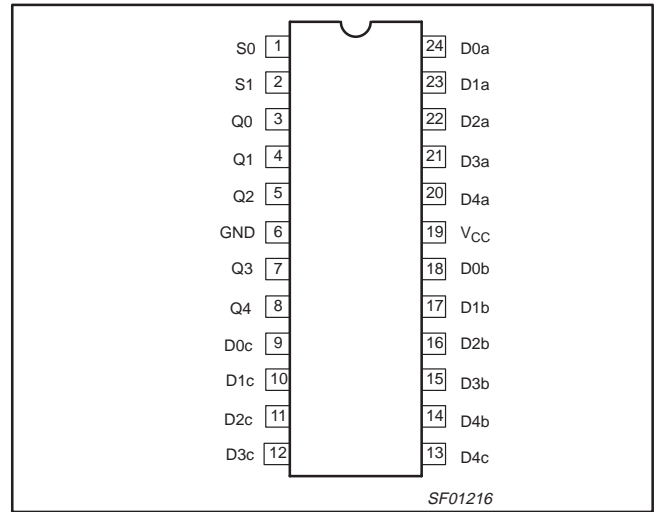
# Multiplexers

## 74F711A/74F711-1/ 74F712A/74F712-1

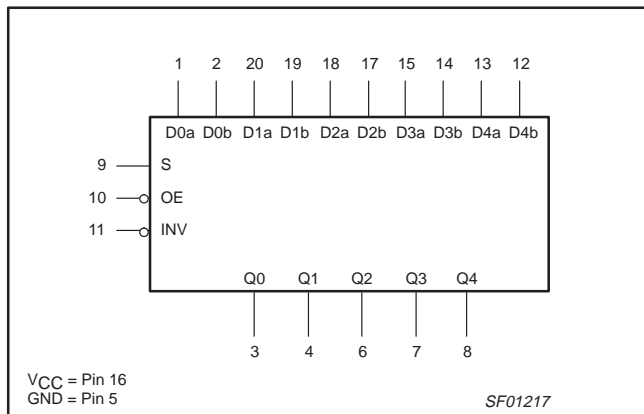
### PIN CONFIGURATION – 74F711A/74F711-1



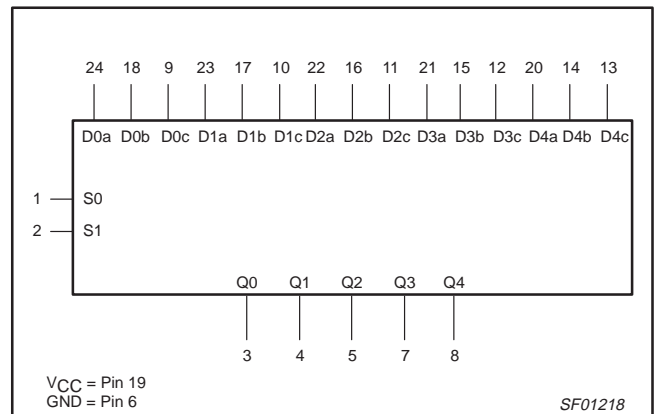
### PIN CONFIGURATION – 74F712A/74F712-1



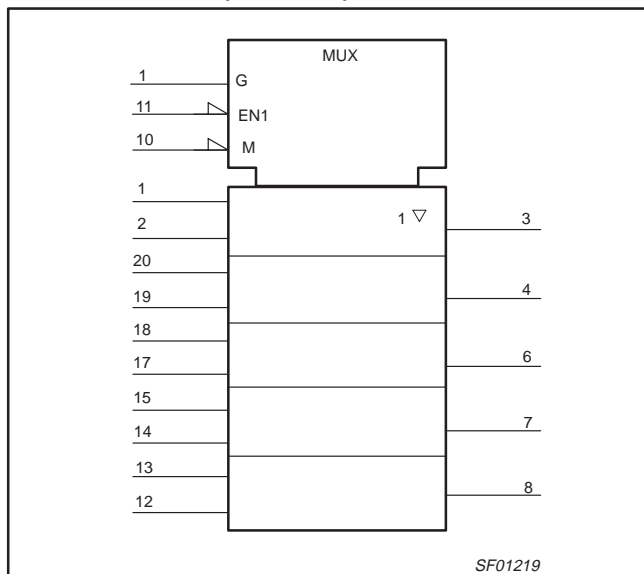
### LOGIC SYMBOL – 74F711A/74F711-1



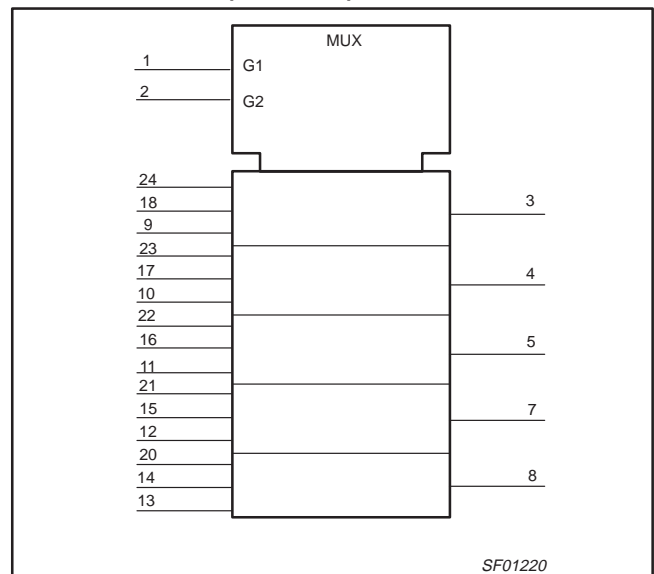
### LOGIC SYMBOL – 74F712A/74F712-1



### LOGIC SYMBOL (IEEE/IEC) – 74F711A/74F711-1



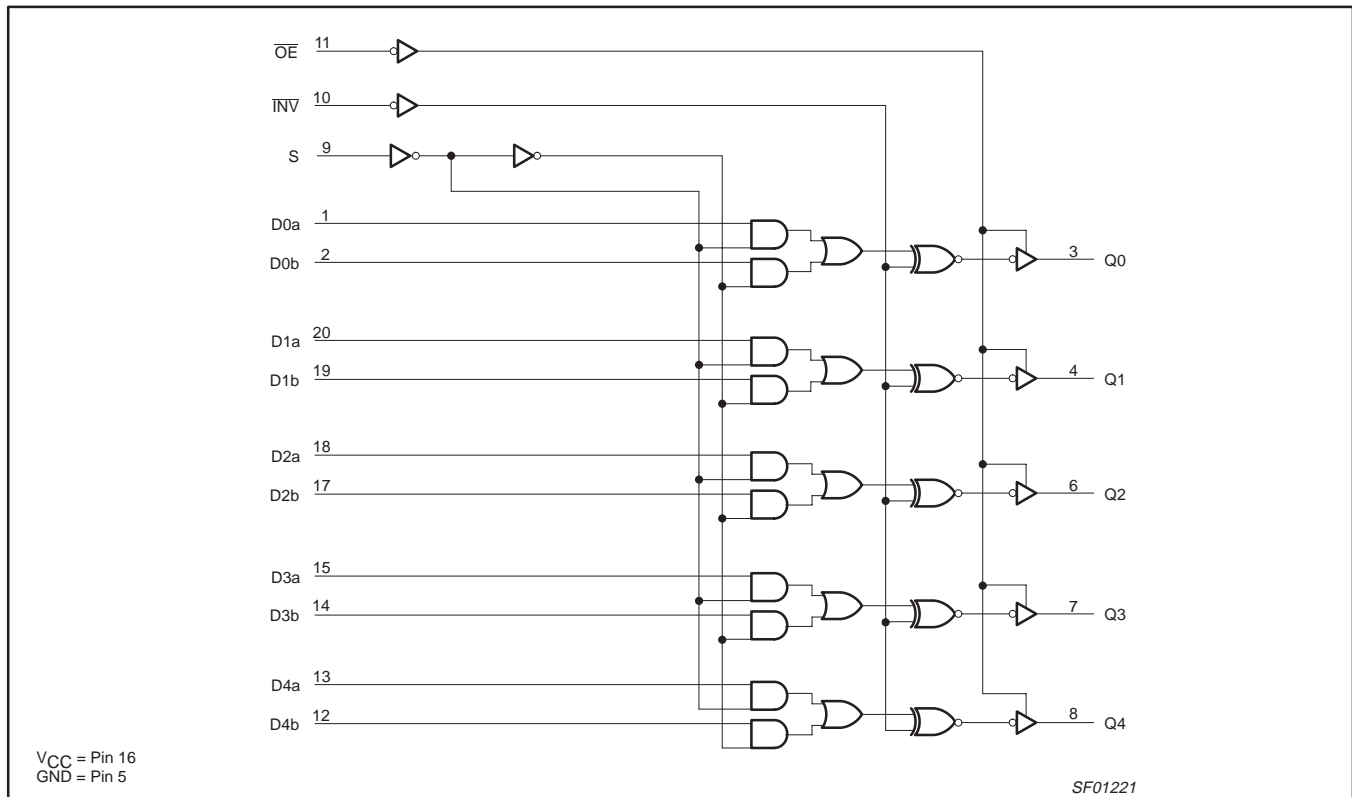
### LOGIC SYMBOL (IEEE/IEC) – 74F712A/74F712-1



# Multiplexers

74F711A/74F711-1/  
74F712A/74F712-1

## LOGIC DIAGRAM – 74F711A/74F711-1



## FUNCTION TABLE – 74F711A/74F711-1

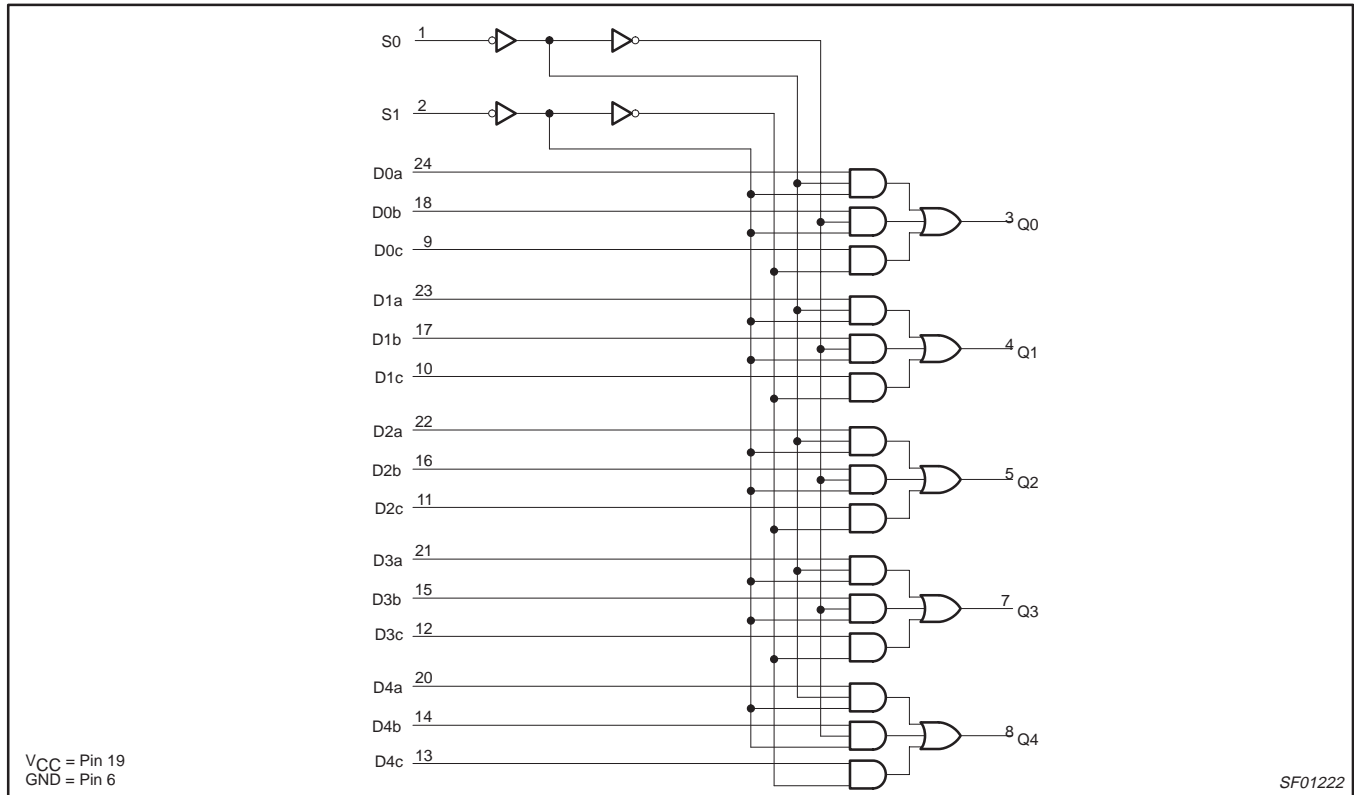
INPUTS					OUTPUT
S	INV	OE	Dna	Dnb	Qn
L	L	L	Data a	Data b	$\overline{\text{Data a}}$
H	L	L	Data a	Data b	$\overline{\text{Data b}}$
L	H	L	Data a	Data b	Data a
H	H	L	Data a	Data b	Data b
X	X	H	X	X	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High impedance "off" state

# Multiplexers

74F711A/74F711-1/  
74F712A/74F712-1

## LOGIC DIAGRAM – 74F712A/74F712-1



## FUNCTION TABLE – 74F712A/74F712-1

INPUTS					OUTPUT
S0	S1	Dna	Dnb	Dnc	Qn
L	L	Data a	Data b	Data c	Data a
H	L	Data a	Data b	Data c	Data b
X	H	Data a	Data b	Data c	Data c

H = High voltage level  
L = Low voltage level  
X = Don't care

## Multiplexers

74F711A/74F711-1/  
74F712A/74F712-1**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	74F711A, 74F712A	96
		74F711-1, 74F712-1	10
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current	74F711A, 74F712A		64	mA
		74F711-1, 74F712-1		5	mA
$T_{amb}$	Operating free-air temperature	0		70	°C

## Multiplexers

74F711A/74F711-1/  
74F712A/74F712-1**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT	
						MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V	
					±5%V <sub>CC</sub>	2.7	3.4		V	
				I <sub>OH</sub> = -15mA	±10%V <sub>CC</sub>	2.0			V	
					±5%V <sub>CC</sub>	2.0			V	
V <sub>OL</sub>	Low-level output voltage	74F711A/ 74F712A only	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.38	0.55	V	
					±5%V <sub>CC</sub>		0.42	0.55	V	
	I <sub>OL</sub> = 5mA	±10%V <sub>CC</sub>			0.38	0.50	V			
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V					100	μA	
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current	Others	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-20	μA	
		Dn only						-40	μA	
I <sub>OZH</sub>	Off-state output current High-level voltage applied	74F711A/ 74F711-1 only	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					50	μA	
I <sub>OZL</sub>	Off-state output current Low-level voltage applied					V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V				
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	74F711-1/ 74F712-1	V <sub>CC</sub> = MAX			-60		-150	mA	
I <sub>O</sub>	Output current <sup>4</sup>	74F711A/ 74F712A	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25 V			-60		-150	mA	
I <sub>CC</sub>	Supply current (total)	74F711A	V <sub>CC</sub> = MAX			I <sub>CCH</sub>		25	35	mA
						I <sub>CCL</sub>		33	46	mA
						I <sub>CCZ</sub>		27	40	mA
		74F711-1				I <sub>CCH</sub>		26	40	mA
						I <sub>CCL</sub>		33	45	mA
						I <sub>CCZ</sub>		28	45	mA
		74F712A				I <sub>CCH</sub>		20	27	mA
						I <sub>CCL</sub>		30	40	mA
						I <sub>CCZ</sub>		20	30	mA
		74F712-1				I <sub>CCH</sub>		20	30	mA
I <sub>CCL</sub>			29	40	mA					

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- I<sub>O</sub> is tested under conditions that produce current approximately one half of the true short-circuit output current (I<sub>OS</sub>).

## Multiplexers

74F711A/74F711-1/  
74F712A/74F712-1

## AC ELECTRICAL CHARACTERISTICS – 74F711A/74F711-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = 5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = 5V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb to Qn	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to Qn		Waveform 1, 3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay INV to Qn		Waveform 1, 3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time OE to Qn		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time OE to Qn		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb to Qn	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S, INV to Qn		Waveform 1, 3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time OE to Qn		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time OE to Qn		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns ns

## AC ELECTRICAL CHARACTERISTICS – 74F712A/74F712-1

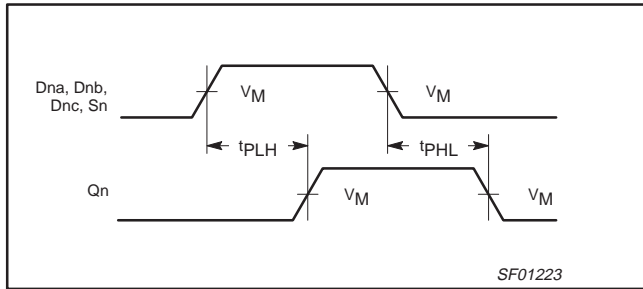
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = 5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0 to +70°C V <sub>CC</sub> = 5V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb, Dnc to Qn	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S0, S1 to Qn		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dna, Dnb, Dnc to Qn	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S0, S1 to Qn		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns ns

# Multiplexers

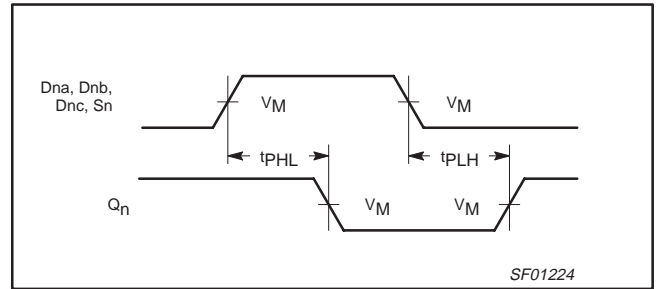
74F711A/74F711-1/  
74F712A/74F712-1

## AC WAVEFORMS

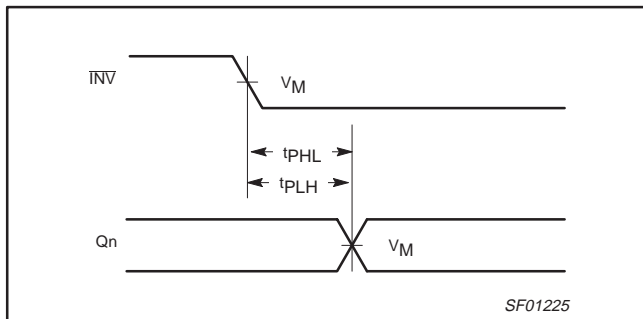
For all waveforms,  $V_M = 1.5V$



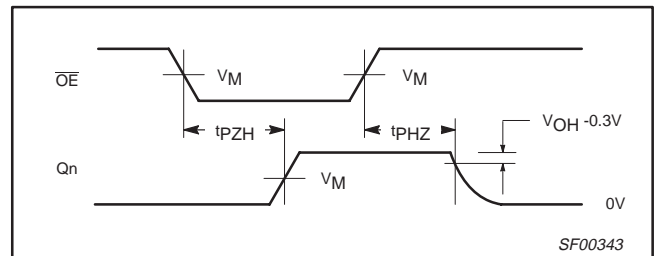
**Waveform 1. Propagation Delay for Non-Inverting Output**



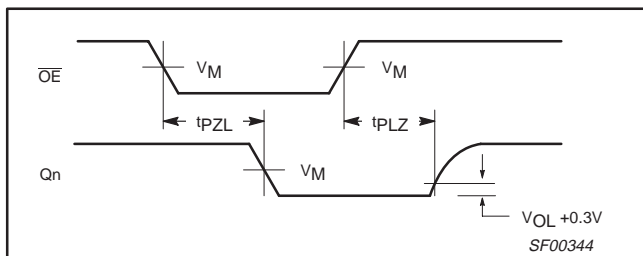
**Waveform 2. Propagation Delay for Inverting Output**



**Waveform 3. Propagation Delay for  $\overline{INV}$  to Output**



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

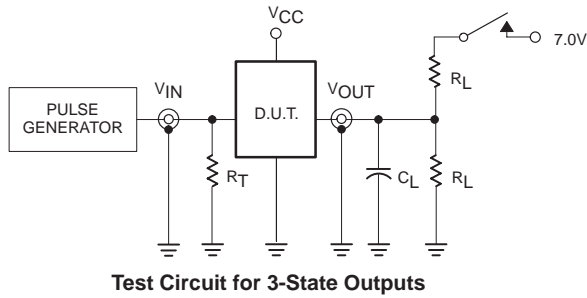


**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

# Multiplexers

## 74F711A/74F711-1/ 74F712A/74F712-1

### TEST CIRCUIT AND WAVEFORMS



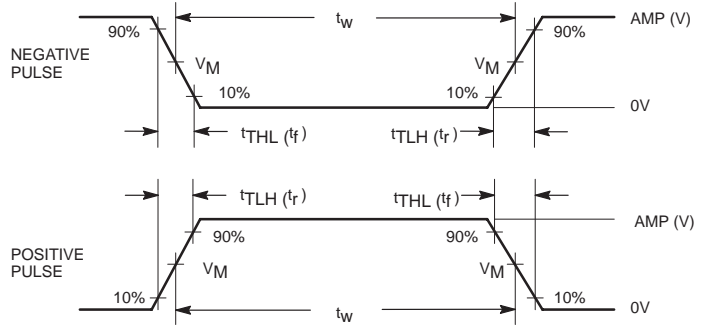
Test Circuit for 3-State Outputs

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

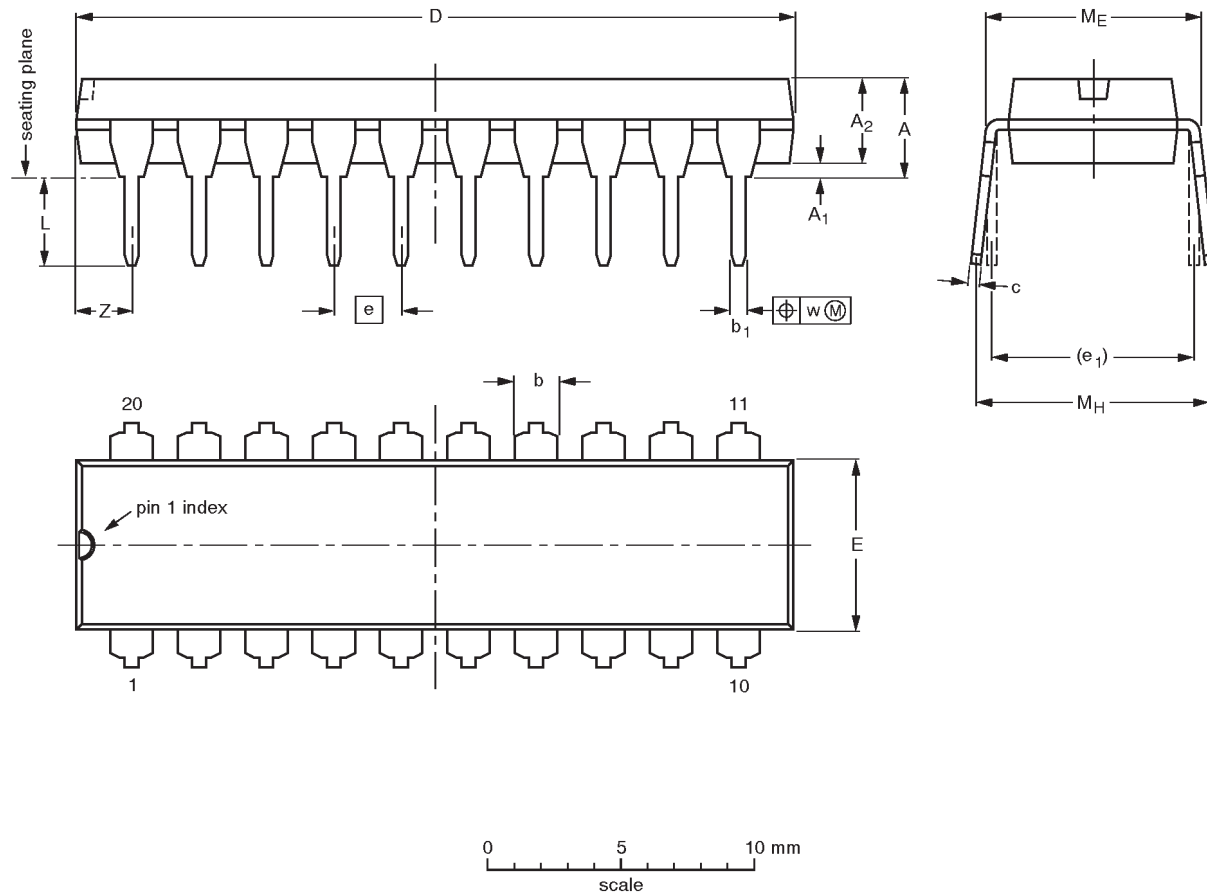
SF00777

# Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

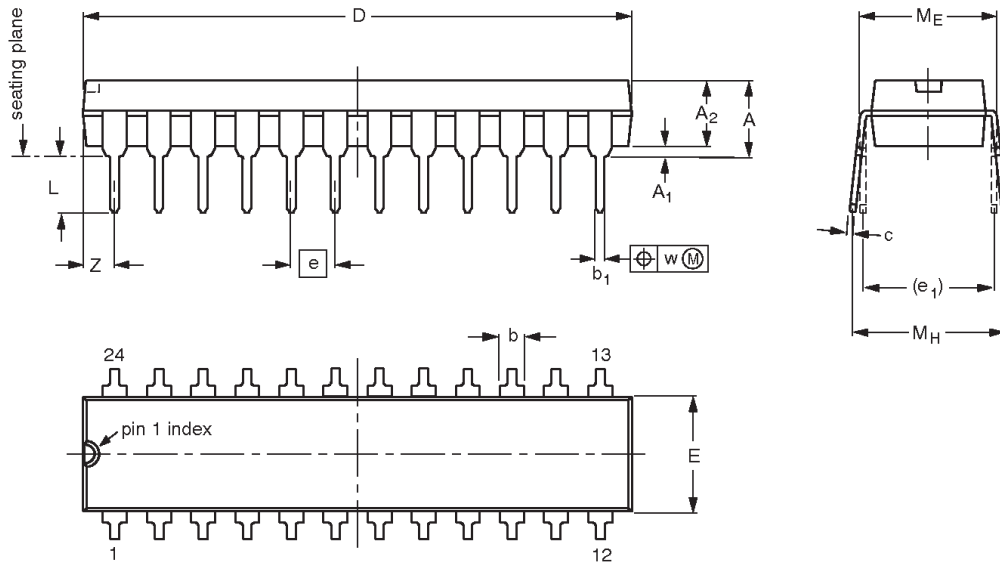
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

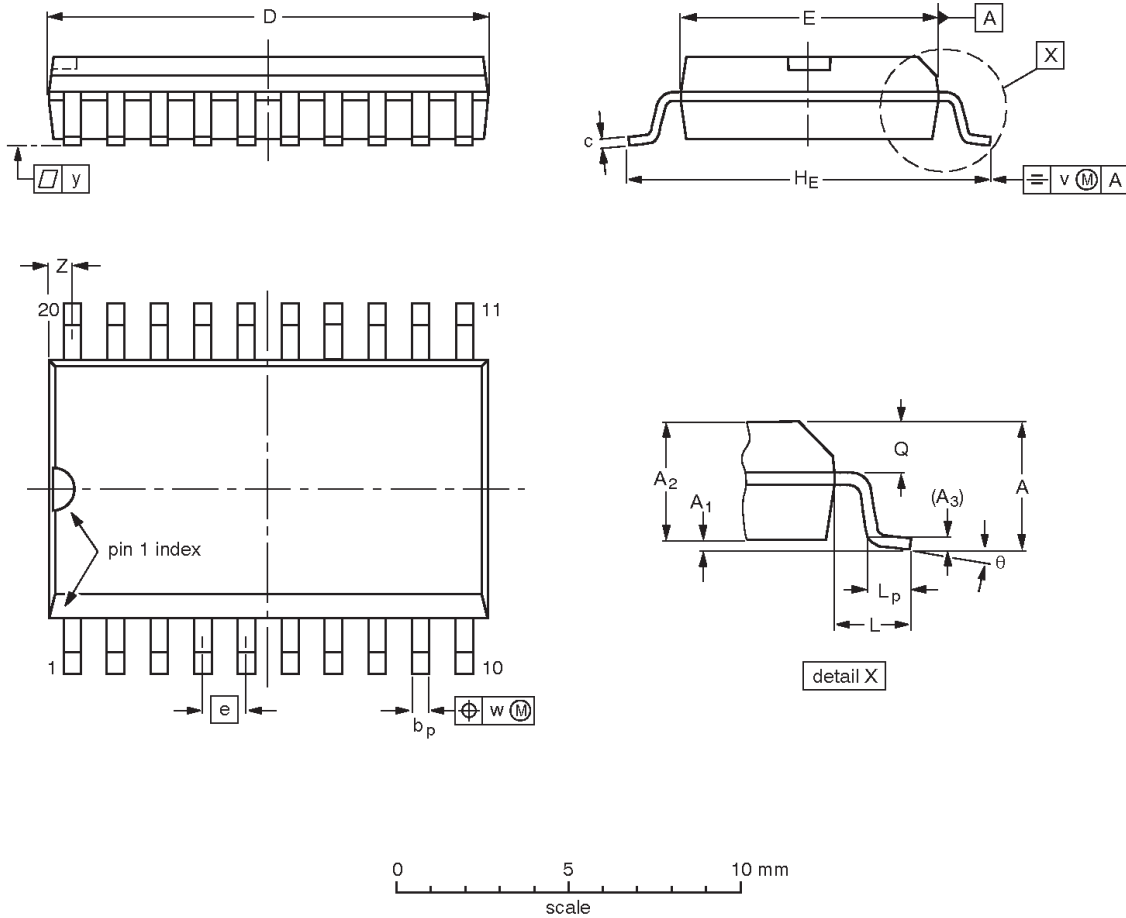
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

# Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

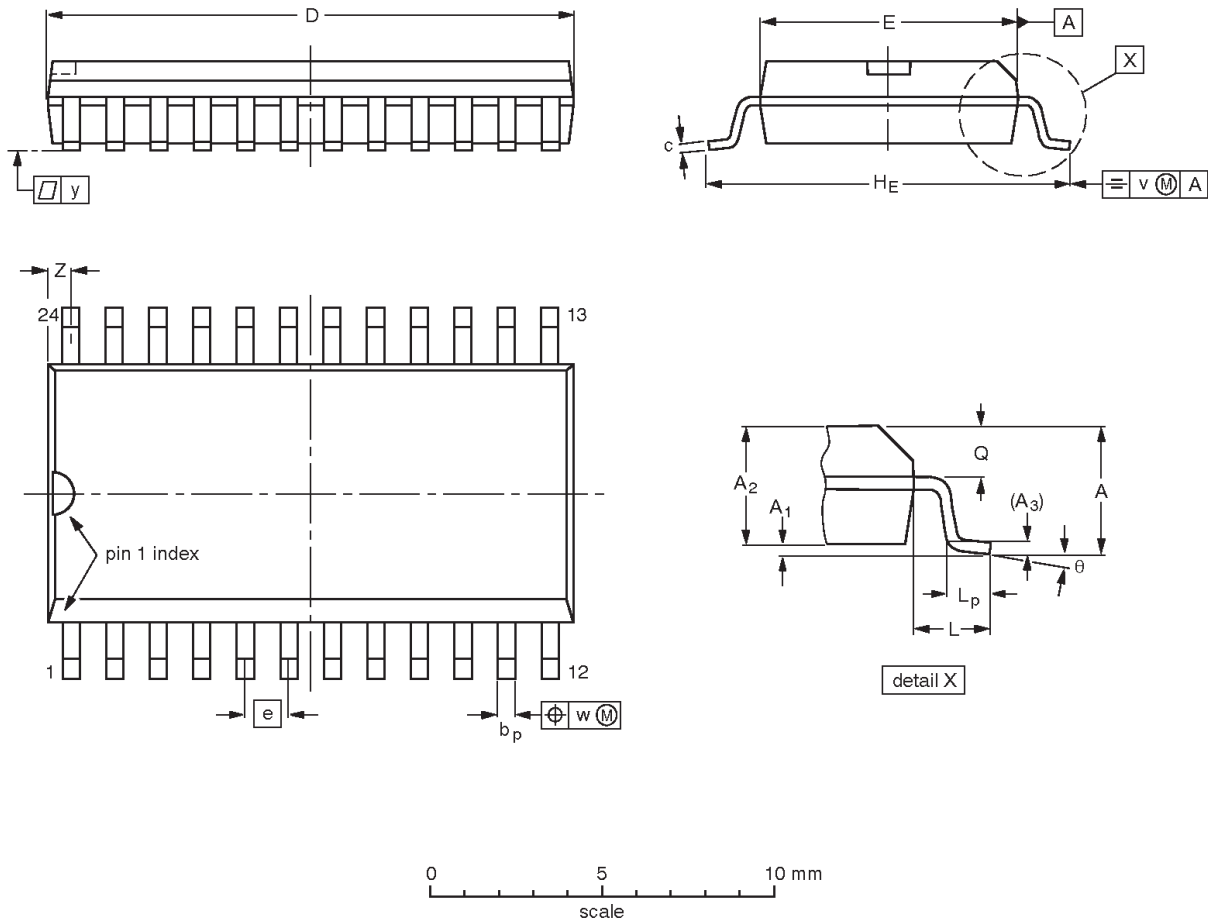
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

# Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

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Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

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**NOTES**

# Multiplexers

74F711A/74F711-1,  
74F712A/74F712-1

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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