16-bit serial/parallel-in, serial-out shift register (3-State) 74F674

FEATURES

- 16-bit serial I/O shift register
- 16-bit parallel-in/serial-out converter
- Recirculating serial shifting
- Common serial data I/O pin (3-State)

DESCRIPTION

The 74F674 is a 16-bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as a 3-State serial output. In the serial out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility. The 74F674 operates in one of four modes, as indicated in the Function table.

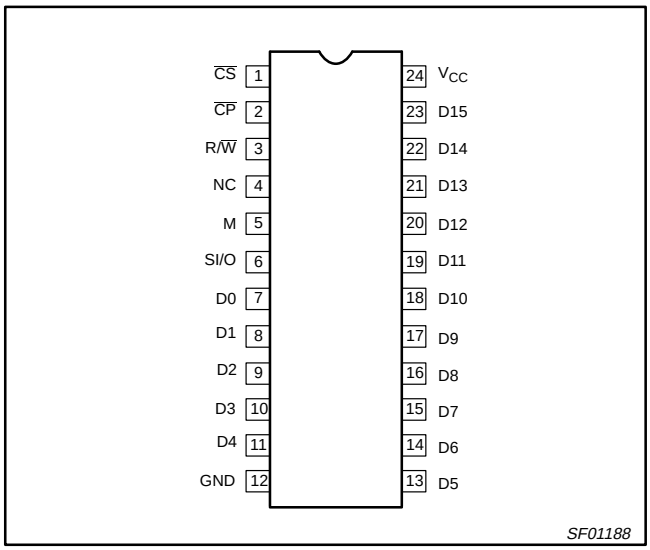
Hold: A High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-State buffer into the high impedance state.

Serial load: Data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q0 position and shifts toward Q15 on successive clocks.

Serial output: The SI/O 3-State buffer is active and the register contents are shifted out from Q15 and simultaneously shifted back into Q0.

Parallel load: Data present on D0–D15 is entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-State buffer is active and represents the Q15 output. To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	95MHz	55mA

ORDERING INFORMATION

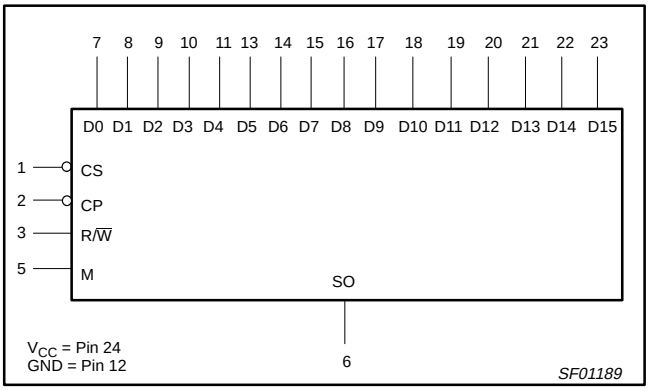
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

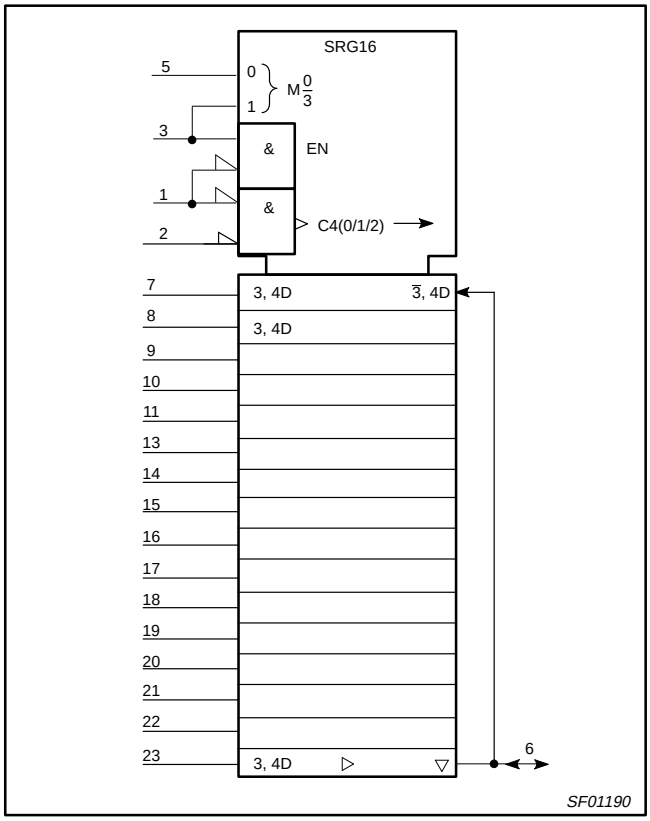
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D15	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
SI/O	Serial data input or	3.5/1.0	70mA/0.6mA
	Serial 3-state output	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

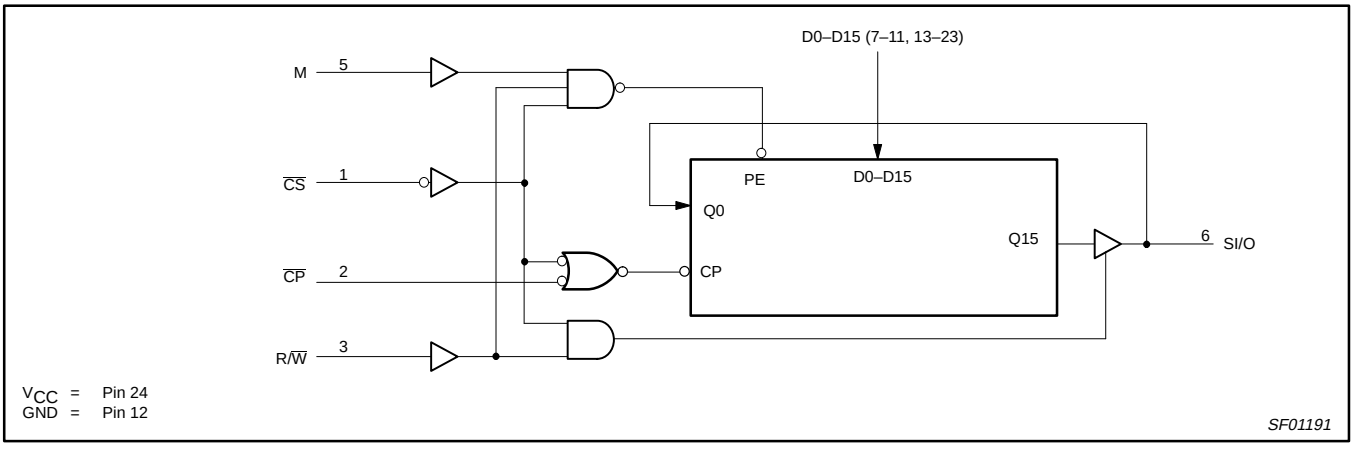


FUNCTION TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of designed input

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	SI/O only	V_{CC} = MAX, V_I = 5.5V				100	µA
		others	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}+I_{IH}	Off-state output current High-level voltage applied	SI/O only	V_{CC} = MAX, V_O = 2.7V				70	µA
I_{OZL}+I_{IL}	Off-state output current Low-level voltage applied	SI/O only	V_{CC} = MAX, V_O = 0.5V				–600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

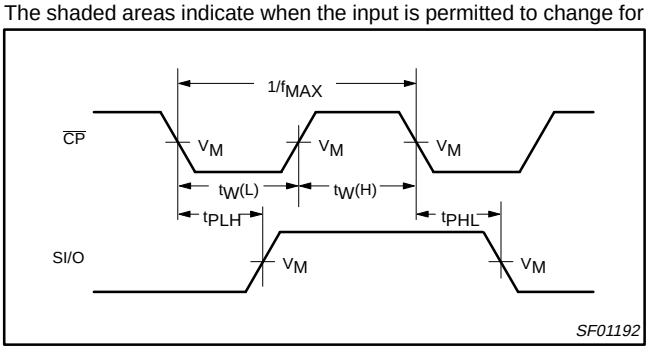
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SI/O	Waveform 1	7.0 6.0	9.5 8.5	12.5 11.5	6.5 5.5	14.0 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	5.5 7.0	8.5 9.5	11.0 12.5	5.0 6.5	12.5 14.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	3.0 4.5	6.0 7.5	8.5 10.0	3.0 4.5	10.0 11.5	ns ns
t_{PZH} t_{PZL}	Output Enable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	6.0 7.5	8.5 10.0	11.5 13.0	5.5 7.0	13.0 14.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	5.0 5.5	7.5 8.0	10.5 11.0	4.5 5.0	12.0 13.5	ns ns

AC SETUP REQUIREMENTS

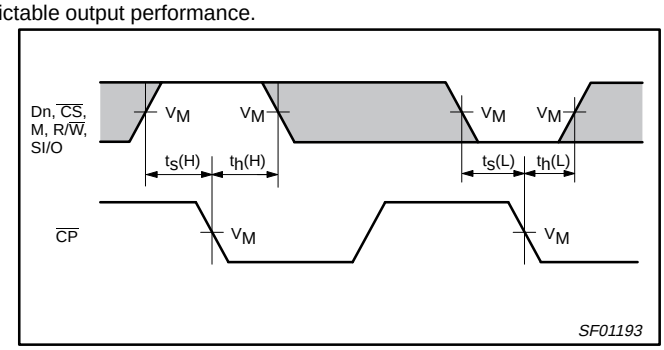
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low SI/O to $\overline{CP}$	Waveform 2	2.0 2.0			2.5 2.5		ns ns
t_h(H) t_h(L)	Hold time, High or Low SI/O to $\overline{CP}$	Waveform 2	1.5 1.5			2.0 2.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low Dn to $\overline{CP}$	Waveform 2	1.5 1.0			2.0 1.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to $\overline{CP}$	Waveform 2	3.0 4.0			3.0 4.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low M to $\overline{CP}$	Waveform 2	2.0 5.5			2.5 6.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low M to $\overline{CP}$	Waveform 2	0.0 0.0			1.0 1.0		ns ns
t_s(L)	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	8.0			9.0		ns
t_h(H)	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	0.0			0.0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width, High or Low	Waveform 1	3.5 4.5			4.0 5.0		ns ns

AC WAVEFORMS

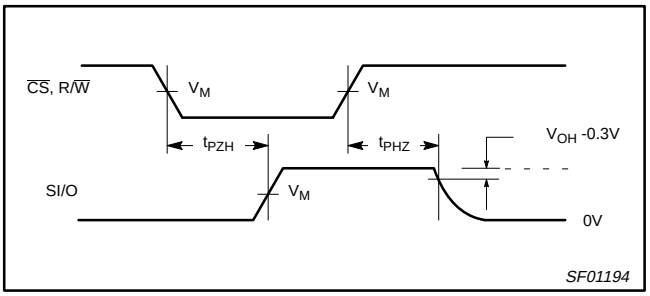
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



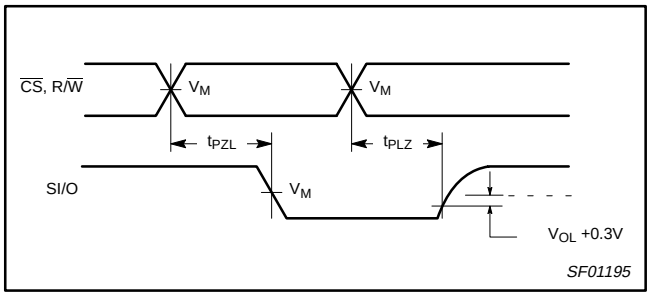
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Setup and Hold Times

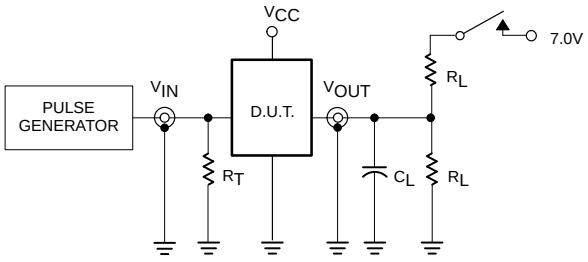


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

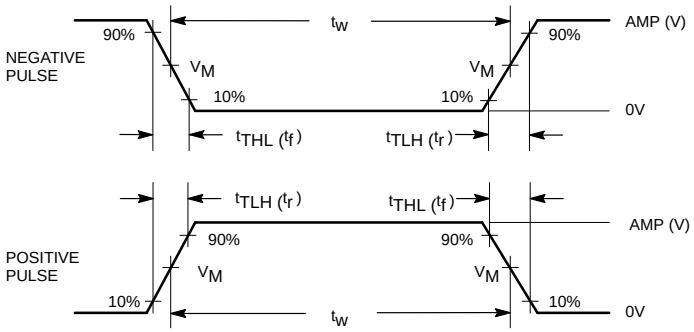
TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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