

# Register stack – 16×4 RAM 3-State output register

# 74F410

## FEATURES

- Edge triggered output register
- Typical access time of 19.5ns
- Optimize for register stack operation
- 3-state outputs
- 18-pin package

The 74F410 is fully compatible with all TTL families.

| TYPE   | TYPICAL ACCESS TIME | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|---------------------|--------------------------------|
| 74F410 | 19.5ns              | 45mA                           |

while  $\overline{WE}$ ,  $\overline{CS}$ , and CP are low, the contents of the selected memory location follow these changes provided setup and hold time criteria are met.

**Read operation** – When  $\overline{CS}$  is low,  $\overline{WE}$  is high, and CP goes from low-to-high, the contents of the memory location selected by the address inputs (A0–A3) are edge-triggered into the output register. When  $\overline{WE}$  is low,  $\overline{CS}$  is low, CP goes from low-to-high, the data at the data inputs is edge-triggered into the output register. The  $\overline{OE}$  input controls the output buffers. When  $\overline{OE}$  is high the four outputs (Q0–Q3) are in a high impedance or off state; when  $\overline{OE}$  is low, the outputs are determined by the state of the output register.

## DESCRIPTION

The 74F410 is a register oriented high speed 64-bit read/write memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility.

## FUNCTIONAL DESCRIPTION

**Write operation** – When the three control inputs, write enable ( $\overline{WE}$ ), chip select ( $\overline{CS}$ ), and clock (CP), are low the information on the data inputs (D0–D3) is written into the memory location selected by the address inputs (A0–A3). If the input data changes

## ORDERING INFORMATION

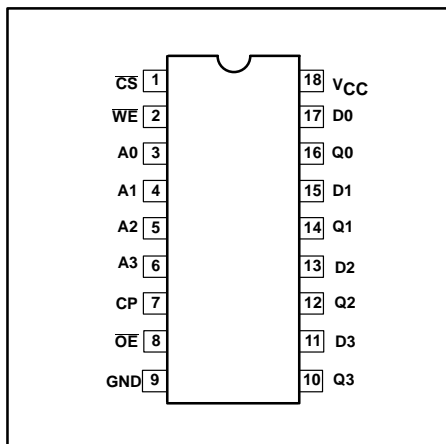
| DESCRIPTION                 | ORDER CODE  |
|-----------------------------|---|
|                             | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ |
| 18-pin plastic DIP (300mil) | N74F410N  |

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

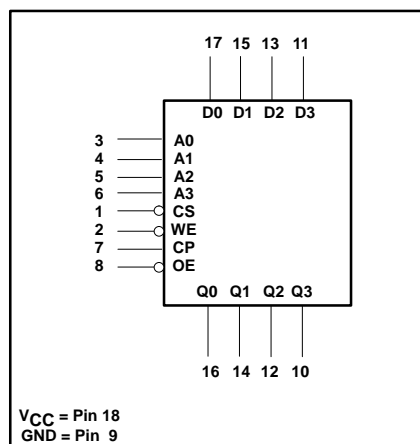
| PINS            | DESCRIPTION                            | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-----------------|--|---------------------|---------------------|
| D0 – D3         | Data inputs                            | 1.0/1.0             | 20µA/0.6mA          |
| A0 – A3         | Address inputs                         | 1.0/1.0             | 20µA/0.6mA          |
| CP              | Clock pulse input (active rising edge) | 1.0/2.0             | 20µA/1.2mA          |
| $\overline{CS}$ | Chip select input (active low)         | 1.0/2.0             | 20µA/1.2mA          |
| $\overline{OE}$ | Output enable input (active low)       | 1.0/1.0             | 20µA/0.6mA          |
| $\overline{WE}$ | Write enable input (active low)        | 1.0/1.0             | 20µA/0.6mA          |
| Q0 – Q3         | Data outputs                           | 150/40              | 3mA/24mA            |

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

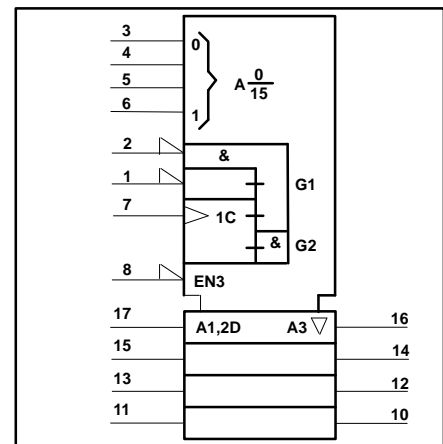
## PIN CONFIGURATION



## LOGIC SYMBOL



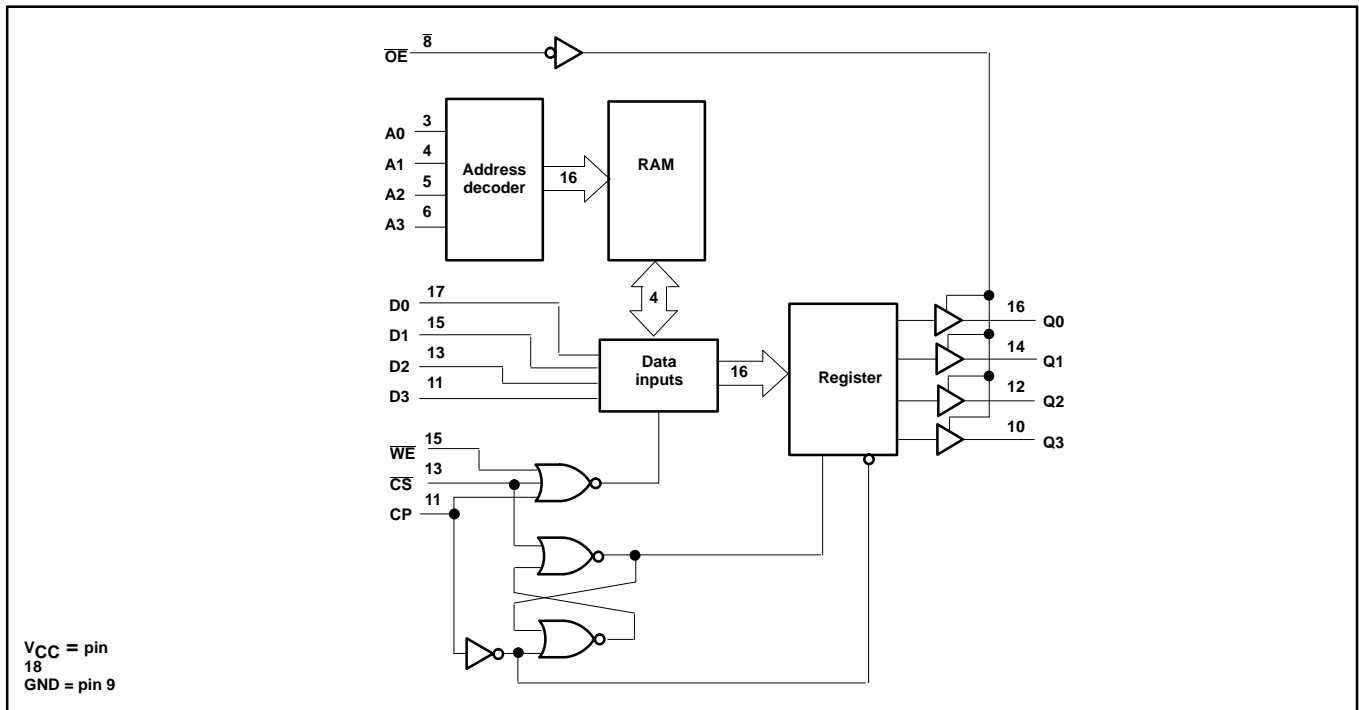
## IEC/IEEE SYMBOL



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## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL           | PARAMETER                                      | RATING                  | UNIT |
|------------------|--|-------------------------|------|
| V <sub>CC</sub>  | Supply voltage                                 | -0.5 to +7.0            | V    |
| V <sub>IN</sub>  | Input voltage                                  | -0.5 to +7.0            | V    |
| I <sub>IN</sub>  | Input current                                  | -30 to +5               | mA   |
| V <sub>OUT</sub> | Voltage applied to output in high output state | -0.5 to V <sub>CC</sub> | V    |
| I <sub>OUT</sub> | Current applied to output in low output state  | 48                      | mA   |
| T <sub>amb</sub> | Operating free air temperature range           | 0 to +70                | °C   |
| T <sub>stg</sub> | Storage temperature range                      | -65 to +150             | °C   |

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL           | PARAMETER                            | LIMITS |     |     | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
|                  |                                      | MIN    | NOM | MAX |      |
| V <sub>CC</sub>  | Supply voltage                       | 4.5    | 5.0 | 5.5 | V    |
| V <sub>IH</sub>  | High-level input voltage             | 2.0    |     |     | V    |
| V <sub>IL</sub>  | Low-level input voltage              |        |     | 0.8 | V    |
| I <sub>IK</sub>  | Input clamp current                  |        |     | -18 | mA   |
| I <sub>OH</sub>  | High-level output current            |        |     | -3  | mA   |
| I <sub>OL</sub>  | Low-level output current             |        |     | 24  | mA   |
| T <sub>amb</sub> | Operating free air temperature range | 0      |     | +70 | °C   |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL           | PARAMETER   | TEST CONDITIONS <sup>1</sup>                            | LIMITS              |                  |      | UNIT |   |
|------------------|---|---|---------------------|------------------|------|------|---|
|                  |   |   | MIN                 | TYP <sup>2</sup> | MAX  |      |   |
| V <sub>OH</sub>  | High-level output voltage                         | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX            | ±10%V <sub>CC</sub> | 2.4              |      | V    |   |
|                  |   | V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX            | ±5%V <sub>CC</sub>  | 2.7              |      | V    |   |
| V <sub>OL</sub>  | Low-level output voltage                          | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX            | ±10%V <sub>CC</sub> |                  | 0.35 | 0.50 | V |
|                  |   | V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX            | ±5%V <sub>CC</sub>  |                  | 0.35 | 0.50 | V |
| V <sub>IK</sub>  | Input clamp voltage                               | V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub> |                     | -0.73            | -1.2 | V    |   |
| I <sub>I</sub>   | Input current at maximum input voltage            | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V            |                     |                  | 100  | μA   |   |
| I <sub>IH</sub>  | High-level input current                          | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V            |                     |                  | 20   | μA   |   |
| I <sub>IL</sub>  | Low-level input current                           | others<br>CP, $\overline{CS}$                           |                     |                  | -0.6 | mA   |   |
|                  |   |   |                     |                  | -1.2 | mA   |   |
| I <sub>OZH</sub> | Offset-output current, high-level voltage applied | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V            |                     |                  | 50   | μA   |   |
| I <sub>OZL</sub> | Offset-output current, low-level voltage applied  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V            |                     |                  | -50  | μA   |   |
| I <sub>OS</sub>  | Short-circuit output current <sup>3</sup>         | V <sub>CC</sub> = MAX                                   |                     | -60              | -150 | mA   |   |
| I <sub>CC</sub>  | Supply current (total)                            | V <sub>CC</sub> = MAX                                   |                     | 45               | 70   | mA   |   |

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

| SYMBOL                               | PARAMETER                       | TEST CONDITION | LIMITS  |            |            |  |             | UNIT |
|--------------------------------------|---------------------------------|----------------|---|------------|------------|--|-------------|------|
|                                      |                                 |                | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |            | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |      |
|                                      |                                 |                | MIN   | TYP        | MAX        | MIN  | MAX         |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>CP to Qn   | Waveform 1     | 4.0<br>4.5  | 6.5<br>6.5 | 8.5<br>9.0 | 3.5<br>4.0   | 9.5<br>10.0 | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>OE to Qn  | Waveform 3, 4  | 3.0<br>4.5  | 4.5<br>6.0 | 7.5<br>9.0 | 2.5<br>3.5   | 8.5<br>9.5  | ns   |
| t <sub>PHZ</sub><br>t <sub>PHL</sub> | Output disable time<br>OE to Qn | Waveform 3, 4  | 2.0<br>2.0  | 3.5<br>3.5 | 6.0<br>6.5 | 1.5<br>2.0   | 6.5<br>7.0  | ns   |

## AC SETUP REQUIREMENTS FOR READ MODE

| SYMBOL                                   | PARAMETER  | TEST CONDITION | LIMITS  |     |     |  |     | UNIT |
|--|--|----------------|---|-----|-----|--|-----|------|
|  |  |                | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |      |
|  |  |                | MIN   | TYP | MAX | MIN  | MAX |      |
| t <sub>su(L)</sub>                       | Setup time, low, $\overline{CS}$ to CP <sup>1</sup>  | Waveform 1     | 4.0   |     |     | 4.5  |     | ns   |
| t <sub>h(L)</sub>                        | Hold time, low, $\overline{CS}$ to CP <sup>1</sup>   | Waveform 1     | 3.5   |     |     | 4.5  |     | ns   |
| t <sub>su(H)</sub><br>t <sub>su(L)</sub> | Setup time, high or low<br>An to CP <sup>1</sup>     | Waveform 1     | 13.0<br>13.0  |     |     | 15.0<br>15.0   |     | ns   |
| t <sub>h(H)</sub><br>t <sub>h(L)</sub>   | Hold time, high or low<br>An to CP <sup>1</sup>      | Waveform 1     | 0<br>0  |     |     | 0<br>0   |     | ns   |
| t <sub>su(H)</sub>                       | Setup time, high, $\overline{WE}$ to CP <sup>1</sup> | Waveform 1     | 13.0  |     |     | 15.0   |     | ns   |
| t <sub>h(H)</sub>                        | Hold time, high, $\overline{WE}$ to CP <sup>1</sup>  | Waveform 1     | 0   |     |     | 0  |     | ns   |
| t <sub>w(L)</sub>                        | CP pulse width, low                                  | Waveform 1     | 5.0   |     |     | 6.0  |     | ns   |

## NOTE:

1. Low-to-high clock transition.

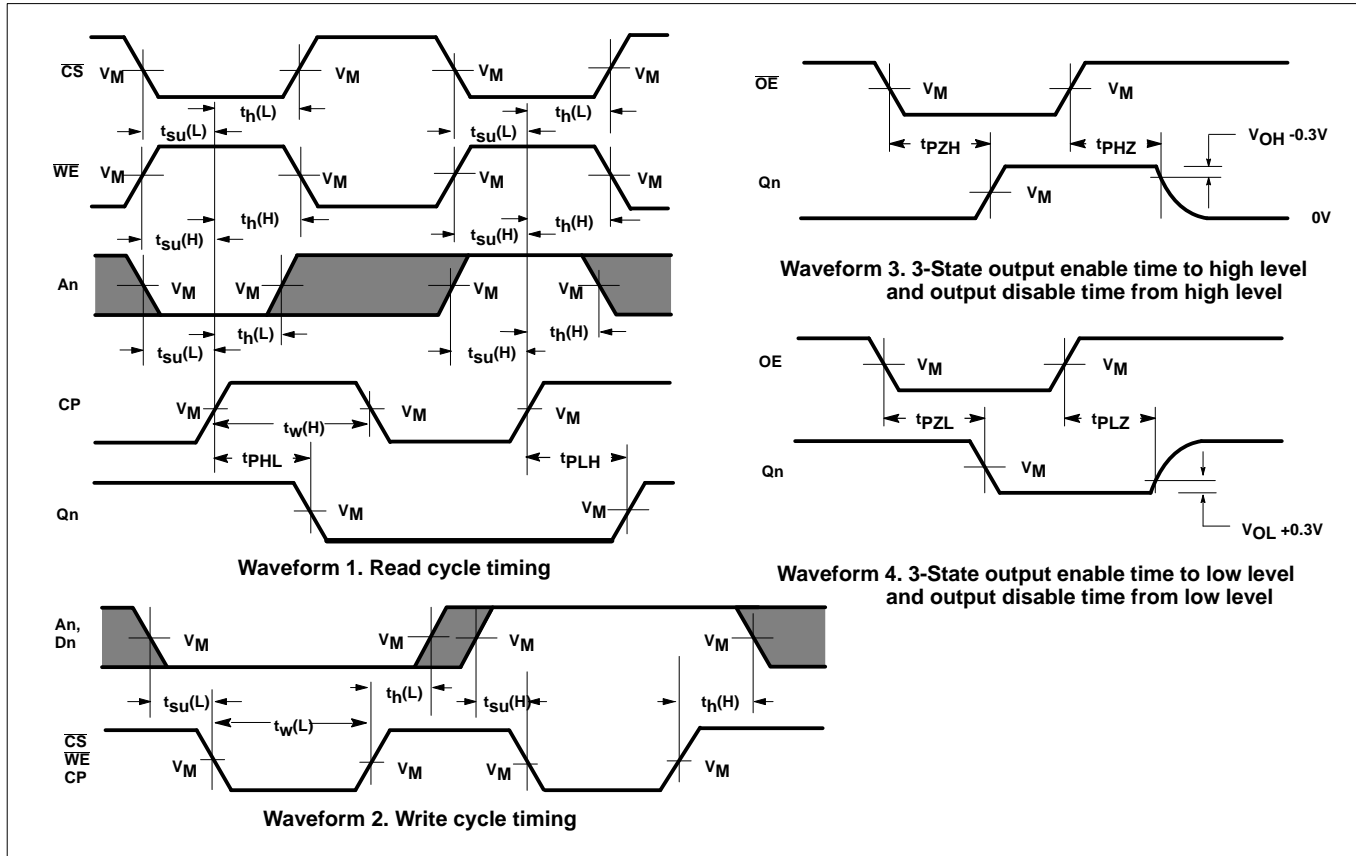
## AC SETUP REQUIREMENTS FOR WRITE MODE

| SYMBOL                                   | PARAMETER   | TEST CONDITION | LIMITS  |     |     |  |     | UNIT |
|--|---|----------------|---|-----|-----|--|-----|------|
|  |   |                | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |      |
|  |   |                | MIN   | TYP | MAX | MIN  | MAX |      |
| t <sub>su(H)</sub><br>t <sub>su(L)</sub> | Setup time, high or low<br>An to $\overline{WE}$ , $\overline{CS}$ , CP | Waveform 2     | 0<br>0  |     |     | 0<br>0   |     | ns   |
| t <sub>h(H)</sub><br>t <sub>h(L)</sub>   | Hold time, high or low<br>An to $\overline{WE}$ , $\overline{CS}$ , CP  | Waveform 2     | 0<br>0  |     |     | 0<br>0   |     | ns   |
| t <sub>su(H)</sub><br>t <sub>su(L)</sub> | Setup time, high or low<br>Dn to $\overline{WE}$ , $\overline{CS}$ , CP | Waveform 2     | 6.0<br>6.0  |     |     | 8.0<br>8.0   |     | ns   |
| t <sub>h(H)</sub><br>t <sub>h(L)</sub>   | Hold time, high or low<br>Dn to $\overline{WE}$ , $\overline{CS}$ , CP  | Waveform 2     | 0<br>0  |     |     | 0<br>0   |     | ns   |
| t <sub>w(L)</sub>                        | $\overline{WE}$ pulse width, low  | Waveform 2     | 7.0   |     |     | 8.0  |     | ns   |
| t <sub>w(L)</sub>                        | $\overline{CS}$ pulse width, low  | Waveform 2     | 6.0   |     |     | 7.0  |     | ns   |
| t <sub>w(L)</sub>                        | CP pulse width, low   | Waveform 2     | 7.0   |     |     | 8.0  |     | ns   |

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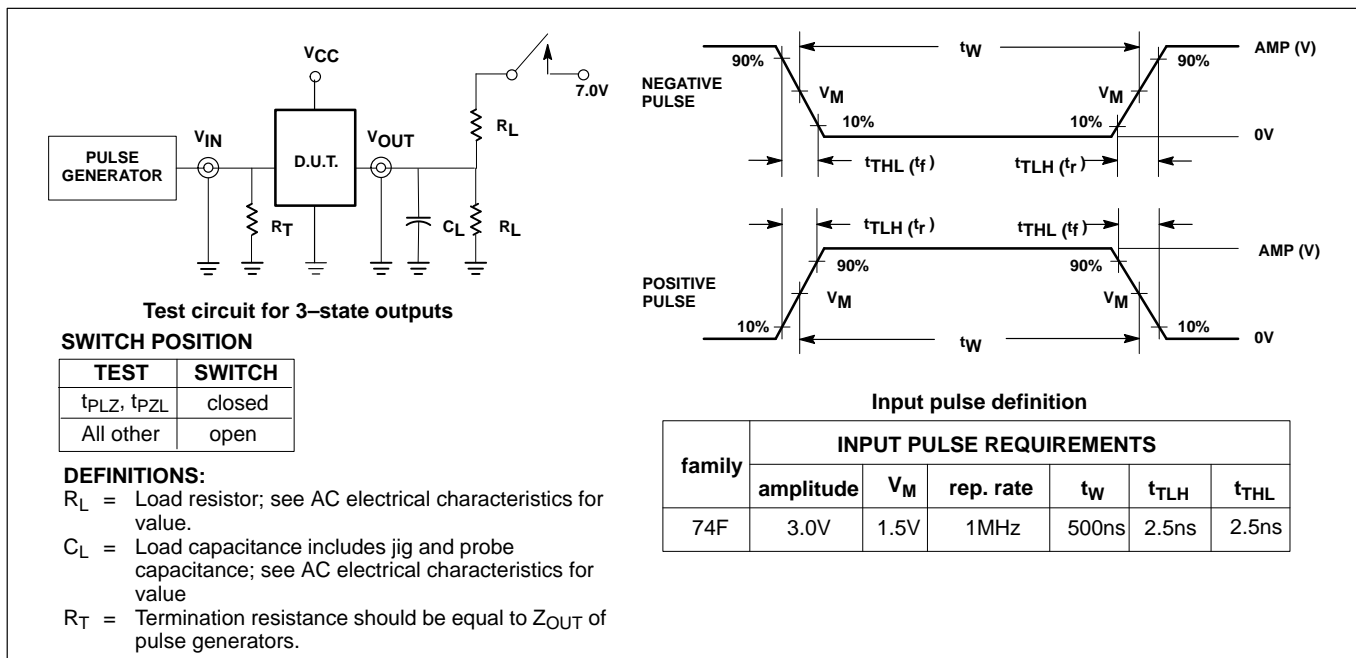
## AC WAVEFORMS



**NOTES:**

1. For all waveforms,  $V_M = 1.5V$ .
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORM





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