

DATA SHEET

74F379A Quad register

Product specification

1996 Mar 12

IC15 Data Handbook

Quad register

74F379A

FEATURES

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complementary outputs
- Offers light loading PNP inputs ($I_{IL} = -20\mu A$)

DESCRIPTION

The 74F379A is a 4-bit register with buffered common enable (\bar{E}). This device is similar to the 74F175A but features the common enable rather than common master reset.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379A	200MHz	29mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG, DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic DIP	N74F379AN	SOT38-4
16-pin plastic SO	N74F379AD	SOT109-1

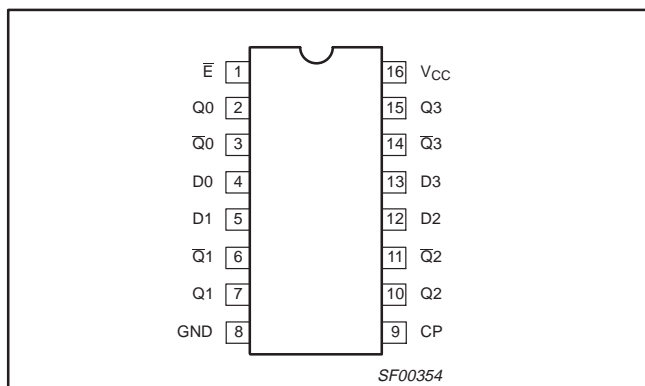
INPUT AND OUTPUT LOADING AND FAN OUT TABLE

TYPE	PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F379A	D0 – D3	Data inputs	1.0/0.033	20 μ A/20 μ A
	CP	Clock pulse input (active rising edge)	1.0/0.033	20 μ A/20 μ A
	\bar{E}	Enable input (active low)	1.0/0.033	20 μ A/20 μ A
	Q0 – Q3	True outputs	50/33	1.0mA/20mA
	$\bar{Q}0 – \bar{Q}3$	Complementary outputs	50/33	15mA/20mA

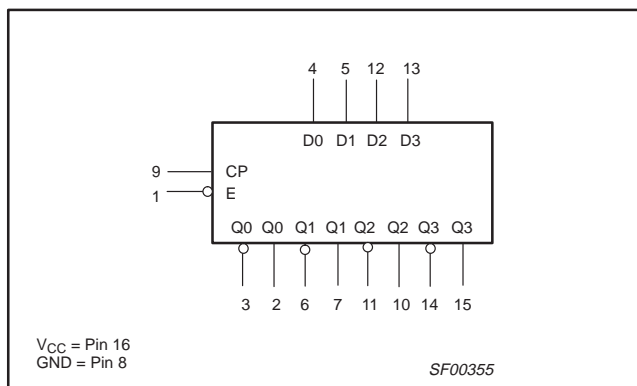
Note to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the low state.

PIN CONFIGURATION



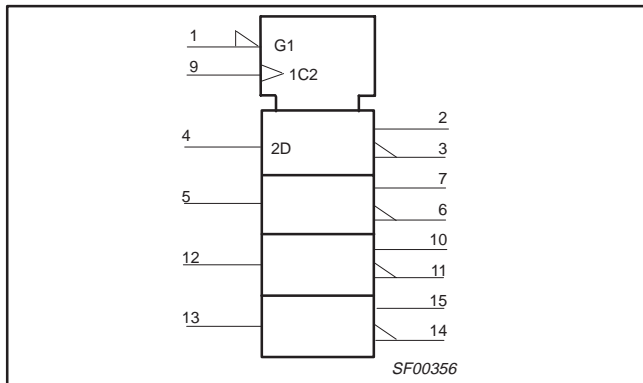
LOGIC SYMBOL



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IEC/IEEE SYMBOL



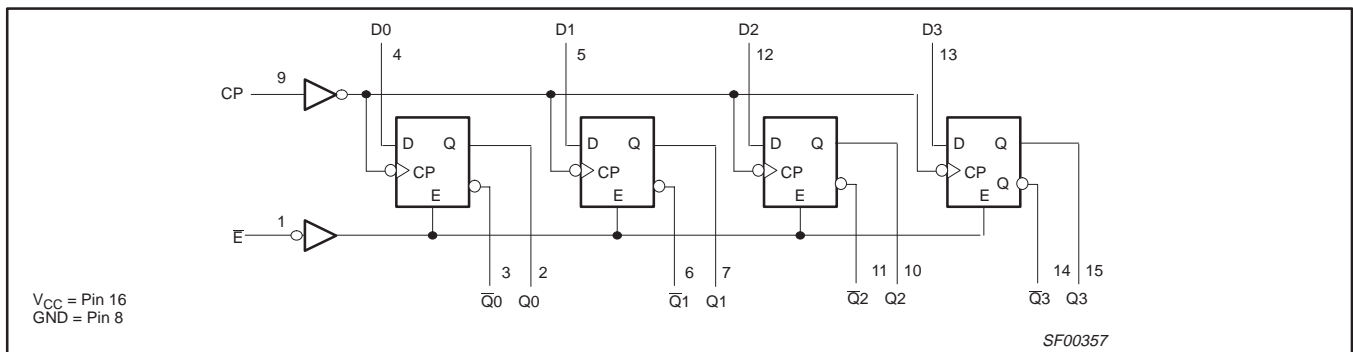
FUNCTION TABLE

INPUTS			OUTPUTS	OUTPUT
\bar{E}	CP	Dn	Qn	$\bar{Q}n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

Notes to function table

- H = High-voltage level
- h = High state must be present one setup time before the low-to-high clock transition
- L = Low-voltage level
- l = Low state must be present one setup time before the low-to-high clock transition
- NC= No change
- X = Don't care
- ↑ = Low-to-high clock transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in high output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state	40	mA
T _{amb}	Operating free air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.5		V
			±5%V _{CC}	2.7	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35 0.50	V
			±5%V _{CC}		0.35 0.50	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V
I _I	Input current at maximum input voltage	V _{CC} = 0.0V, V _I = 7.0V			100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	Low-level input current				-20	μA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-60		-150	mA
I _{CC}	Supply current (total)			29	42	mA

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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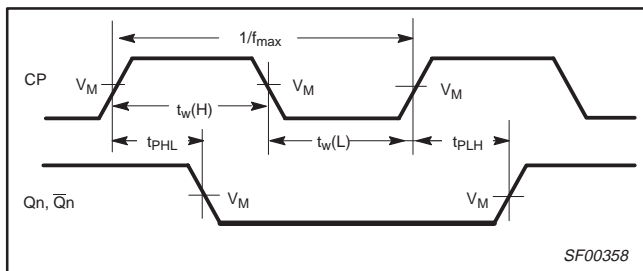
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{max}	Maximum clock frequency	Waveform 1	175	200		155		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn or Q̄n	Waveform 1	2.0 4.0	3.5 5.5	6.5 8.0	2.0 3.5	7.0 8.5	ns

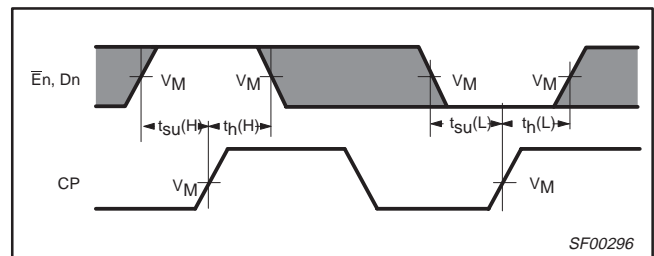
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, high or low level Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		ns
t _h (H) t _h (L)	Hold time, high or low level Dn to CP	Waveform 2	0 0			0 0		ns
t _{su} (H) t _{su} (L)	Setup time, high or low level E to CP	Waveform 2	4.0 3.5			4.5 4.0		ns
t _h (H) t _h (L)	Hold time, high or low level E to CP	Waveform 2	0 0			0 0		ns
t _w (H) t _w (L)	CP Pulse width, high or low	Waveform 1	3.5 4.5			3.5 4.5		ns

AC WAVEFORMS



Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Data and enable setup time and hold times

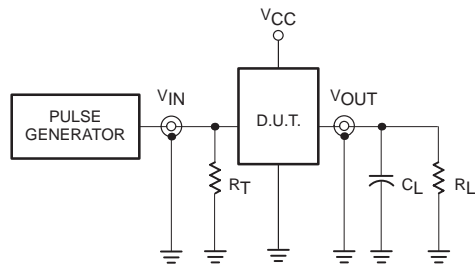
Notes to AC waveforms

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

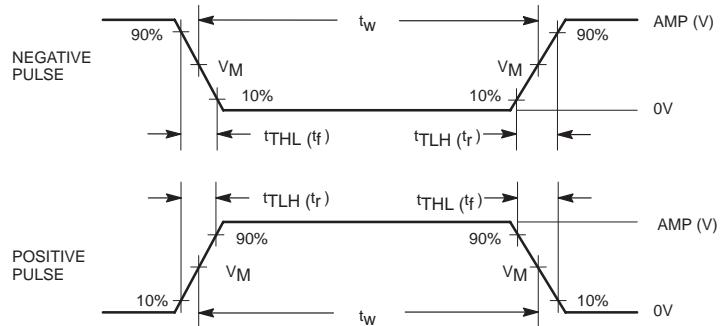
Quad register

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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

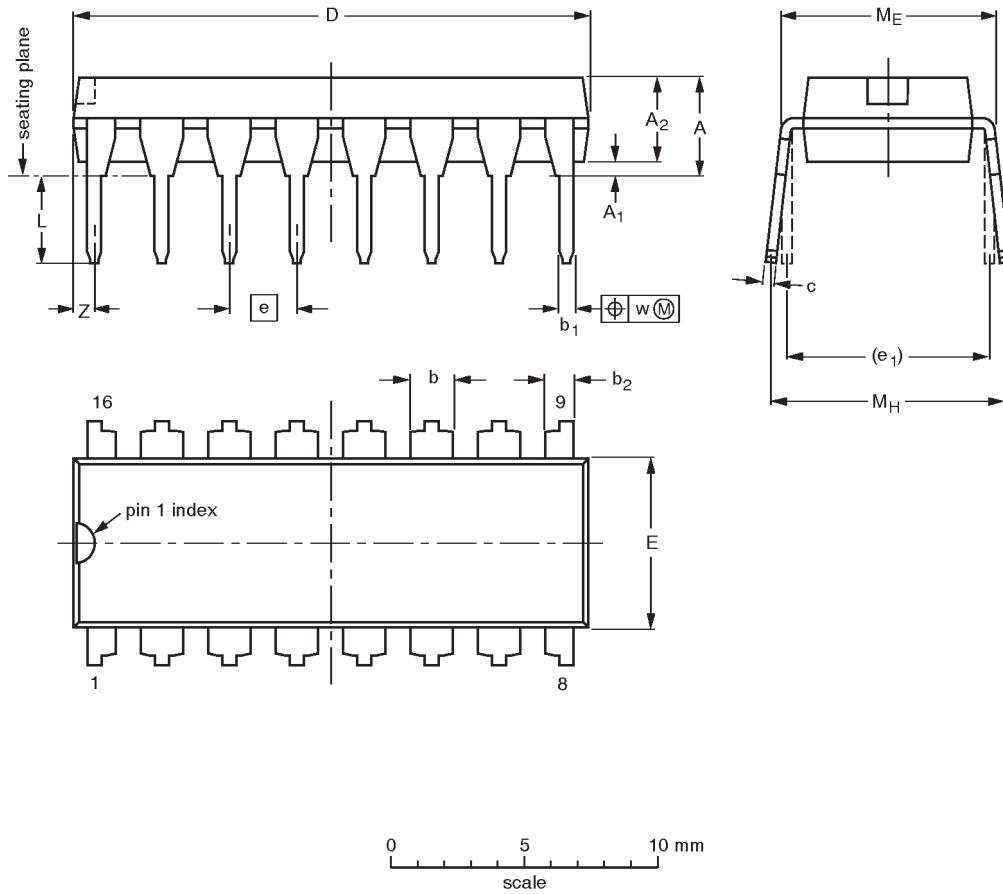
SF00006

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

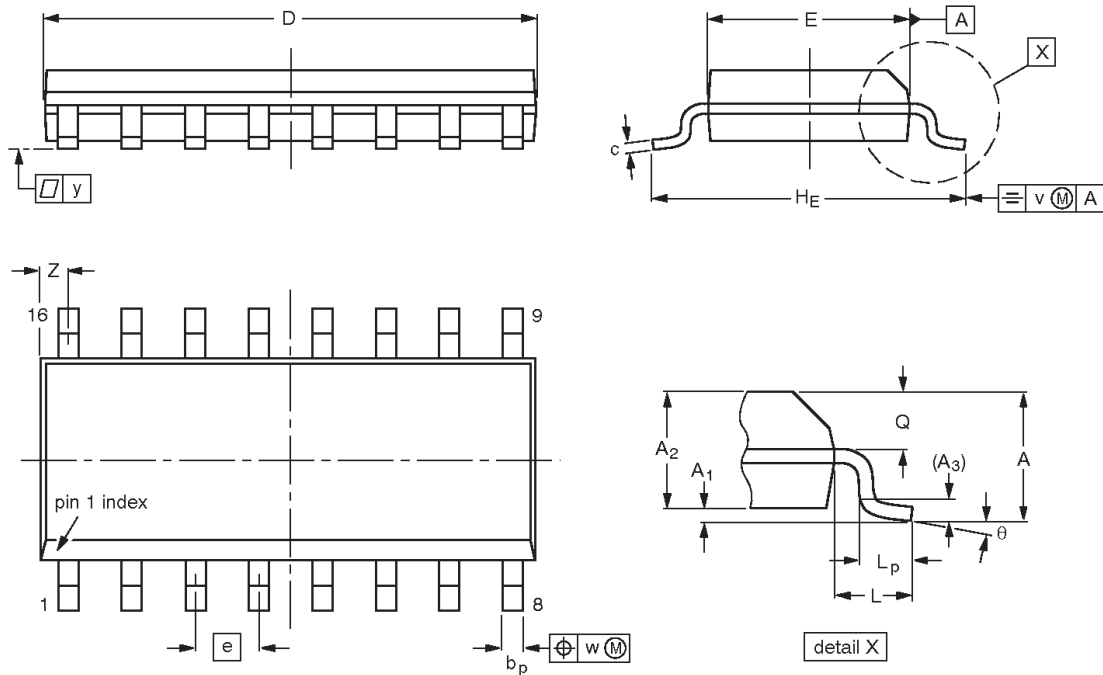
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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