

74F2645 Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

General Description

This device is an octal bus transceiver designed for asynchronous two-way data flow between the A and B busses and is functionally equivalent to the 74F645. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, have 3-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive (T/R) input. The 74F2645 is a low power version of the 74F245 with 25Ω series resistors in the outputs.

Features

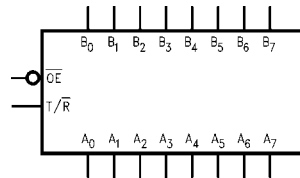
- 25Ω series resistors in the outputs eliminates the need for external resistors
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Transmit/receive (T/R) input controls the direction of data flow
- 74F2645 is a low power version of the 74F245 with 25Ω series resistors in the outputs

Ordering Code:

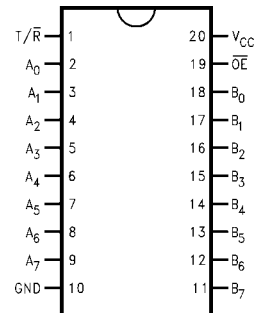
Order Number	Package Number	Package Description
74F2645SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



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Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
\overline{OE}	Output Enable Input (Active LOW)	1.0/1.0	20 μ A/-0.6 mA
T/\overline{R}	Transmit/Receive Input	1.0/1.0	20 μ A/-0.6 mA
A_0 - A_7	Side A Inputs or 3-STATE Outputs	3.5/0.667	70 μ A/-0.4 mA
B_0 - B_7	Side B Inputs or 3-STATE Outputs	3.5/0.667	70 μ A/-0.4 mA
		750/20	-15 mA/12 mA

Functional Description

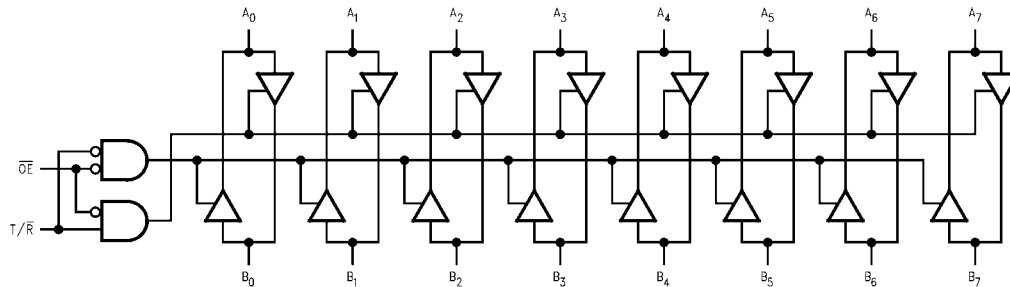
The output enable (\overline{OE}) is active LOW. If the device is disabled (\overline{OE} HIGH), the outputs are in the high impedance state. The transmit/receive input (T/\overline{R}) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When T/\overline{R} is LOW, B data is sent to the A bus. If T/\overline{R} is HIGH, A data is sent to the B bus.

Function Table

Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance State

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

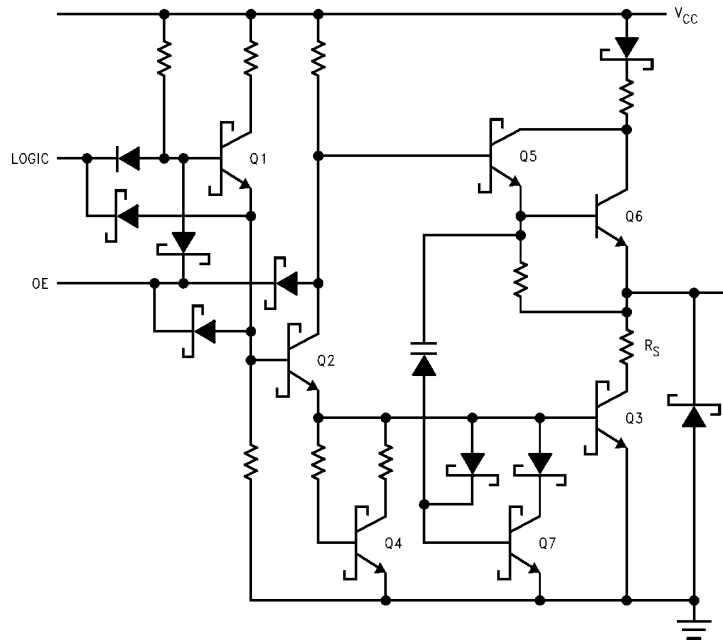
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage 10% V _{CC}	2.0			V	Min	I _{OH} = -15 mA (A _n , B _n)
V _{OL}	Output LOW Voltage 10% V _{CC}			0.50 0.75	V	Min	I _{OL} = 1 mA (A _n , B _n) I _{OL} = 12 mA (A _n , B _n)
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V (Non I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (Non I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25
I _{CCL}	Power Supply Current (74F2645)			82	mA	Max	V _O = LOW, V _{IN} = 0.2V
I _{CCZ}	Power Supply Current (74F2645)			95	mA	Max	V _O = HIGH Z

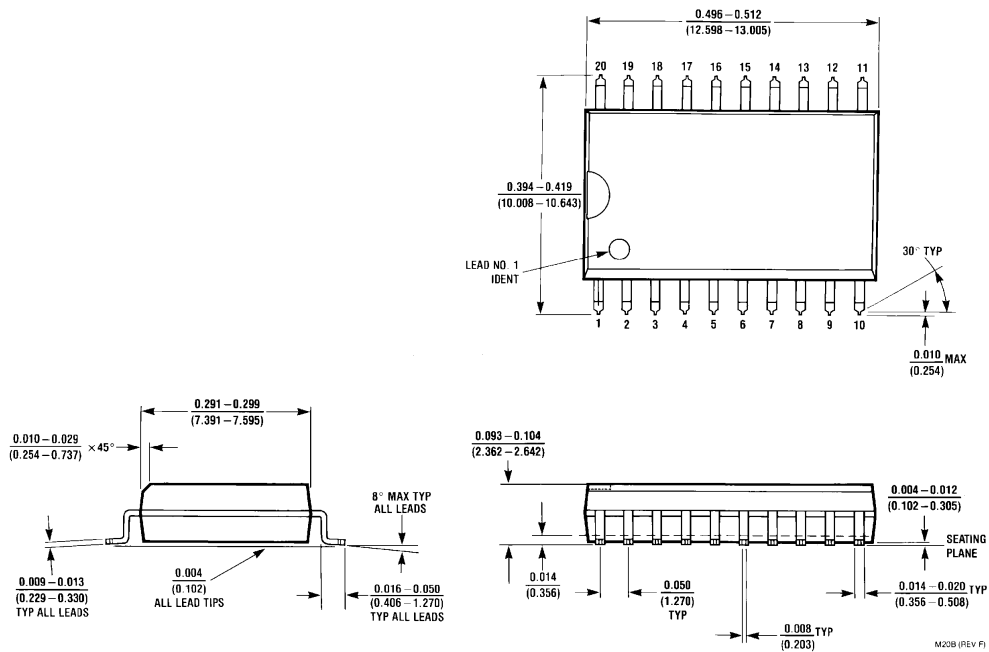
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay A Input to B Output	1.5		6.0	1.5	7.0	ns
t_{PHL}	A Input to B Output	2.5		7.5	2.5	8.0	
t_{PLH}	Propagation Delay B Input to A Output	1.5		6.0	1.5	7.0	ns
t_{PHL}	B Input to A Output	2.5		7.5	2.5	8.0	
t_{PZH}	Enable Time OE Input to A Output	2.5		8.0	2.0	9.0	ns
t_{PZL}	OE Input to A Output	2.5		8.5	2.0	8.5	
t_{PHZ}	Disable Time OE Input to A Output	1.5		7.0	1.0	8.0	ns
t_{PLZ}	OE Input to A Output	1.0		5.5	1.0	5.5	
t_{PZH}	Enable Time OE Input to B Output	2.5		7.5	2.0	9.5	ns
t_{PZL}	OE Input to B Output	2.5		8.5	2.5	9.0	
t_{PHZ}	Disable Time OE Input to B Output	1.5		6.5	1.0	7.5	ns
t_{PLZ}	OE Input to B Output	1.0		6.5	1.0	6.5	

Basic FAST Circuit Showing Series Resistor Placement



Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

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