DATA SHEET

74F195A
4-bit parallel-access shift register

Product specification

1996 Mar 12

IC15 Data Handbook

Philips
Semiconductors

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4-bit parallel-access shift register 74F195A

FEATURES

- Shift right and parallel load capability
- J – $\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset
- Diode inputs

DESCRIPTION

The 74F195A is a 4-Bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic Diagram and Function Table. This device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195A operates in two primary modes: shift right (Q0→Q1) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction Q0→Q1→Q2→Q3 following each Low-to-High clock transition.

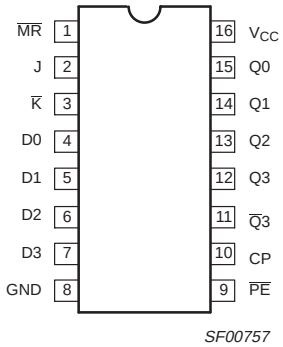
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D0–D3) is transferred to the respective Q0–Q3 outputs. Shift left operation (Q3–Q2) can be achieved by tying the Qn outputs to the Dn-1 inputs and holding the $\overline{PE}$ input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195A utilizes edge-triggering, therefore there is no restriction on the activity of the J, $\overline{K}$, Dn, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195A	180MHz	40mA

ORDERING INFORMATION

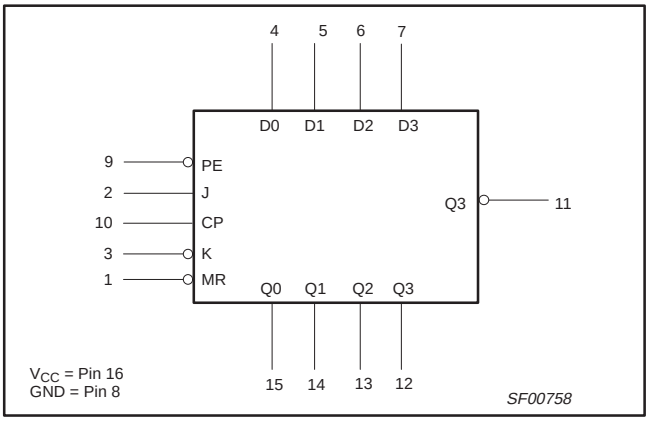
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG. DWG. #
16-pin plastic DIP	N74F195AN	SOT 38-4
16-pin plastic SO	N74F195AD	SOT 109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

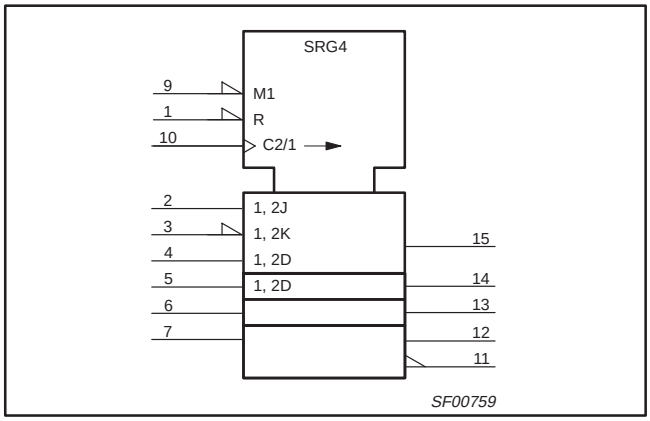
PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Data inputs	74F195	1.0/0.033	20µA/20µA
		74F195A	1.0/1.0	20µA/0.6mA
J, $\overline{K}$	J-K or D type serial inputs	74F195	1.0/0.033	20µA/20µA
		74F195A	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	74F195	1.0/0.033	20µA/20µA
		74F195A	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	74F195	2.0/0.066	40µA/40µA
		74F195A	1.0/1.0	20µA/0.6mA
Q0–Q3, $\overline{Q3}$	Data outputs		50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

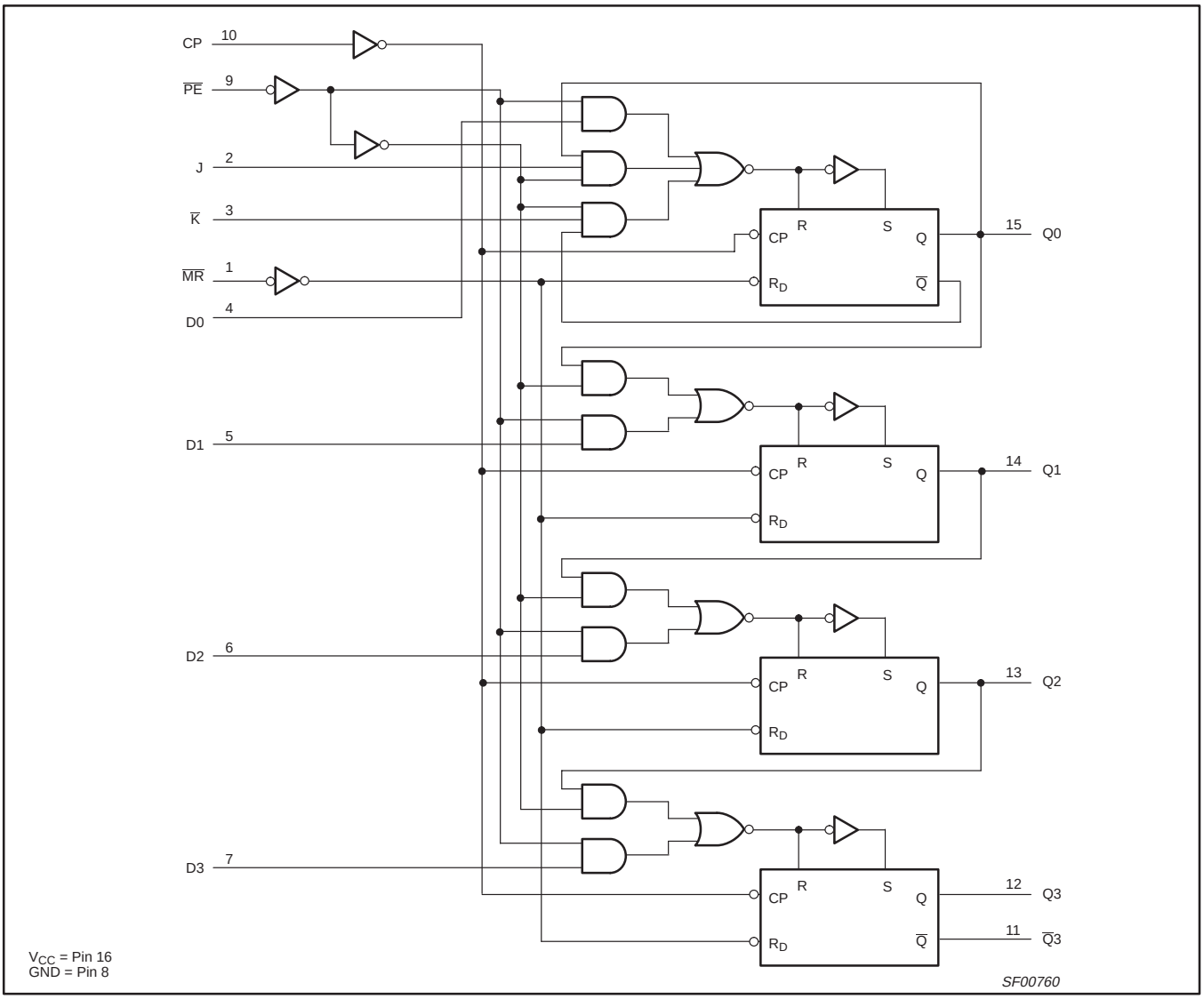
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	Dn	Q0	Q1	Q2	Q3	$\overline{Q}$3	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q0	q1	q2	$\overline{q}$2	Shift, set First stage
H	↑	h	l	l	X	L	q0	q1	q2	$\overline{q}$2	Shift, reset First stage
H	↑	h	h	l	X	$\overline{q}$0	q0	q1	q2	$\overline{q}$2	Shift, toggle First stage
H	↑	h	l	h	X	q0	q0	q1	q2	$\overline{q}$2	Shift, retain First stage

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[NO TAG]		LIMITS			UNIT
				MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	74F195A			100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	all others			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	74F195A			–600	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	74F195A		40	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Load mode	Waveform NO TAG	165	180		150		MHz
		Shift mode		180	190		170		
t_{PLH} t_{PHL}	Propagation delay CP to Qn		Waveform NO TAG	3.0 2.5	5.0 4.0	9.5 7.0	2.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}$3		Waveform NO TAG	2.0 2.0	5.5 4.0	9.5 6.5	2.5 2.0	9.5 7.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Qn		Waveform 2	2.0	4.0	7.0	2.0	7.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}$3		Waveform 2	2.5	4.5	8.0	2.0	10.0	ns

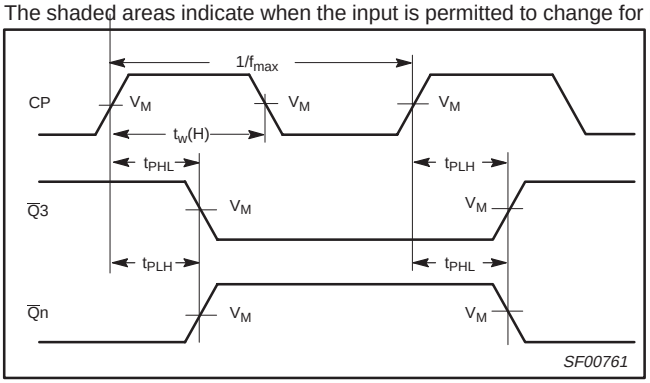
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_S(H)$ $t_S(L)$	Setup time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	2.5 2.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and Dn to CP	Waveform 3	0.0 1.0			0.0 1.0		ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	2.0 2.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_W(H)$	CP Pulse width High	Waveform NO TAG	4.5			4.5		ns
$t_W(L)$	$\overline{MR}$ Pulse width Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	2.5			3.0		ns

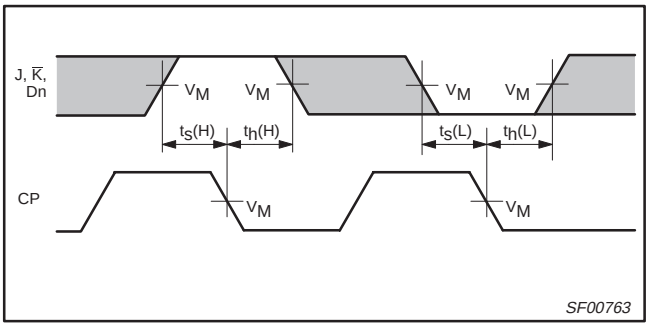
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

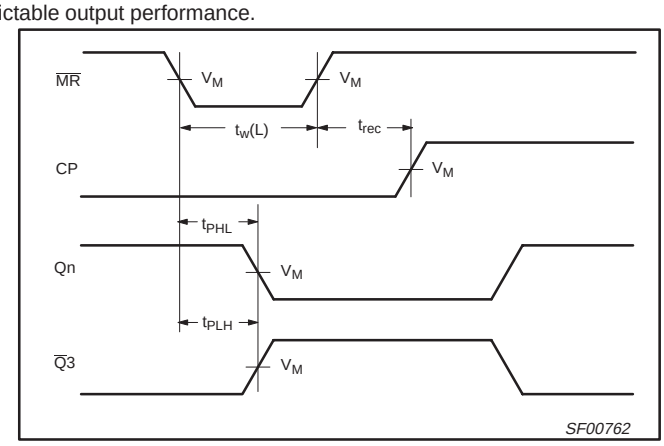
The shaded areas indicate when the input is permitted to change for predictable output performance.



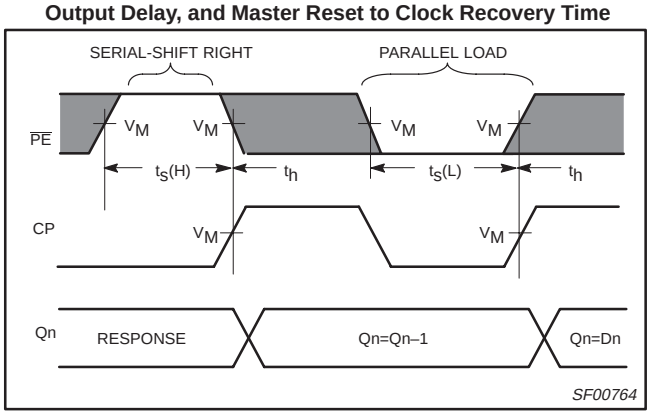
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

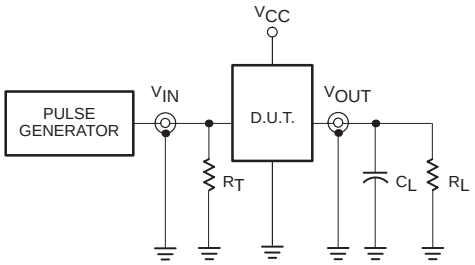


Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

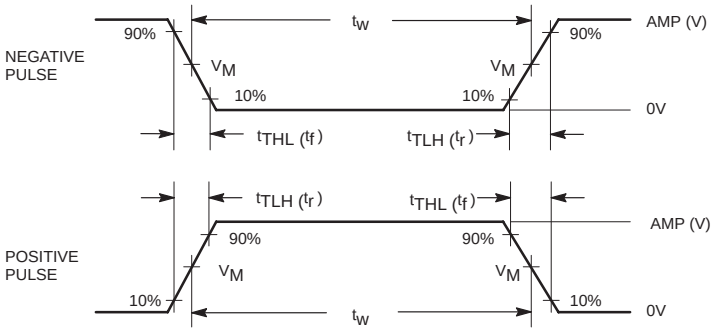


Waveform 4. Setup and Hold Times, Parallel Enable to Clock

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

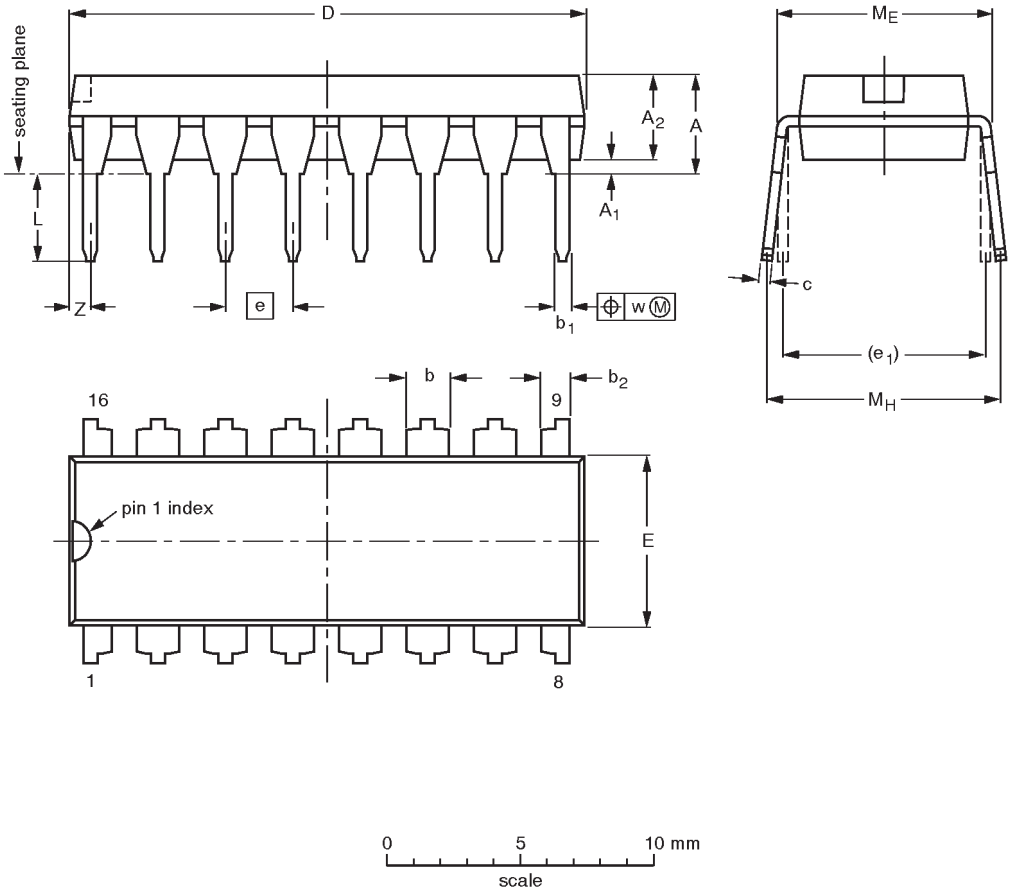
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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