

# DATA SHEET

## **74F189A**

64-bit TTL bipolar RAM, inverting  
(3-State)

Product specification

1990 Feb 23

IC15 Data Handbook

# 64-bit TTL bipolar RAM, inverting (3-State)

# 74F189A

## FEATURES

- High speed performance
- Replaces 74F189
- Address access time: 8ns max vs 28ns for 74F189
- Power dissipation: 4.3mW/bit
- Schottky clamp TTL
- One chip enable
- Inverting outputs (for non-inverting outputs see 74F219A)
- 3-State outputs
- 74F189A in 150 mil wide SO is preferred options for new designs

are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ( $\overline{CE}$ ) is high. The outputs are active only in the READ mode ( $\overline{WE}$  = high) and the output data is the complement of the stored data.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT ( TOTAL)
74F189A	5.0ns	55mA

## DESCRIPTION

The 74F189A is a high speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and

## ORDERING INFORMATION

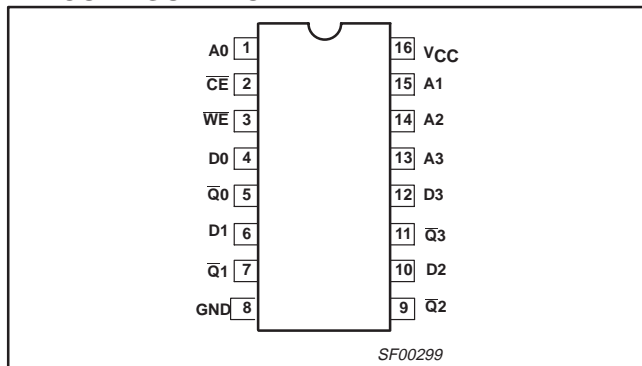
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic Dual In-line Package	N74F189AN	SOT38-4
16-pin plastic Small Outline (150mil)	N74F189AD	SOT109-1

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

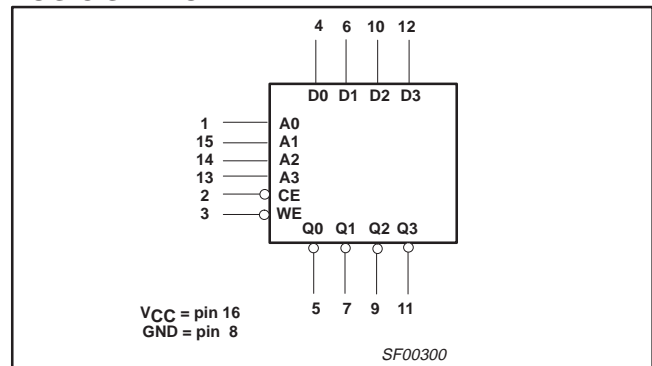
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
A0 – A3	Address inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20 $\mu$ A/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20 $\mu$ A/1.2mA
$\overline{Q0} - \overline{Q3}$	Data outputs	150/40	3mA/24mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the high state and 0.6mA in the low state.

## PIN CONFIGURATION



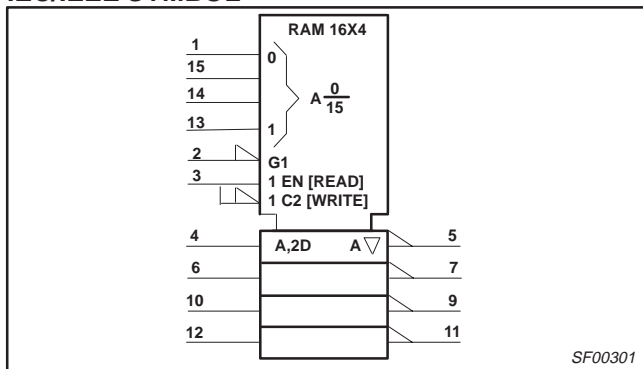
## LOGIC SYMBOL



# 64-bit TTL bipolar RAM, inverting (3-State)

# 74F189A

### IEC/IEEE SYMBOL

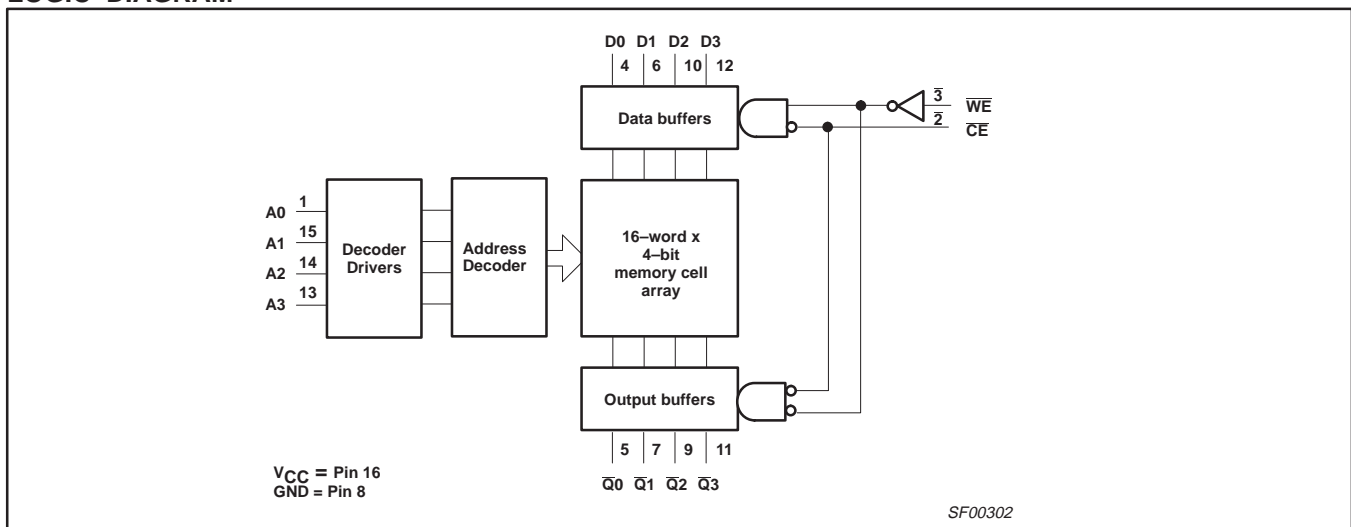


### FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	$D_n$	$\overline{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
H	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

**NOTES:**  
 H = High voltage level  
 L = Low voltage level  
 X = Don't care

### LOGIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in high output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in low output state	48	mA
$T_{amb}$	Operating free air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	$T_A = -40$ to $+85^\circ\text{C}$
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free air temperature range	0		+70	$^\circ\text{C}$

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V	
			$\pm 5\%V_{CC}$	2.7	3.4	V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
			$\pm 5\%V_{CC}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	$\mu\text{A}$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	$\mu\text{A}$	
$I_{IL}$	Low-level input current	others CE, WE	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-0.6	mA
							-1.2
$I_{OZH}$	Offset output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			50	$\mu\text{A}$	
$I_{OZL}$	Offset output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-50	$\mu\text{A}$	
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA	
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX}, \overline{\text{CE}} = \overline{\text{WE}} = \text{GND}$		55	80	mA	
$C_{IN}$	Input capacitance	$V_{CC} = 5\text{V}, V_{IN} = 2.0\text{V}$		4		pF	
$C_{OUT}$	Output capacitance	$V_{CC} = 5\text{V}, V_{OUT} = 2.0\text{V}$		7		pF	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

64-bit TTL bipolar RAM, inverting (3-State)

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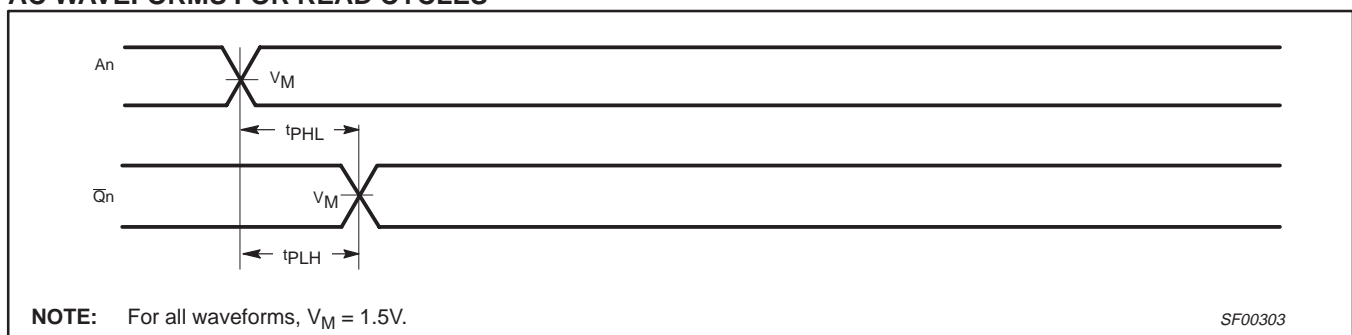
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Access time	Propagation delay An to Qn	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>		Enable time CE to Qn	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable time CE to Qn		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Write recovery time	Enable time WE to Qn	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable time WE to Qn		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns

AC SETUP REQUIREMENT

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>su(H)</sub> t <sub>su(L)</sub>	Setup time, high or low An to WE		Waveform 4	4.5 4.5			5.0 5.0		ns
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold time, high or low An to WE		Waveform 4	0 0			0 0		ns
t <sub>su(H)</sub> t <sub>su(L)</sub>	Setup time, high or low Dn to WE		Waveform 4	7.5 6.5			9.0 8.0		ns
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold time, high or low Dn to WE		Waveform 4	0 0			0 0		ns
t <sub>su(L)</sub>	Setup time, low CE (falling edge) to WE (falling edge)		Waveform 4	0			0		ns
t <sub>h(L)</sub>	Hold time, low WE (falling edge) to WE (rising edge)		Waveform 4	6.5			7.5		ns
t <sub>w(L)</sub>	Pulse width, low WE		Waveform 4	7.0			8.0		ns

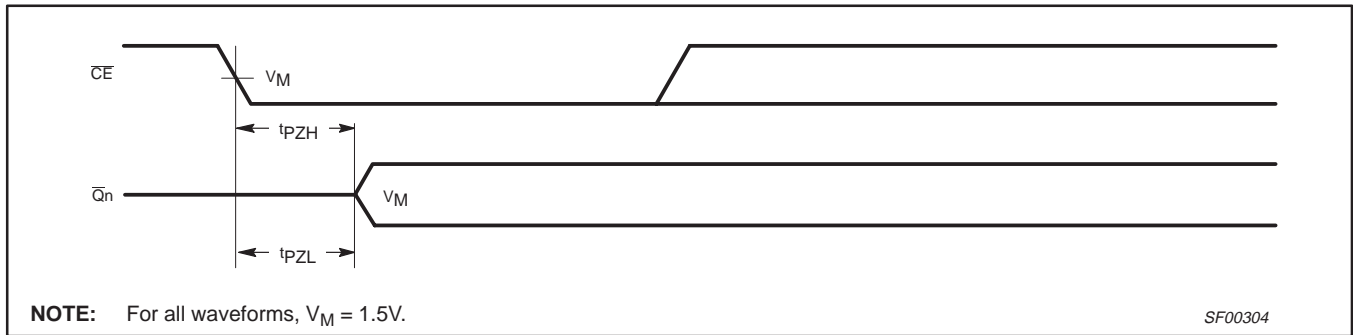
AC WAVEFORMS FOR READ CYCLES



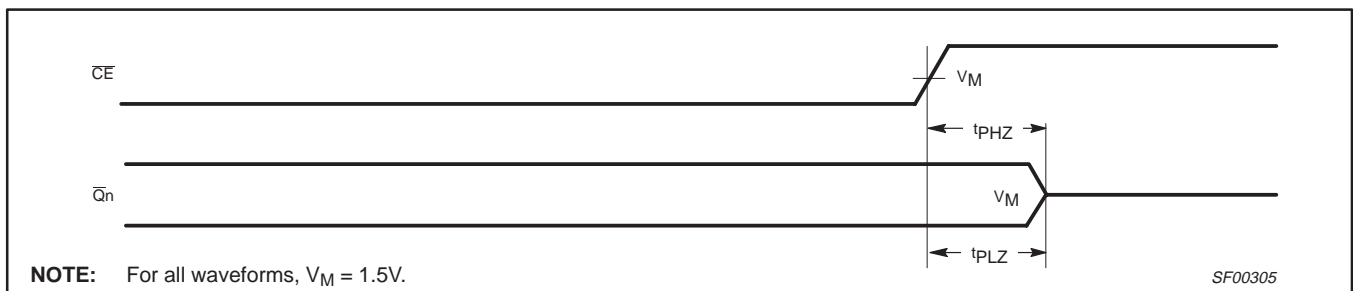
Waveform 1. Read cycle, address access time

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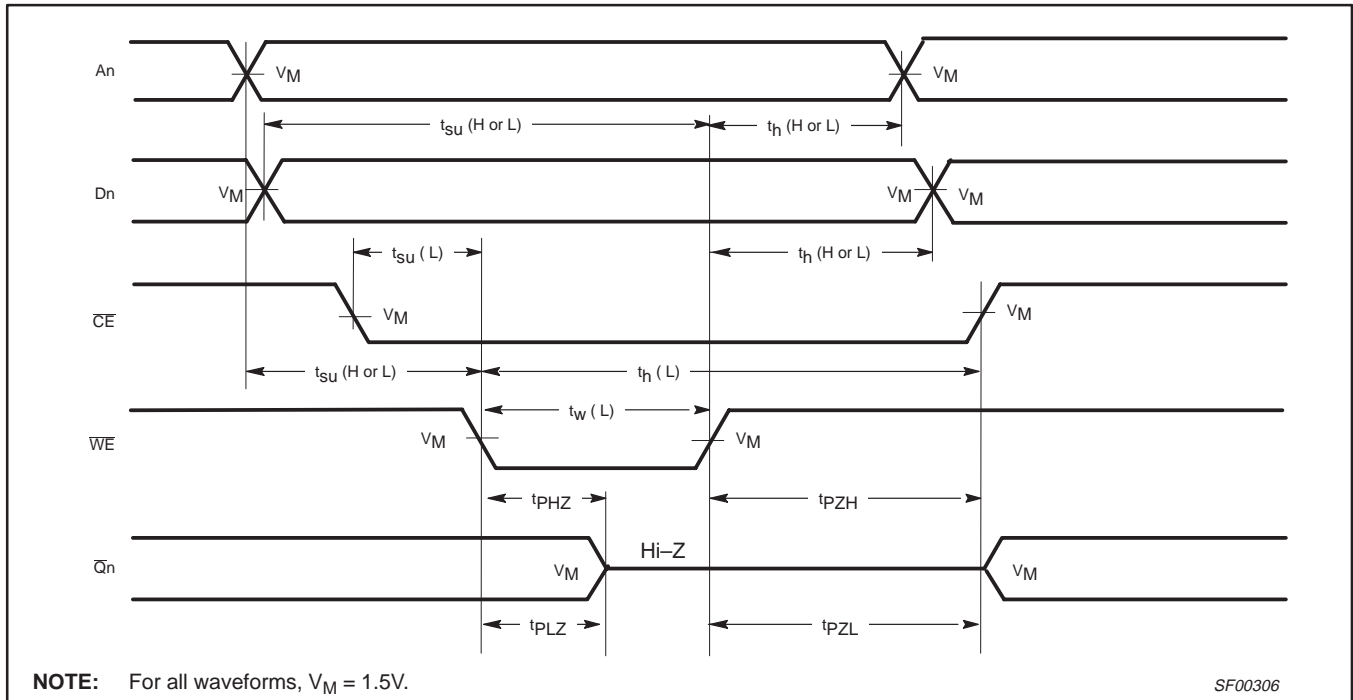


Waveform 2. Read cycle, chip enable access time



Waveform 3. Read cycle, chip disable time

AC WAVEFORMS FOR WRITE CYCLE

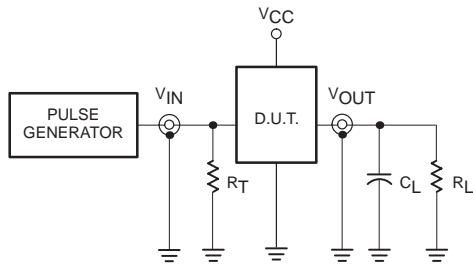


Waveform 4. Write cycle

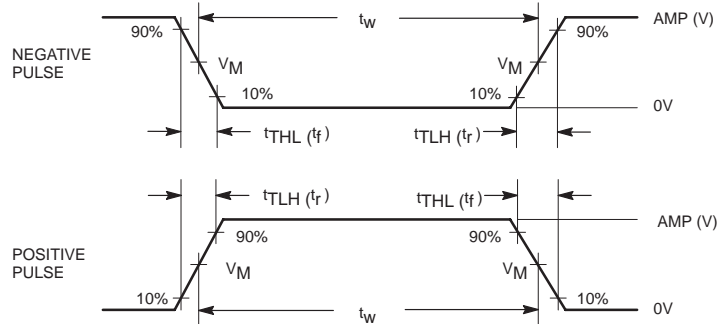
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TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

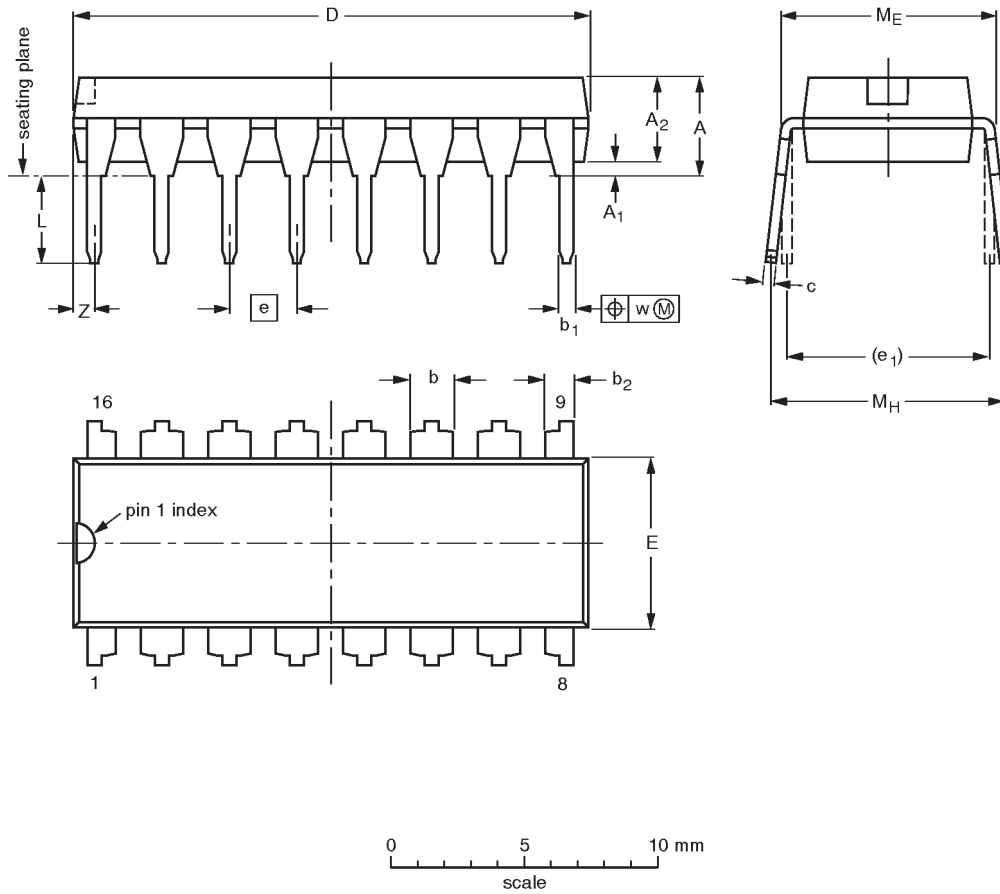
SF00006

64-bit TTL bipolar RAM, inverting (3-State)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

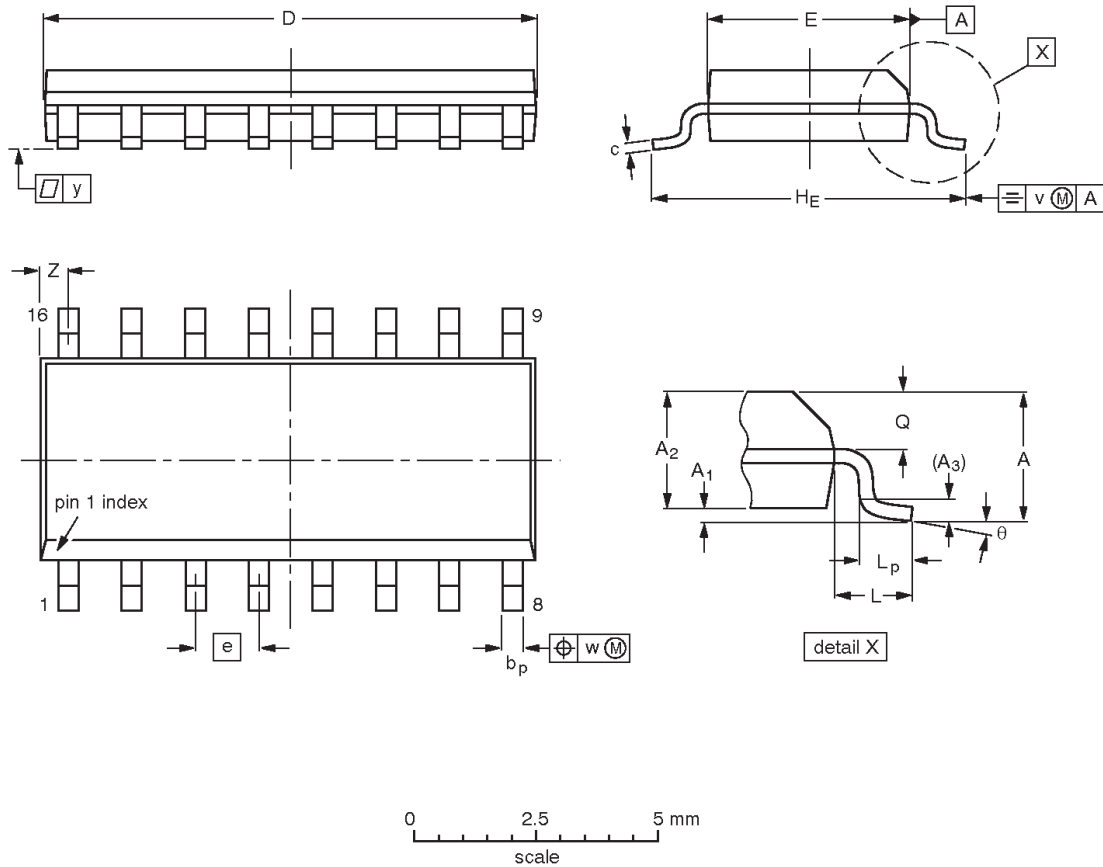
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	1.75 0.10	0.25 1.25	1.45 0.049	0.25 0.019	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.014	0.01 0.0075	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07S	MS-012AC			95-01-23 97-05-22

## 64-bit TTL bipolar RAM, inverting (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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