

✓ **54H/74H71** 011514  
**JK MASTER/SLAVE FLIP-FLOP**  
 (With AND-OR Inputs)

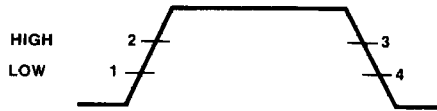
**DESCRIPTION** — The '71 is a high speed JK master/slave flip-flop with AND-OR gate inputs. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from AND-OR gate inputs to master; 3) disable AND-OR gate inputs; 4) transfer information from master to slave. The logic state of J and K inputs must not be allowed to change when the clock pulse is in a HIGH state.

**TRUTH TABLE**

INPUTS		OUTPUT
J	K	Q
L	L	Q <sub>n</sub>
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = HIGH Voltage Level  
 L = LOW Voltage Level

**CLOCK WAVEFORM**



Asynchronous Input:  
 LOW input to  $\bar{S}_D$  sets Q to HIGH level  
 Set is independent of clock

$J = (J_{1A} \cdot J_{1B}) + (J_{2A} \cdot J_{2B})$   
 $K = (K_{1A} \cdot K_{1B}) + (K_{2A} \cdot K_{2B})$   
 $t_n$  = Bit time before clock pulse.  
 $t_{n+1}$  = Bit time after clock pulse.

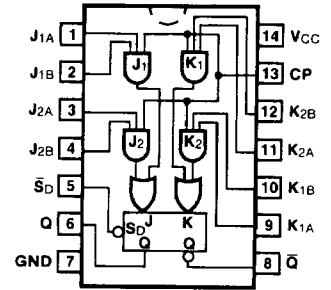
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	74H71PC		9A
Ceramic DIP (D)	A	74H71DC	54H71DM	6A
Flatpak (F)	B	74H71FC	54H71FM	3I

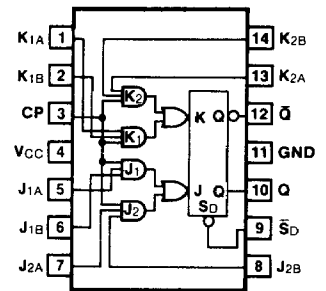
**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74H (U.L.) HIGH/LOW
J <sub>1A</sub> , J <sub>1B</sub> , J <sub>2A</sub> , J <sub>2B</sub> K <sub>1A</sub> , K <sub>1B</sub> , K <sub>2A</sub> , K <sub>2B</sub>	Data Inputs	1.25/1.25
CP	Clock Pulse Input (Active Falling Edge)	2.5/2.5
$\bar{S}_D$	Direct Set Input (Active LOW)	3.75/3.75
Q, $\bar{Q}$	Outputs	12.5/12.5

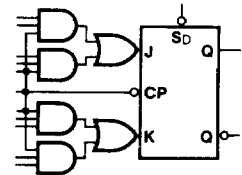
**CONNECTION DIAGRAMS**  
**PINOUT A**



**PINOUT B**



**LOGIC SYMBOL**



V<sub>CC</sub> = Pin 14 (4)  
 GND = Pin 7 (11)



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