

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT251 8-input multiplexer; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

8-input multiplexer; 3-state

74HC/HCT251

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S₀, S₁, S₂) controlling the switch positions. Assertion (Y) and negation (\bar{Y}) outputs are both provided. The output enable input (\bar{OE}) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \bar{OE} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	I _n to Y		15	19	ns
	I _n to \bar{Y}		17	19	ns
	S _n to Y		20	20	ns
	S _n to \bar{Y}		21	21	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

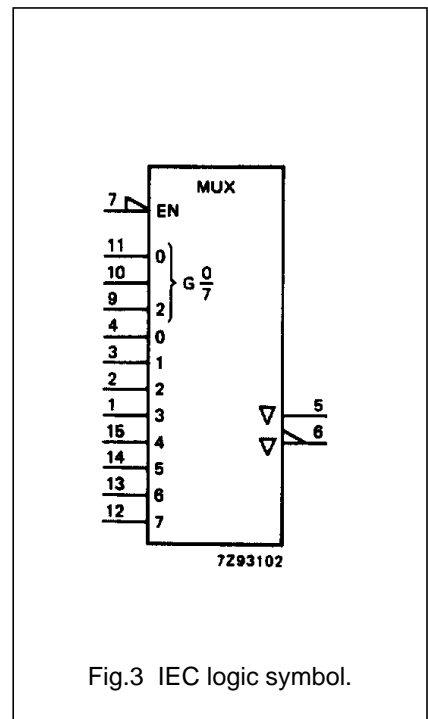
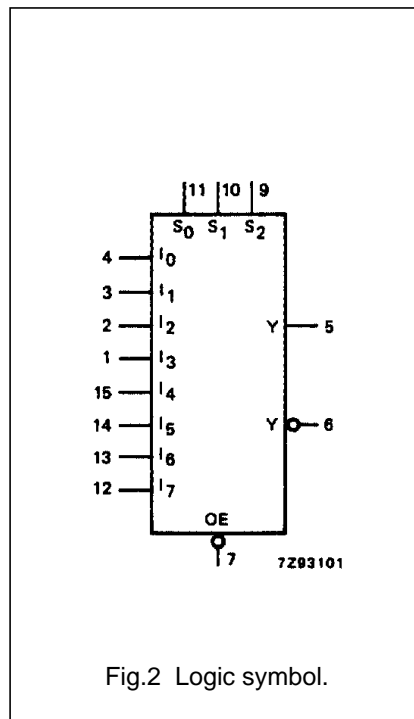
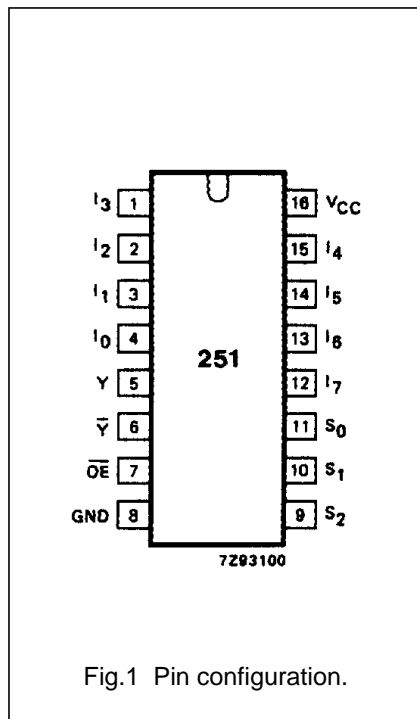
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-input multiplexer; 3-state

74HC/HCT251

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	\bar{Y}	complementary multiplexer output
7	\overline{OE}	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage



8-input multiplexer; 3-state

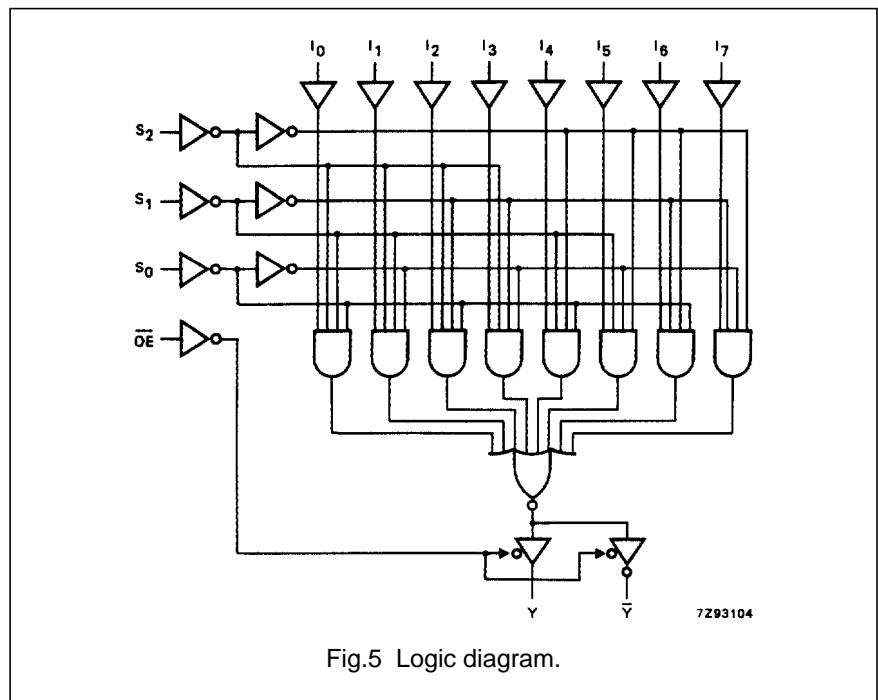
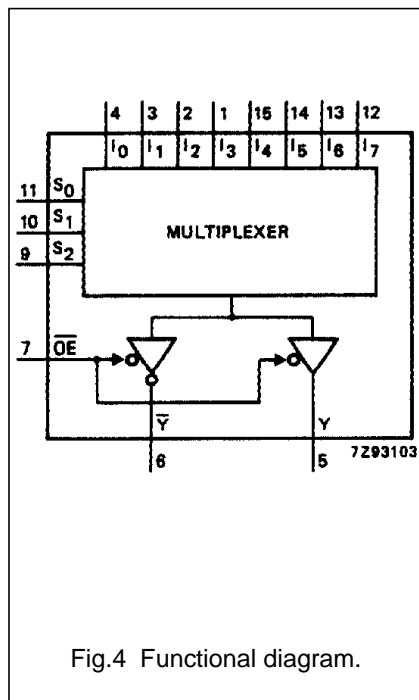
74HC/HCT251

FUNCTION TABLE

INPUTS												OUTPUTS	
\overline{OE}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\overline{Y}	Y
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

Note

- H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state



8-input multiplexer; 3-state

74HC/HCT251

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay I _n to Y		50 18 14	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay I _n to \bar{Y}		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay S _n to Y		66 24 19	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to \bar{Y}		69 25 20	205 41 35		255 51 43		310 62 53	ns	2.0 4.5 6.0	Fig.7
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to Y, \bar{Y}		36 13 10	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to Y, \bar{Y}		39 14 11	140 28 24		170 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

8-input multiplexer; 3-state

74HC/HCT251

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n	1.00
S ₀	1.50
S ₁ , S ₂	1.50
\overline{OE}	1.50

AC CHARACTERISTICS FOR HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay I _n to Y		22	35		44		53	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay I _n to \overline{Y}		22	35		44		53	ns	4.5	Fig.7
t _{PHL} / t _{PLH}	propagation delay S _n to Y		24	44		55		66	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to \overline{Y}		25	44		55		66	ns	4.5	Fig.7
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE} to Y, \overline{Y}		13	28		35		42	ns	4.5	Fig.7
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE} to Y, \overline{Y}		14	28		35		42	ns	4.5	Fig.7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

8-input multiplexer; 3-state

74HC/HCT251

AC WAVEFORMS

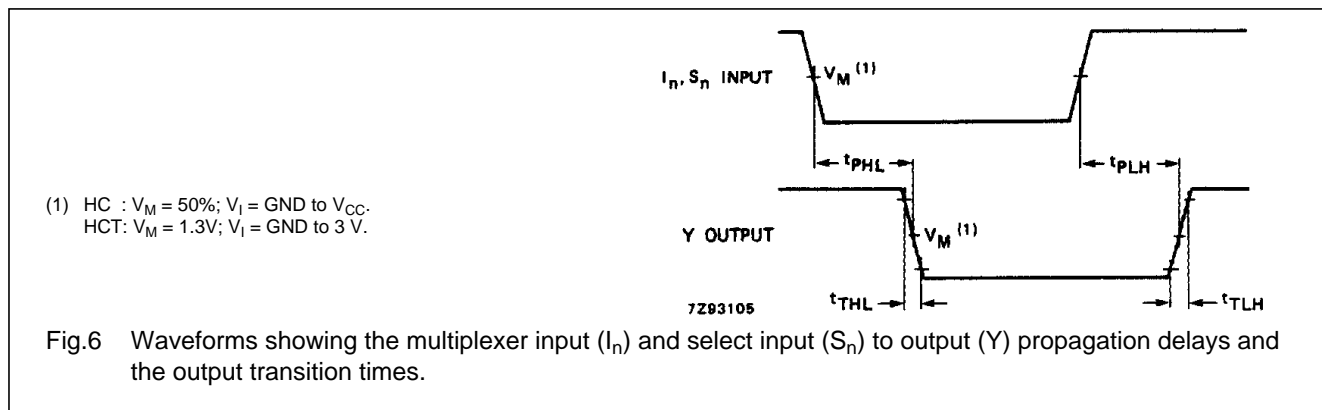


Fig.6 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays and the output transition times.

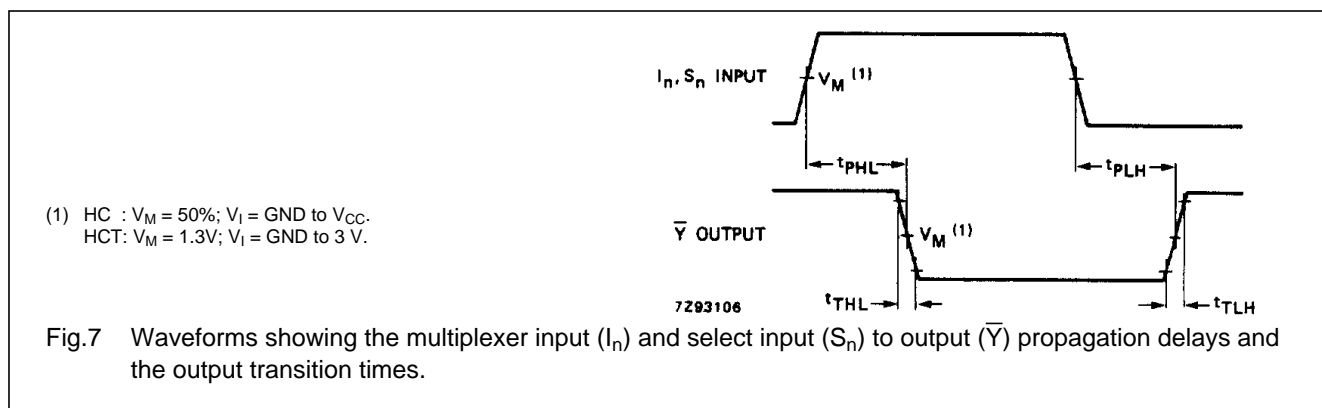


Fig.7 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (\bar{Y}) propagation delays and the output transition times.

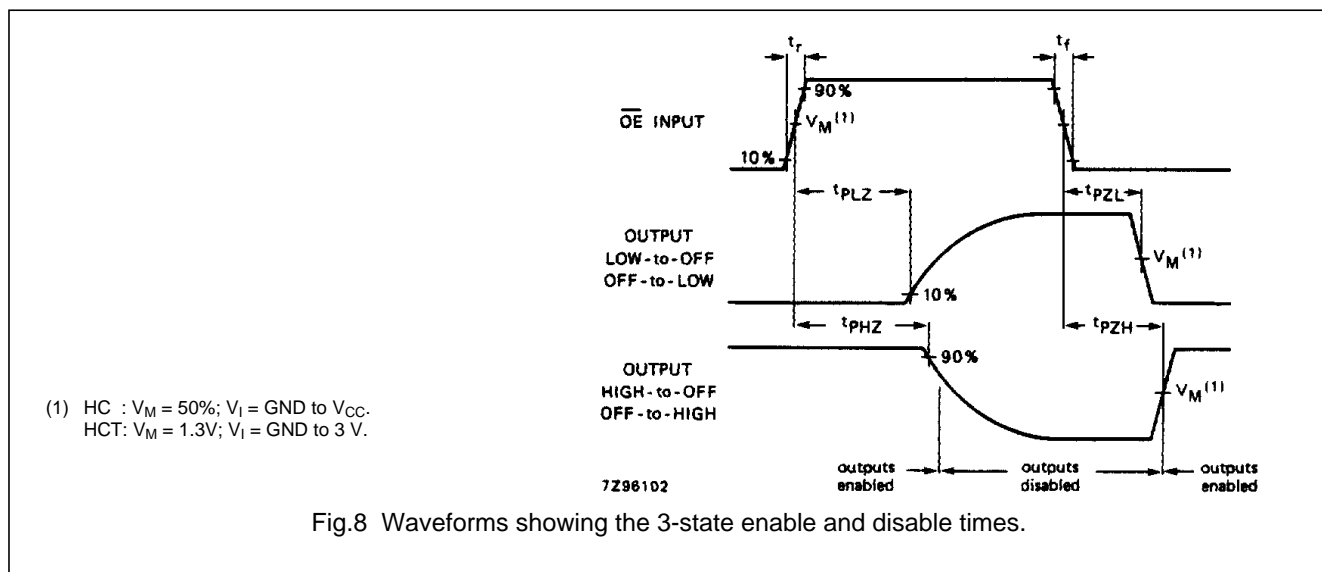


Fig.8 Waveforms showing the 3-state enable and disable times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".



LittleDiode supplies new, hard to find or obsolete electronic components and semiconductors all over the world.

With over two million different components listed you are sure to find the part you need.

Feel free to visit us today at our online store:

LittleDiode.com

Looking forward to providing you with the best possible service.