DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4024
7-stage binary ripple counter

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

7-stage binary ripple counter 74HC/HCT4024

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4024 are high-speed Si-gate CMOS devices and are pin compatible with the “4024” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4024 are 7-stage binary ripple counters with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (Q_0 to Q_6).

The counter advances on the HIGH-to-LOW transition of $\overline{CP}$.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$.

Each counter stage is a static toggle flip-flop.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

APPLICATIONS

- Frequency dividing circuits
- Time delay circuits

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0	C_L = 15 pF; V_{CC} = 5 V	14	14	ns
f_{max}	maximum clock frequency		90	70	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	25	27	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{CP}$	clock input (HIGH-to-LOW, edge-triggered)
2	MR	master reset input (active HIGH)
12, 11, 9, 6, 5, 4, 3	Q_0 to Q_6	parallel outputs
7	GND	ground (0 V)
8, 10, 13	n.c.	not connected
14	V_{CC}	positive supply voltage

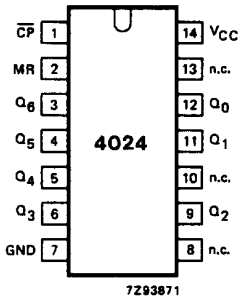


Fig.1 Pin configuration.

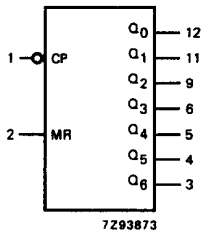


Fig.2 Logic symbol.

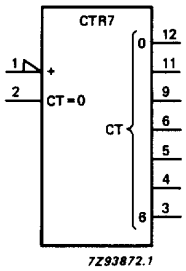


Fig.3 IEC logic symbol.

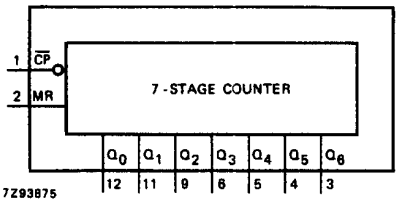


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{CP}$	MR	Q_n
↑	L	no change
↓	L	count
X	H	L

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
   ↓ = HIGH-to-LOW clock transition

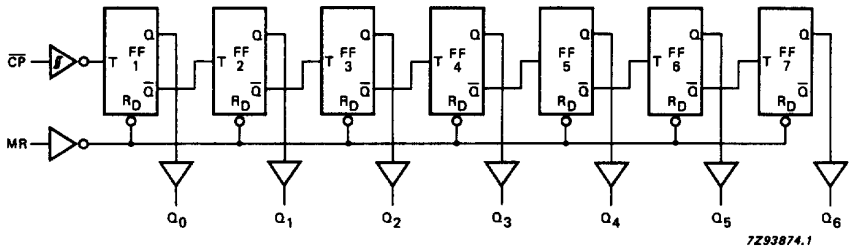


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +125		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t_{PHL}	propagation delay MR to Q_0		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		25 9 7	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width HIGH	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_{rem}	removal time MR to $\overline{CP}$	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.6
f_{max}	maximum clock pulse frequency	6.0 30 35	27 82 98		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

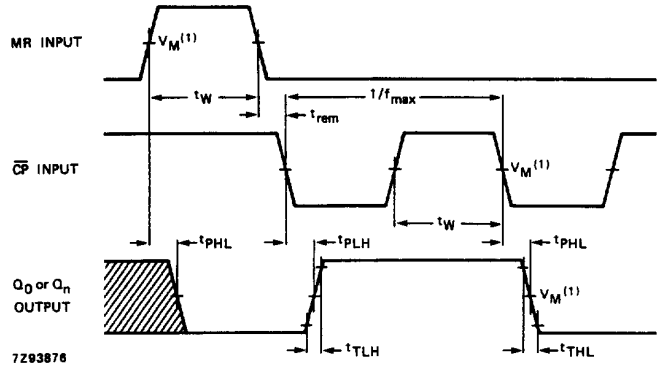
INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}$	0.75
MR	0.85

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +125		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{CP}$ to Q_0		17	35		44		53	ns	4.5	Fig.6
t_{PHL}	propagation delay MR to Q_0		21	40		50		60	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		9	16		20		24	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig.6
t_W	master reset pulse width HIGH	16	6		20		24		ns	4.5	Fig.6
t_{rem}	removal time MR to $\overline{CP}$	10	0		13		15		ns	4.5	Fig.6
f_{max}	maximum clock pulse frequency	30	64		24		20		MHz	4.5	Fig.6

AC WAVEFORMS



Also showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock ($\overline{CP}$) removal time.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock ($\overline{CP}$) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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