

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4352 Dual 4-channel analog multiplexer/demultiplexer with latch

Product specification
File under Integrated Circuits, IC06

December 1990

Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

FEATURES

- Wide analog input voltage range: ± 5 V.
- Low "ON" resistance:
 - 80 Ω (typ.) at $V_{CC} - V_{EE} = 4.5$ V
 - 70 Ω (typ.) at $V_{CC} - V_{EE} = 6.0$ V
 - 60 Ω (typ.) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4352 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4352 are dual 4-channel analog multiplexers/demultiplexers with common select logic.

Each multiplexer has four independent inputs/outputs (nY_0 to nY_3) and a common input/output (nZ).

The common channel select logics include two select inputs (S_0 and S_1), an active LOW enable input (\bar{E}_1), an active HIGH enable input (E_2) and a latch enable input ($\bar{L}\bar{E}$).

With \bar{E}_1 LOW and E_2 HIGH, one of the four switches is selected (low impedance ON-state) by S_0 and S_1 . The data at the select inputs may be latched by using the active LOW latch enable input ($\bar{L}\bar{E}$). When $\bar{L}\bar{E}$ is HIGH, the latch is transparent. When either of the two enable inputs, \bar{E}_1 (active LOW) and E_2 (active HIGH), is inactive, all analog switches are turned off.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_0 , S_1 , $\bar{L}\bar{E}$, \bar{E}_1 and E_2). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 to nY_3 , and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

QUICK REFERENCE DATA

$V_{EE} = \text{GND} = 0$ V; $T_{\text{amb}} = 25$ °C; $t_r = t_f = 6$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t_{PZH}/t_{PZL} | turn "ON" time \bar{E}_1 , E_2 or S_n to V_{OS} | $C_L = 15$ pF; $R_L = 1$ k Ω ; $V_{CC} = 5$ V | 31 | 33 | ns |
| t_{PHZ}/t_{PLZ} | turn "OFF" time \bar{E}_1 , E_2 or S_n to V_{OS} | | 20 | 20 | ns |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per switch | notes 1 and 2 | 55 | 55 | pF |
| C_S | max. switch capacitance | | | | |
| | independent (Y) | | 5 | 5 | pF |
| | common (Z) | | 12 | 12 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \} \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum \{ (C_L + C_S) \times V_{CC}^2 \times f_o \}$ = sum of outputs

C_L = output load capacitance in pF

C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND}$ to V_{CC}
For HCT the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5$ V

Dual 4-channel analog multiplexer/demultiplexer with latch

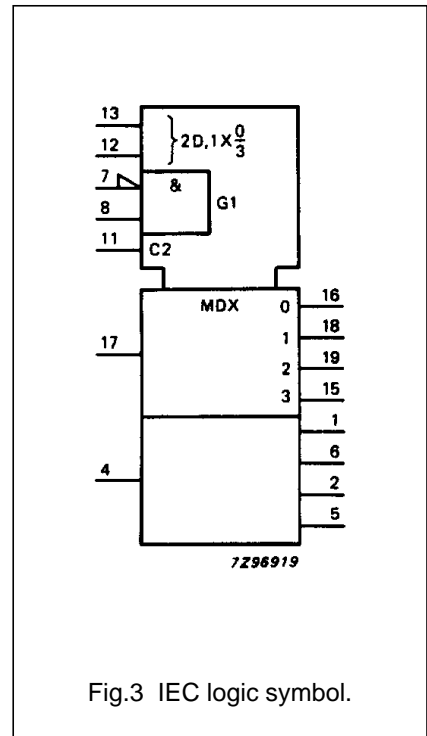
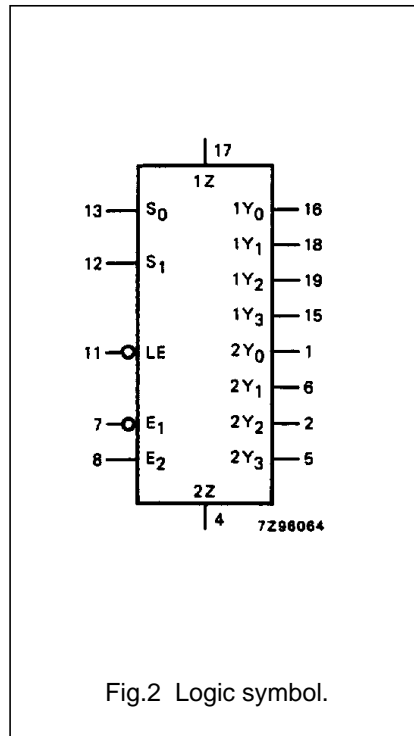
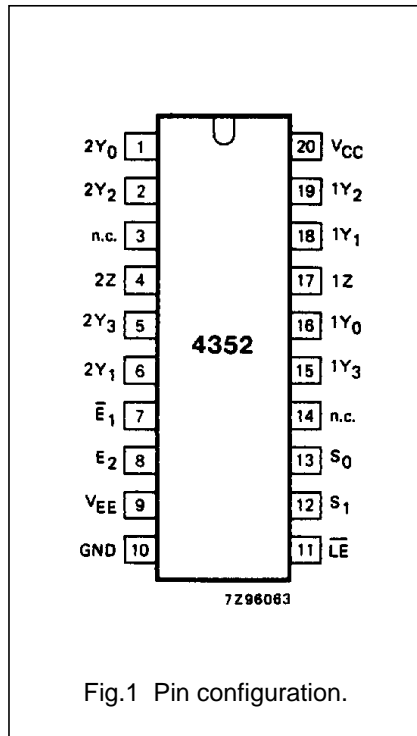
74HC/HCT4352

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------|------------------------------------|---------------------------------|
| 1, 6, 2, 5 | 2Y ₀ to 2Y ₃ | independent inputs/outputs |
| 3, 14 | n.c. | not connected |
| 7 | \bar{E}_1 | enable input (active LOW) |
| 8 | E ₂ | enable input (active HIGH) |
| 9 | V _{EE} | negative supply voltage |
| 10 | GND | ground (0 V) |
| 11 | $\bar{L}E$ | latch enable input (active LOW) |
| 13, 12 | S ₀ , S ₁ | select inputs |
| 16, 18, 19, 15 | 1Y ₀ to 1Y ₃ | independent inputs/outputs |
| 17, 4 | 1Z, 2Z | common inputs/outputs |
| 20 | V _{CC} | positive supply voltage |



Dual 4-channel analog multiplexer/demultiplexer with latch

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FUNCTION TABLE

| INPUTS | | | | | CHANNEL ON |
|-------------|-------|------------|-------|-------|-------------|
| \bar{E}_1 | E_2 | \bar{LE} | S_1 | S_0 | |
| H | X | X | X | X | none |
| X | L | X | X | X | none |
| L | H | H | L | L | $nY_0 - nZ$ |
| L | H | H | L | H | $nY_1 - nZ$ |
| L | H | H | H | L | $nY_2 - nZ$ |
| L | H | H | H | H | $nY_3 - nZ$ |
| L | H | L | X | X | (1) |
| X | X | ↓ | X | X | (2) |

Notes

1. Last selected channel "ON".
2. Selected channels latched.

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 ↓ = HIGH-to-LOW \bar{LE} transition

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

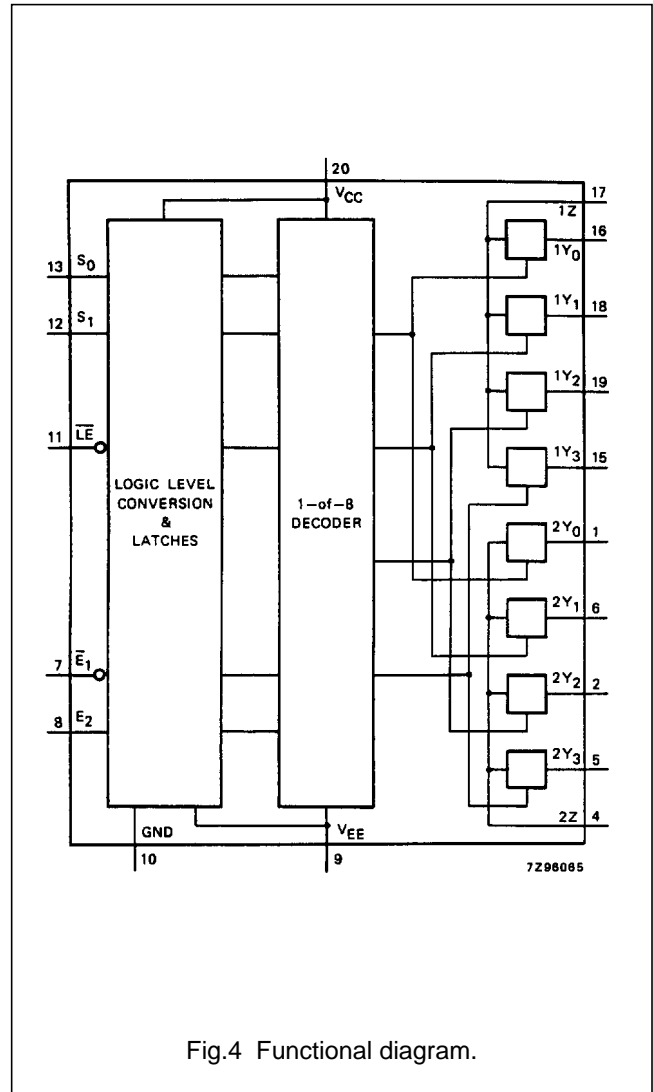


Fig.4 Functional diagram.

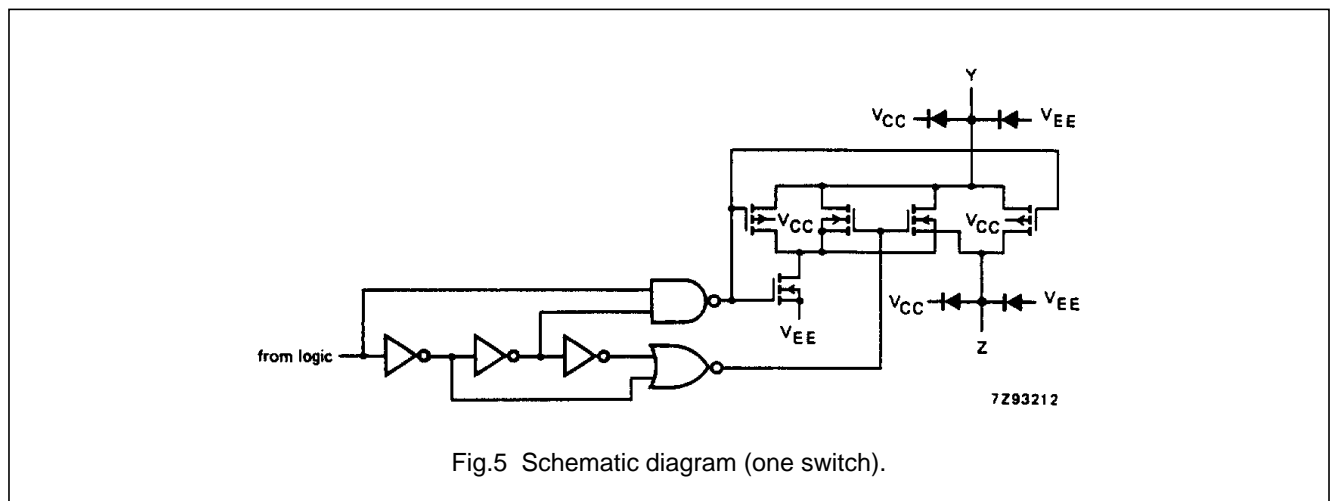


Fig.5 Schematic diagram (one switch).

Dual 4-channel analog multiplexer/demultiplexer with latch

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to $V_{EE} = \text{GND}$ (ground = 0 V)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | CONDITIONS |
|--------------------------------|--------------------------------|------|-------|------|--|
| V_{CC} | DC supply voltage | -0.5 | +11.0 | V | |
| $\pm I_{IK}$ | DC digital input diode current | | 20 | mA | for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$ |
| $\pm I_{SK}$ | DC switch diode current | | 20 | mA | for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$ |
| $\pm I_S$ | DC switch current | | 25 | mA | for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$ |
| $\pm I_{EE}$ | DC V_{EE} current | | 20 | mA | |
| $\pm I_{CC};$ $\pm I_{GND}$ | DC V_{CC} or GND current | | 50 | mA | |
| T_{stg} | storage temperature range | -65 | +150 | °C | |
| P_{tot} | power dissipation per package | | | | for temperature range: -40 to +125 °C 74HC/HCT |
| | plastic DIL | | 750 | mW | above +70 °C: derate linearly with 12 mW/K |
| | plastic mini-pack (SO) | | 500 | mW | above +70 °C: derate linearly with 6 mW/K |
| P_S | power dissipation per switch | | 100 | mW | |

Note

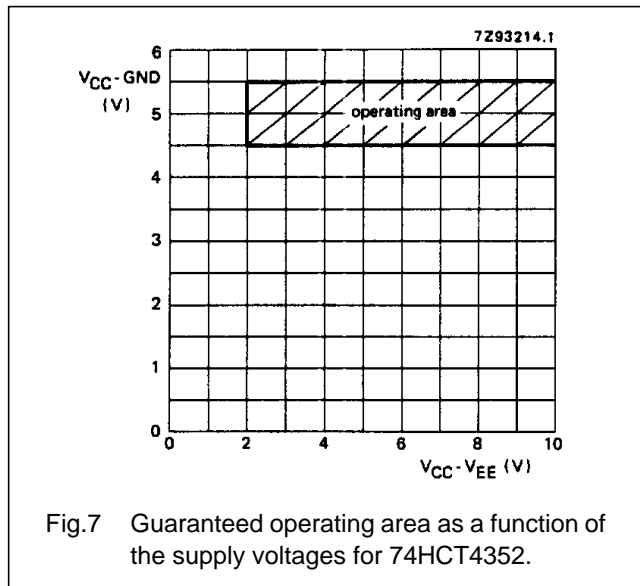
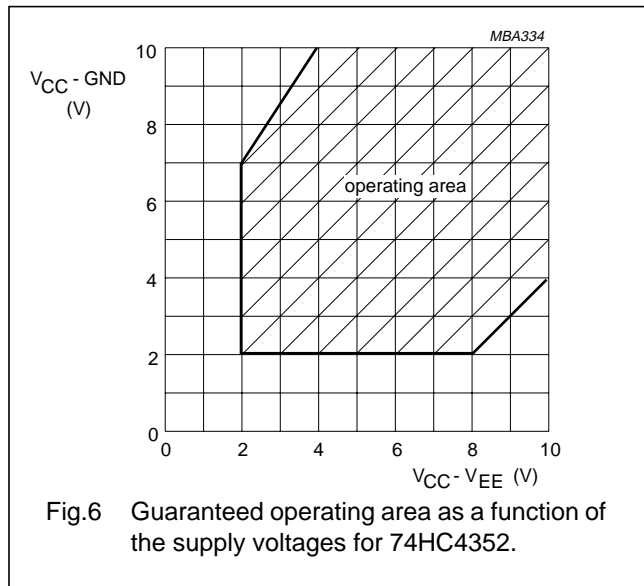
- To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nY_n, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nY_n. In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 74HC | | | 74HCT | | | UNIT | CONDITIONS |
|------------|---------------------------------------|----------|------|---------------------------|----------|------|----------|------|---|
| | | min. | typ. | max. | min. | typ. | max. | | |
| V_{CC} | DC supply voltage $V_{CC}-\text{GND}$ | 2.0 | 5.0 | 10.0 | 4.5 | 5.0 | 5.5 | V | see Figs 6 and 7 |
| V_{CC} | DC supply voltage $V_{CC}-V_{EE}$ | 2.0 | 5.0 | 10.0 | 2.0 | 5.0 | 10.0 | V | see Figs 6 and 7 |
| V_I | DC input voltage range | GND | | V_{CC} | GND | | V_{CC} | V | |
| V_S | DC switch voltage range | V_{EE} | | V_{CC} | V_{EE} | | V_{CC} | V | |
| T_{amb} | operating ambient temperature range | -40 | | +85 | -40 | | +85 | °C | see DC and AC CHARACTERISTICS |
| T_{amb} | operating ambient temperature range | -40 | | +125 | -40 | | +125 | °C | |
| t_r, t_f | input rise and fall times | | 6.0 | 1000 500 400 250 | | 6.0 | 500 | ns | $V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$ |

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DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | | | |
|-----------------|---|----------------|------|------|------------|------|-------------|------|----------|-----------------|-----------------|----------------------|----------------------------|----------------------------|
| | | 74HC/HCT | | | | | | | | V_{CC} (V) | V_{EE} (V) | I_S (μA) | V_{is} | V_I |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | | |
| R_{ON} | ON resistance (peak) | | - | - | | - | | - | Ω | 2.0 | 0 | 100 | V_{CC} to V_{EE} | V_{IN} or V_{IL} |
| | | | 100 | 180 | | 225 | | 270 | Ω | 4.5 | 0 | 1000 | | |
| | | | 90 | 160 | | 200 | | 240 | Ω | 6.0 | 0 | 1000 | | |
| | | | 70 | 130 | | 165 | | 195 | Ω | 4.5 | -4.5 | 1000 | | |
| R_{ON} | ON resistance (rail) | | 150 | - | | - | | - | Ω | 2.0 | 0 | 100 | V_{EE} | V_{IH} or V_{IL} |
| | | | 80 | 140 | | 175 | | 210 | Ω | 4.5 | 0 | 1000 | | |
| | | | 70 | 120 | | 150 | | 180 | Ω | 6.0 | 0 | 1000 | | |
| | | | 60 | 105 | | 130 | | 160 | Ω | 4.5 | -4.5 | 1000 | | |
| R_{ON} | ON resistance (rail) | | 150 | - | | - | | - | Ω | 2.0 | 0 | 100 | V_{CC} | V_{IH} or V_{IL} |
| | | | 90 | 160 | | 200 | | 240 | Ω | 4.5 | 0 | 1000 | | |
| | | | 80 | 140 | | 175 | | 210 | Ω | 6.0 | 0 | 1000 | | |
| | | | 65 | 120 | | 150 | | 180 | Ω | 4.5 | -4.5 | 1000 | | |
| ΔR_{ON} | maximum ΔR_{ON} resistance between any two channels | | - | | | | | | Ω | 2.0 | 0 | | V_{CC} to V_{EE} | V_{IH} or V_{IL} |
| | | | 9 | | | | | | Ω | 4.5 | 0 | | | |
| | | | 8 | | | | | | Ω | 6.0 | 0 | | | |
| | | | 6 | | | | | | Ω | 4.5 | -4.5 | | | |

Notes

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig.8.

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DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | | |
|-----------------|--|---------------------------|--------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|------|--------------------------|------------------------|--|---|
| | | 74HC | | | | | | | | V _{CC} (V) | V _{EE} (V) | V _I | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| V _{IH} | HIGH level input voltage | 1.5 3.15 4.2 6.3 | 1.2 2.4 3.2 4.7 | | 1.5 3.15 4.2 6.3 | | 1.5 3.15 4.2 6.3 | | V | 2.0 4.5 6.0 9.0 | | | |
| V _{IL} | LOW level input voltage | | 0.8 2.1 2.8 4.3 | 0.5 1.35 1.8 2.7 | | 0.5 1.35 1.8 2.7 | | 0.5 1.35 1.8 2.7 | V | 2.0 4.5 6.0 9.0 | | | |
| ±I _I | input leakage current | | | 0.1 0.2 | | 1.0 2.0 | | 1.0 2.0 | µA | 6.0 10.0 | 0 0 | V _{CC} or GND | |
| ±I _S | analog switch OFF-state current per channel | | | 0.1 | | 1.0 | | 1.0 | µA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.10) |
| ±I _S | analog switch OFF-state current all channels | | | 0.2 | | 2.0 | | 2.0 | µA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.10) |
| ±I _S | analog switch ON-state current | | | 0.2 | | 2.0 | | 2.0 | µA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.11) |
| I _{CC} | quiescent supply current | | | 8.0 16.0 | | 80.0 160.0 | | 160.0 320.0 | µA | 6.0 10.0 | 0 0 | V _{CC} or GND | V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE} |

Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

AC CHARACTERISTICS FOR 74HCGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------------------------|------------------------|-------|--|
| | | 74HC | | | | | | | V _{CC} (V) | V _{EE} (V) | OTHER | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | | max. | | | |
| t _{PHL} / t _{PLH} | propagation delay V _{is} to V _{os} | | 17 | 60 | | 75 | | 90 | ns | 2.0 | 0 | R _L = ∞; C _L = 50 pF (see Fig.18) |
| | | | 6 | 12 | | 15 | | 18 | | 4.5 | 0 | |
| | | | 5 | 10 | | 13 | | 15 | | 6.0 | 0 | |
| | | | 5 | 8 | | 10 | | 12 | | 4.5 | -4.5 | |
| t _{PZH} / t _{PZL} | turn "ON" time \overline{E}_1 ; E ₂ to V _{os} LE to V _{os} | | 99 | 325 | | 405 | | 490 | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.19) |
| | | | 36 | 65 | | 81 | | 98 | | 4.5 | 0 | |
| | | | 29 | 55 | | 69 | | 83 | | 6.0 | 0 | |
| | | | 25 | 46 | | 58 | | 69 | | 4.5 | -4.5 | |
| t _{PZH} / t _{PZL} | turn "ON" time S _n to V _{os} | | 99 | 325 | | 405 | | 490 | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.19) |
| | | | 36 | 65 | | 81 | | 98 | | 4.5 | 0 | |
| | | | 29 | 55 | | 69 | | 80 | | 6.0 | 0 | |
| | | | 25 | 46 | | 58 | | 69 | | 4.5 | -4.5 | |
| t _{PHZ} / t _{PLZ} | turn "OFF" time \overline{E}_1 ; E ₂ to V _{os} LE to V _{os} | | 58 | 200 | | 250 | | 300 | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.19) |
| | | | 21 | 40 | | 50 | | 60 | | 4.5 | 0 | |
| | | | 17 | 34 | | 43 | | 51 | | 6.0 | 0 | |
| | | | 21 | 40 | | 50 | | 60 | | 4.5 | -4.5 | |
| t _{PHZ} / t _{PLZ} | turn "OFF" time S _n to V _{os} | | 63 | 200 | | 250 | | 300 | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.19) |
| | | | 23 | 40 | | 50 | | 60 | | 4.5 | 0 | |
| | | | 18 | 34 | | 43 | | 51 | | 6.0 | 0 | |
| | | | 24 | 40 | | 50 | | 60 | | 4.5 | -4.5 | |
| t _{su} | set-up time S _n to \overline{LE} | 90 | 17 | | 115 | | 135 | | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.20) |
| | | 18 | 6 | | 23 | | 27 | | | 4.5 | 0 | |
| | | 15 | 5 | | 20 | | 23 | | | 6.0 | 0 | |
| | | 18 | 9 | | 23 | | 27 | | | 4.5 | -4.5 | |
| t _h | hold time S _n to \overline{LE} | 5 | -6 | | 5 | | 5 | | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.20) |
| | | 5 | -2 | | 5 | | 5 | | | 4.5 | 0 | |
| | | 5 | -2 | | 5 | | 5 | | | 6.0 | 0 | |
| | | 5 | -3 | | 5 | | 5 | | | 4.5 | -4.5 | |
| t _w | \overline{LE} minimum pulse width HIGH | 80 | 11 | | 100 | | 120 | | ns | 2.0 | 0 | R _L = 1 kΩ; C _L = 50 pF (see Fig.20) |
| | | 16 | 4 | | 20 | | 24 | | | 4.5 | 0 | |
| | | 14 | 3 | | 17 | | 20 | | | 6.0 | 0 | |
| | | 16 | 4 | | 20 | | 24 | | | 4.5 | -4.5 | |

Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | | |
|------------------|---|-----------------------|------|-------------|------------|---------------|-------------|----------------|------|------------------------|------------------------|------------------------------------|---|
| | | 74HCT | | | | | | | | V _{CC} (V) | V _{EE} (V) | V _I | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| V _{IH} | HIGH level input voltage | 2.0 | 1.6 | | 2.0 | | 2.0 | | V | 4.5 to 5.5 | | | |
| V _{IL} | LOW level input voltage | | 1.2 | 0.8 | | 0.8 | | 0.8 | V | 4.5 to 5.5 | | | |
| ±I _I | input leakage current | | | 0.1 | | 1.0 | | 1.0 | μA | 5.5 | 0 | V _{CC} or GND | |
| ±I _S | analog switch OFF-state current per channel | | | 0.1 | | 1.0 | | 1.0 | μA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.10) |
| ±I _S | analog switch OFF-state current all channels | | | 0.2 | | 2.0 | | 2.0 | μA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.10) |
| ±I _S | analog switch ON-state current | | | 0.2 | | 2.0 | | 2.0 | μA | 10.0 | 0 | V _{IH} or V _{IL} | V _S = V _{CC} - V _{EE} (see Fig.11) |
| I _{CC} | quiescent supply current | | | 8.0 16.0 | | 80.0 160.0 | | 160.0 320.0 | μA | 5.5 5.0 | 0 -5.0 | V _{CC} or GND | V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE} |
| ΔI _{CC} | additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) | | 100 | 360 | | 450 | | 490 | μA | 4.5 to 5.5 | 0 | V _{CC} - 2.1 V | other inputs at V _{CC} or GND |

Note to HCT types

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------------|-----------------------|
| \overline{E}_1, E_2 | 0.50 |
| \overline{S}_n | 0.50 |
| \overline{LE} | 1.5 |

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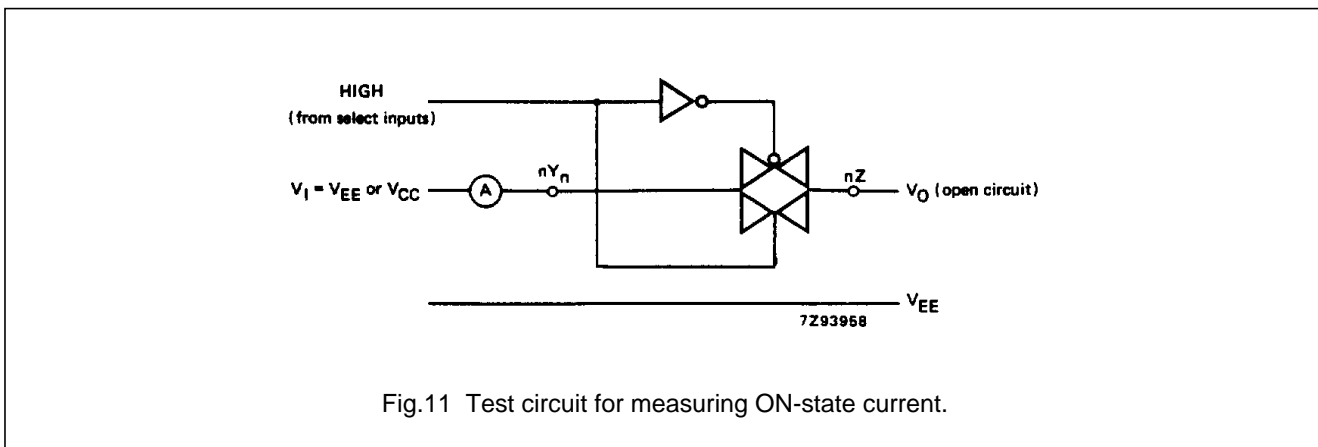
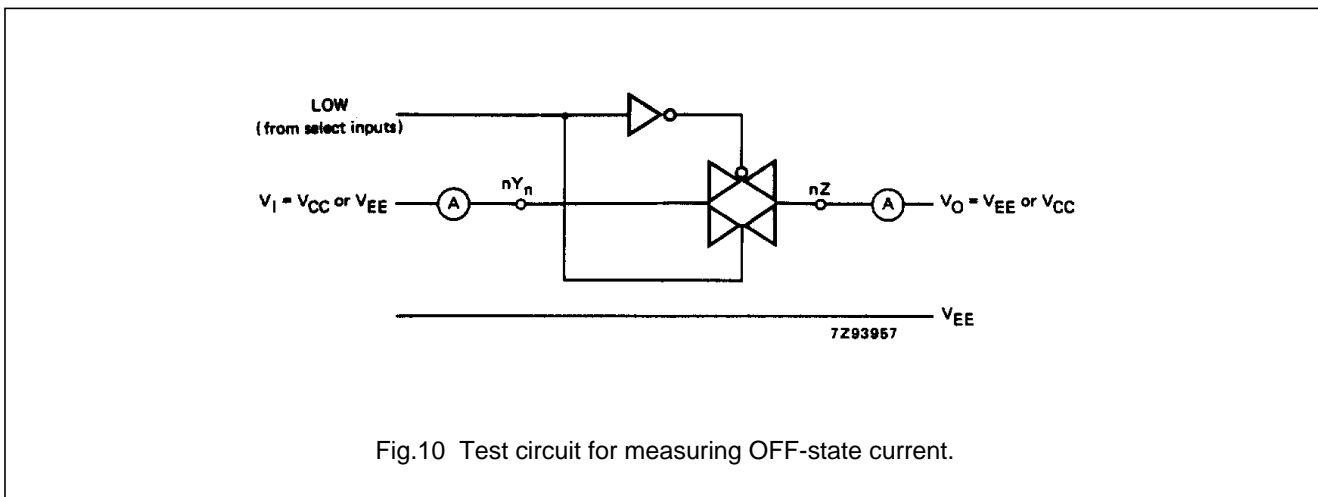
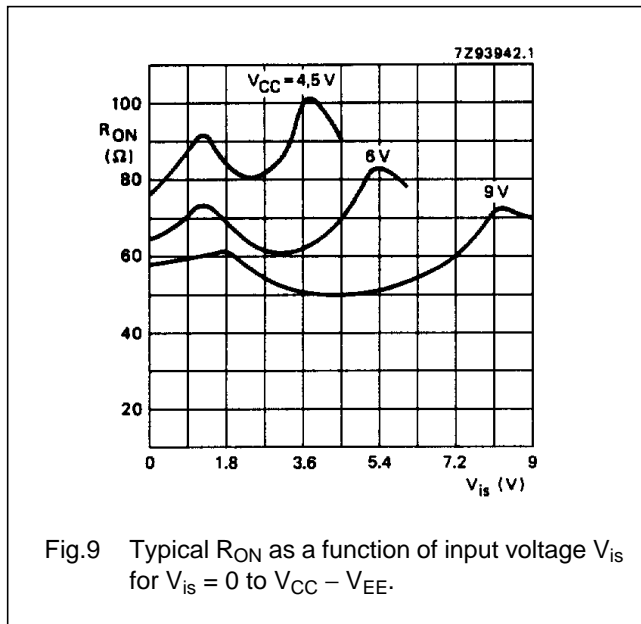
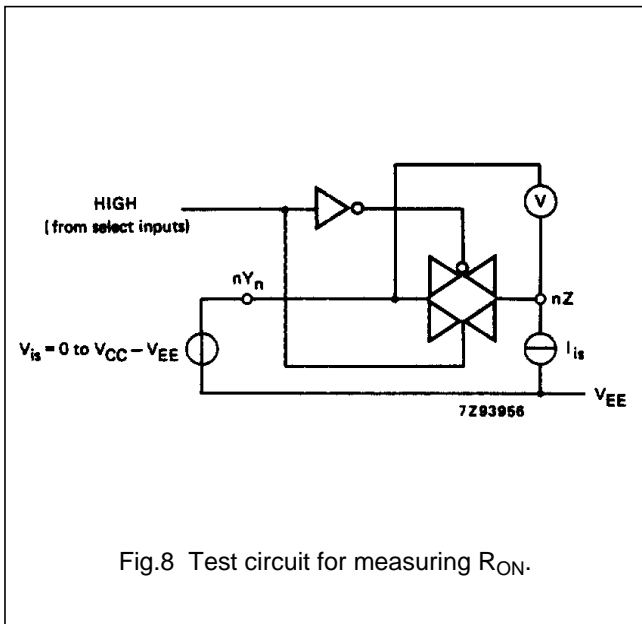
74HC/HCT4352

AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | | |
|-------------------|---|----------------|----------|----------|------------|----------|-------------|----------|-----------------|-----------------|-----------|---|
| | | 74HCT | | | | | | | V_{CC} (V) | V_{EE} (V) | OTHER | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | | max. | | | |
| t_{PHL}/t_{PLH} | propagation delay V_{is} to V_{os} | | 6 5 | 12 8 | | 15 10 | | 18 12 | ns | 4.5 4.5 | 0 -4.5 | $R_L = \infty$; $C_L = 50$ pF (see Fig.18) |
| t_{PZH}/t_{PZL} | turn "ON" time \overline{E}_1 ; E_2 to V_{os} \overline{LE} to V_{os} | | 38 28 | 65 46 | | 81 58 | | 98 69 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.19) |
| t_{PZH}/t_{PZL} | turn "ON" time S_n to V_{os} | | 38 27 | 65 46 | | 81 58 | | 98 69 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.19) |
| t_{PHZ}/t_{PLZ} | turn "OFF" time \overline{E}_1 to V_{os} \overline{LE} to V_{os} | | 20 20 | 40 40 | | 50 50 | | 60 60 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.19) |
| t_{PHZ}/t_{PLZ} | turn "OFF" time \overline{E}_2 , S_n to V_{os} | | 25 25 | 43 43 | | 54 54 | | 65 65 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.19) |
| t_{su} | set-up time S_n to \overline{LE} | 16 18 | 7 9 | | 20 23 | | | 24 27 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.20) |
| t_h | hold time S_n to \overline{LE} | 5 5 | -1 -1 | | 5 5 | | | 5 5 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.20) |
| t_w | \overline{LE} minimum pulse width HIGH | 16 16 | 3 4 | | 20 20 | | | 24 24 | ns | 4.5 4.5 | 0 -4.5 | $R_L = 1$ k Ω ; $C_L = 50$ pF (see Fig.20) |

Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352



Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$

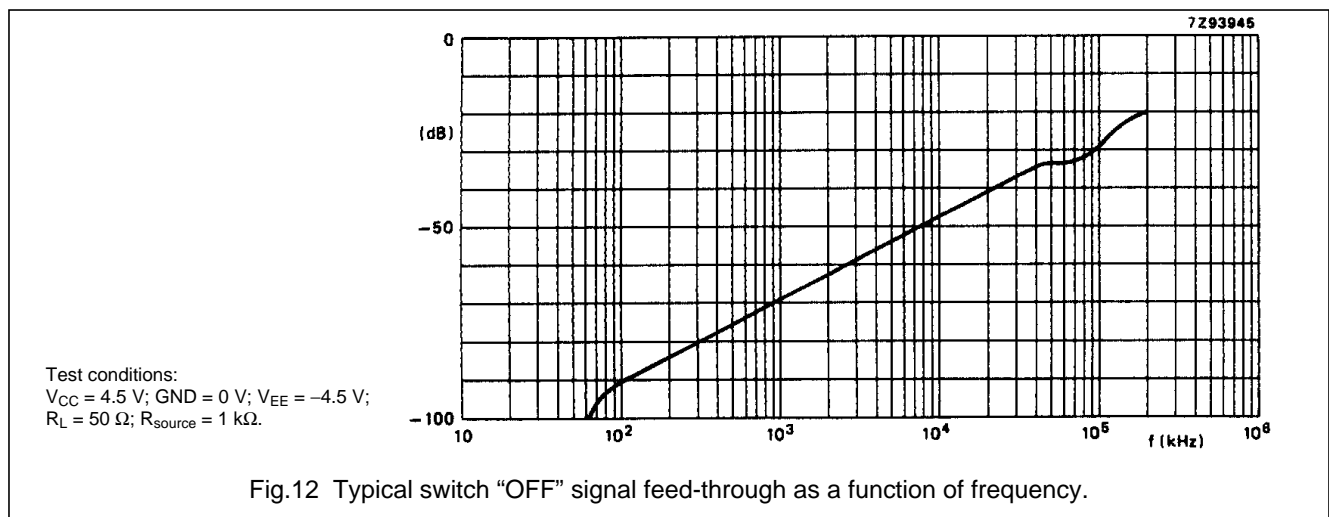
| SYMBOL | PARAMETER | typ. | UNIT | V_{CC} (V) | V_{EE} (V) | $V_{is(p-p)}$ (V) | CONDITIONS |
|-------------|---|--------------|------------|-----------------|-----------------|----------------------|--|
| | sine-wave distortion f = 1 kHz | 0.04 0.02 | % % | 2.25 4.5 | -2.25 -4.5 | 4.0 8.0 | $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ (see Fig.14) |
| | sine-wave distortion f = 10 kHz | 0.12 0.06 | % % | 2.25 4.5 | -2.25 -4.5 | 4.0 8.0 | $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ (see Fig.14) |
| | switch "OFF" signal feed-through | -50 -50 | dB dB | 2.25 4.5 | -2.25 -4.5 | note 1 | $R_L = 600\text{ }\Omega$; $C_L = 50\text{ pF}$ f = 1 MHz (see Figs 12 and 15) |
| | crosstalk between any two switches/ multiplexers | -60 -60 | dB dB | 2.25 4.5 | -2.25 -4.5 | note 1 | $R_L = 600\text{ }\Omega$; $C_L = 50\text{ pF}$; f = 1 MHz (see Fig.16) |
| $V_{(p-p)}$ | crosstalk voltage between control and any switch (peak-to-peak value) | 110 220 | mV mV | 4.5 4.5 | 0 -4.5 | | $R_L = 600\text{ }\Omega$; $C_L = 50\text{ pF}$; f = 1 MHz (\bar{E}_1 , E_2 or S_n , square-wave between V_{CC} and GND, $t_r = t_f = 6\text{ ns}$) (see Fig.17) |
| f_{max} | minimum frequency response (-3dB) | 160 170 | MHz MHz | 2.25 4.5 | -2.25 -4.5 | note 2 | $R_L = 50\text{ }\Omega$; $C_L = 10\text{ pF}$ (see Figs 13 and 14) |
| C_S | maximum switch capacitance independent (Y) common (Z) | 5 12 | pF pF | | | | |

Notes

- Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
- Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

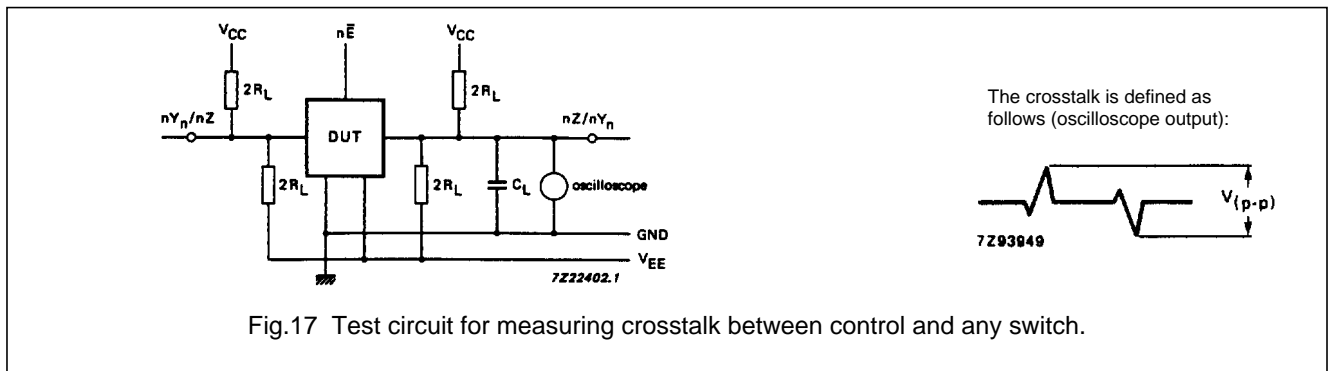
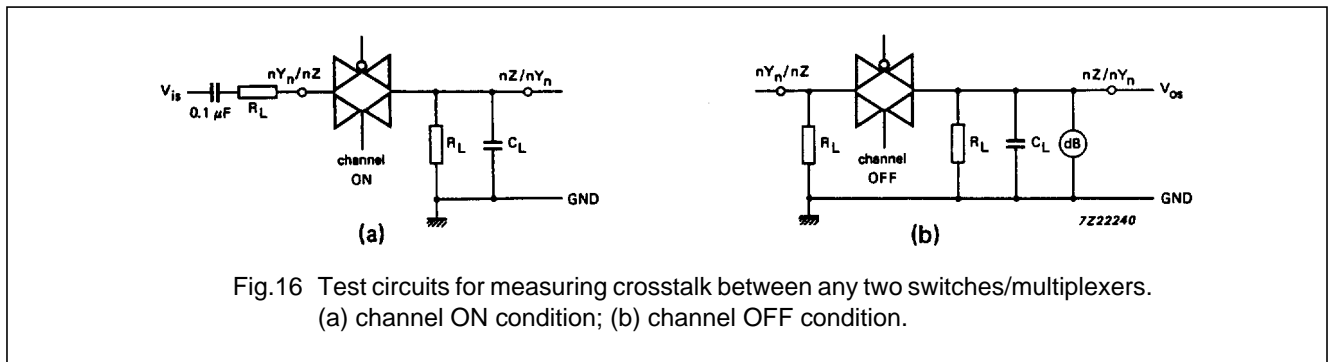
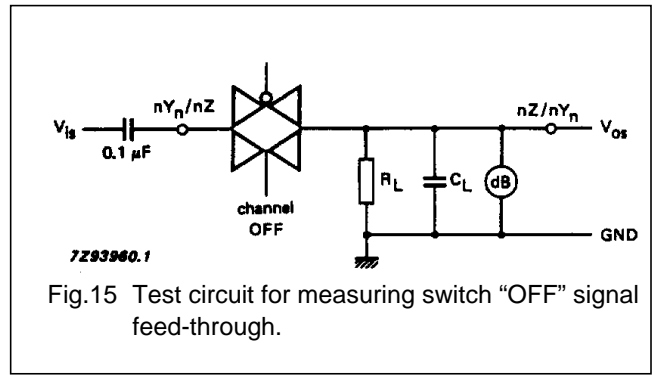
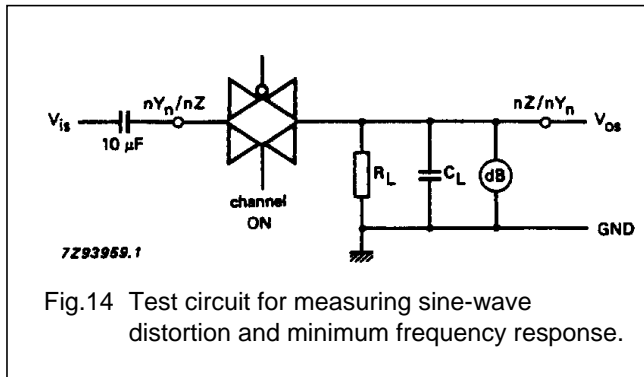
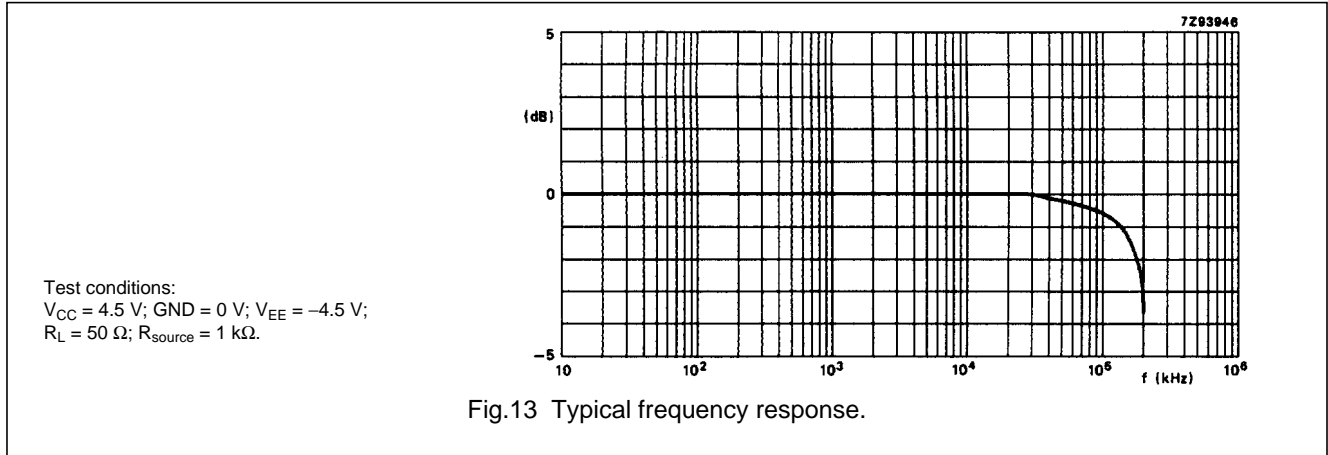
V_{is} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output.



Dual 4-channel analog multiplexer/demultiplexer with latch

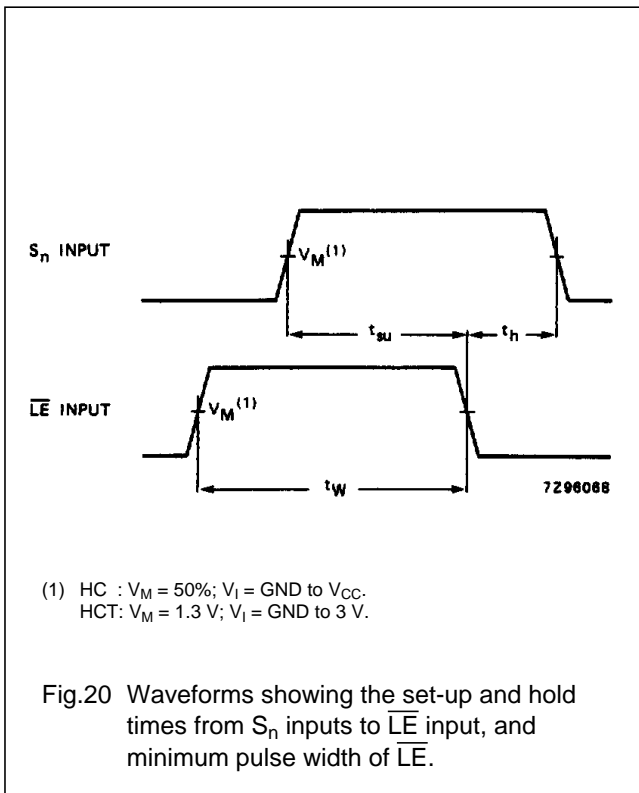
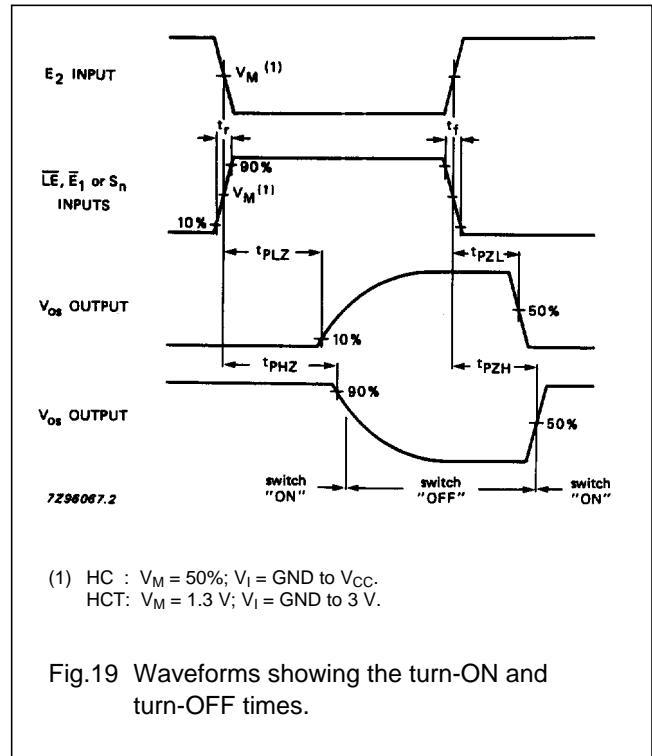
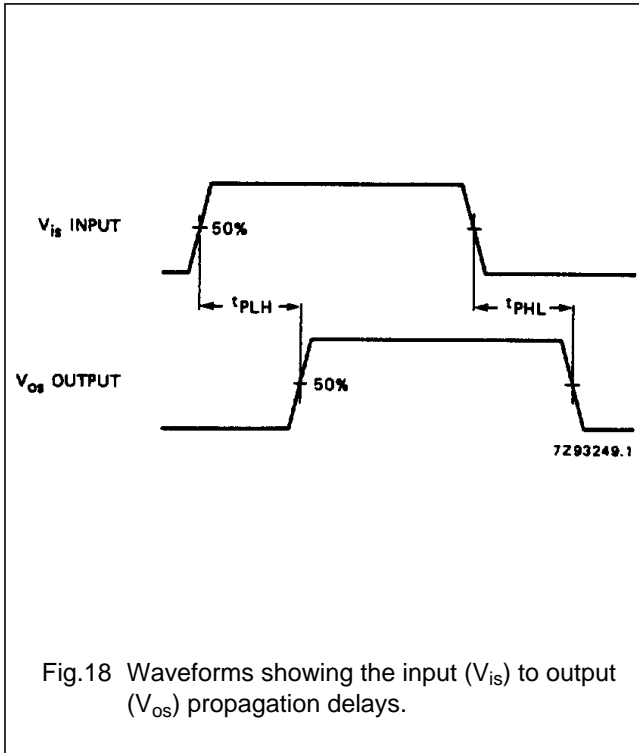
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Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

AC WAVEFORMS



Dual 4-channel analog multiplexer/demultiplexer with latch

74HC/HCT4352

TEST CIRCUIT AND WAVEFORMS

Conditions

| TEST | SWITCH | V _{is} |
|------------------|-----------------|-----------------|
| t _{PZH} | V _{EE} | V _{CC} |
| t _{PZL} | V _{CC} | V _{EE} |
| t _{PHZ} | V _{EE} | V _{CC} |
| t _{PLZ} | V _{CC} | V _{EE} |
| others | open | pulse |

7293951

| FAMILY | AMPLITUDE | V _M | t _r ; t _f | |
|--------|-----------------|----------------|---------------------------------|-------|
| | | | f _{max} ; PULSE WIDTH | OTHER |
| 74HC | V _{CC} | 50% | < 2 ns | 6 ns |
| 74HCT | 3.0 V | 1.3 V | < 2 ns | 6 ns |

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
 t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.21 Test circuit for measuring AC performance.

Conditions

| TEST | SWITCH | V _{is} |
|------------------|-----------------|-----------------|
| t _{PZH} | V _{EE} | V _{CC} |
| t _{PZL} | V _{CC} | V _{EE} |
| t _{PHZ} | V _{EE} | V _{CC} |
| t _{PLZ} | V _{CC} | V _{EE} |
| others | open | pulse |

7287476.3

| FAMILY | AMPLITUDE | V _M | t _r ; t _f | |
|--------|-----------------|----------------|---------------------------------|-------|
| | | | f _{max} ; PULSE WIDTH | OTHER |
| 74HC | V _{CC} | 50% | < 2 ns | 6 ns |
| 74HCT | 3.0 V | 1.3 V | < 2 ns | 6 ns |

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
 R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.
 t_r = t_f = 6 ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

Fig.22 Input pulse definitions.

Dual 4-channel analog
multiplexer/demultiplexer with latch

74HC/HCT4352

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.



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