NEC

MOS FIELD EFFECT TRANSISTOR
2SK3749

N-CHANNEL MOS FET FOR HIGH-SPEED SWITCHIG

DESCRIPTION

The 2SK3749 is an N-channel vertical MOS FET. Because it can be driven by a voltage as low as 2.5 V and it is not necessary to consider a drive current, this FET is ideal as an actuator for low-current portable systems such as headphone stereos and video cameras.

FEATURES

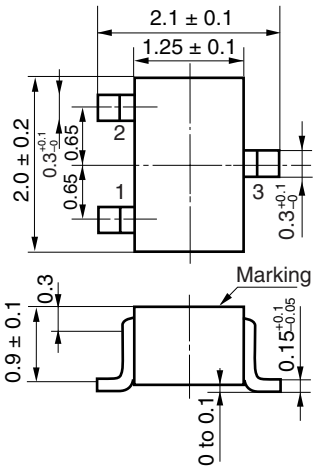
- Gate can be driven by 2.5 V
- Because of its high input impedance, there's no need to consider drive current

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3749	SC-70 (SSP)

Marking: G27

PACKAGE DRAWING (Unit: mm)



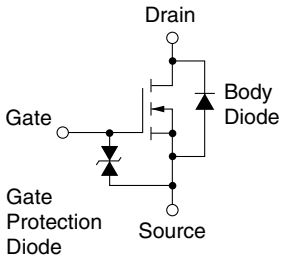
1 : Source
2 : Gate
3 : Drain

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	50	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±7.0	V
Drain Current (DC)	$I_{D(DC)}$	±100	mA
Drain Current (pulse) **Note**	$I_{D(pulse)}$	±200	mA
Total Power Dissipation	P_T	150	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Note PW ≤ 10 ms, Duty Cycle ≤ 50%

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

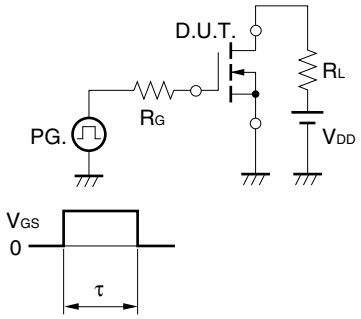
Document No. D17136EJ1V0DS00 (1st edition)
Date Published April 2004 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

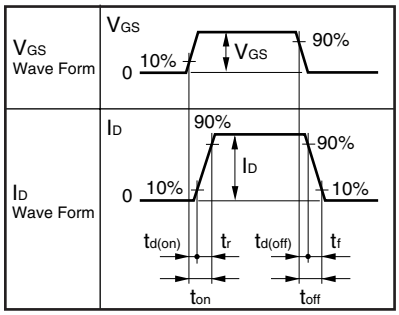
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V			1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±7.0 V, V_{DS} = 0 V			±5.0	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 3.0 V, I_D = 1.0 μA	0.9	1.2	1.5	V
Forward Transfer Admittance **Note**	$\|y_{fs}\|$	V_{DS} = 3.0 V, I_D = 10 mA	20			mS
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 2.5 V, I_D = 10 mA		20	40	Ω
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 10 mA		15	20	Ω
Input Capacitance	C_{iss}	V_{DS} = 3.0 V		6.0		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		8.0		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		1.2		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 3.0 V, I_D = 20 mA		9.0		ns
Rise Time	t_r	V_{GS} = 3.0 V		50		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		20		ns
Fall Time	t_f			40		ns

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT SWITCHING TIME

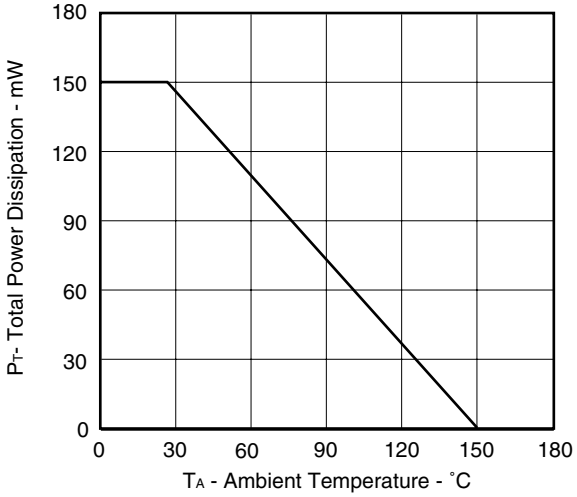


τ = 1 μs
Duty Cycle ≤ 1%

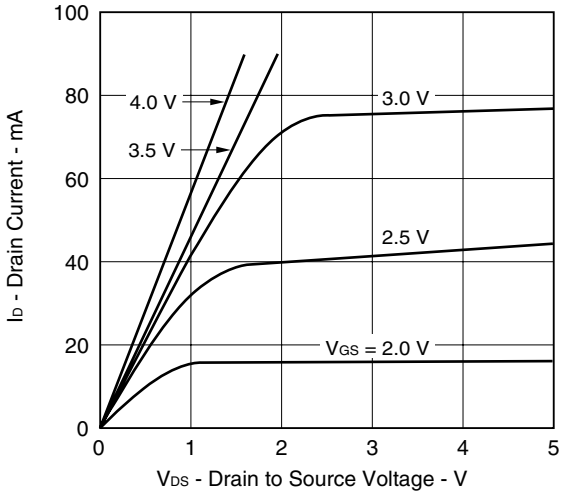


TYPICAL CHARACTERISTICS (T_A = 25°C)

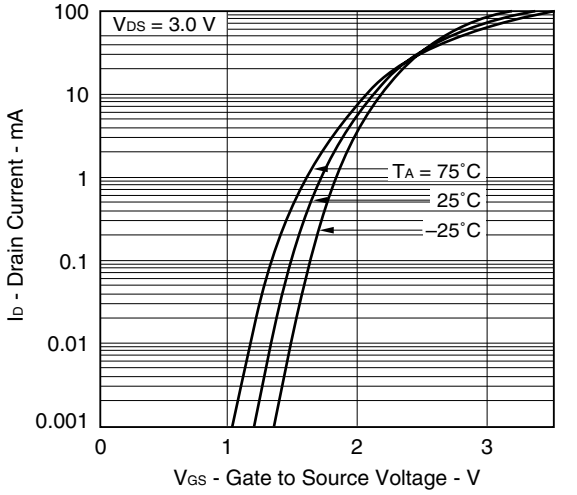
TOTAL POWER DISSIPATION vs. AMBIENT TEMPRATURE



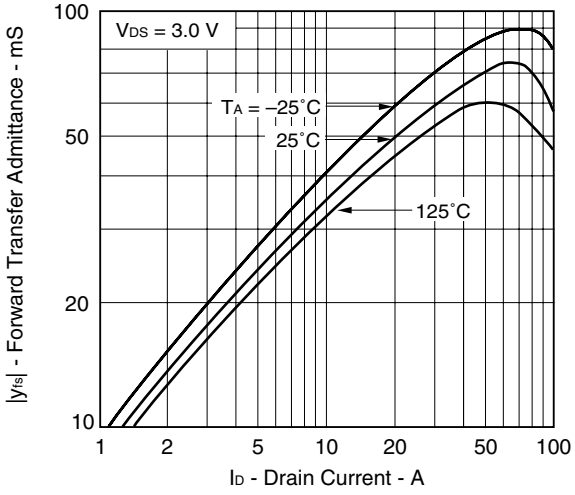
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



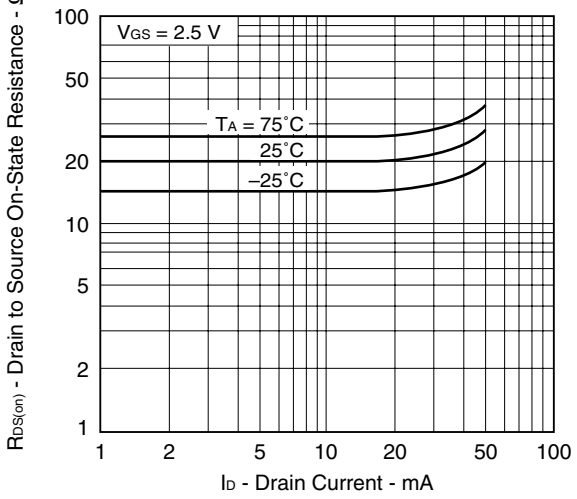
TRANSFER CHARACTERISTICS



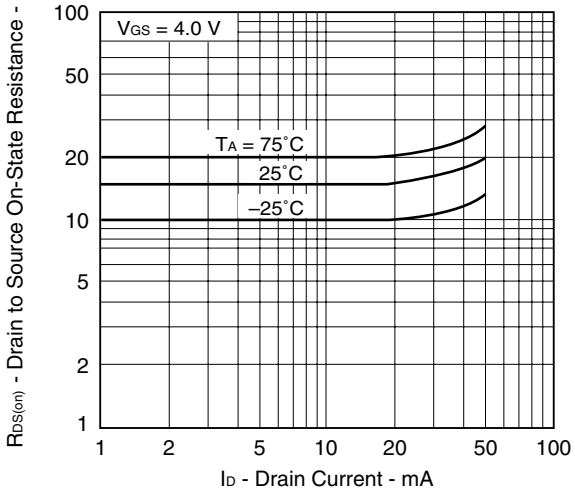
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



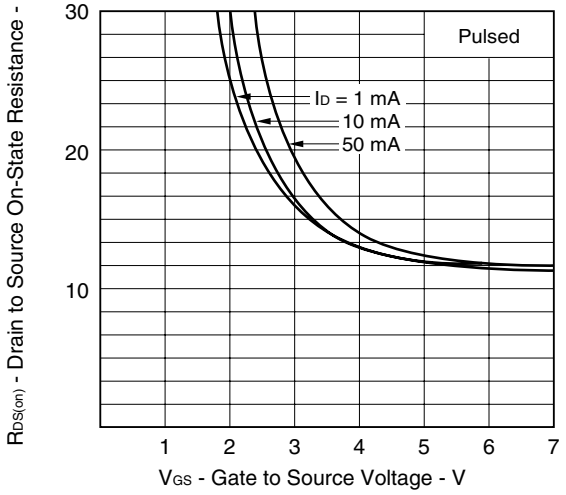
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



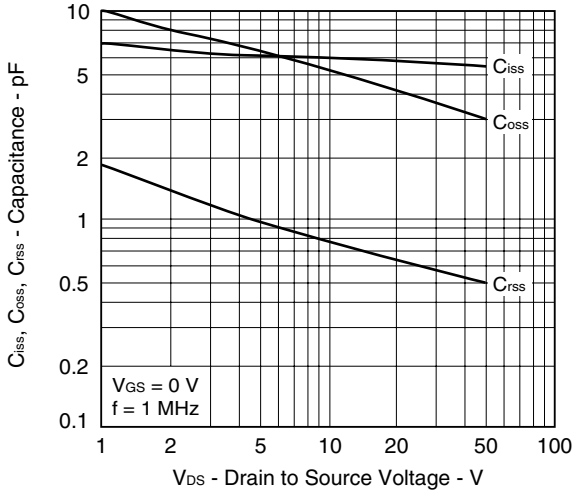
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



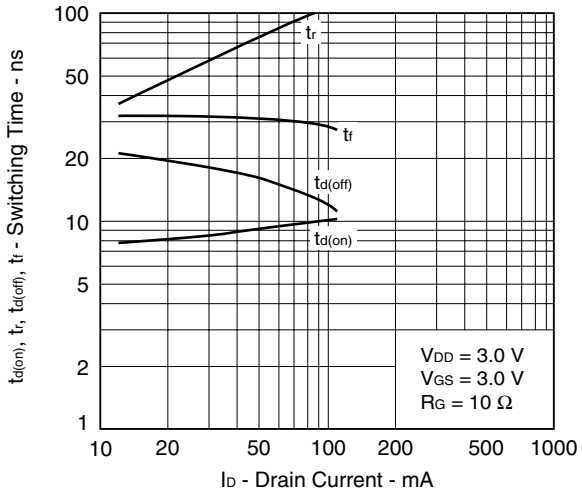
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



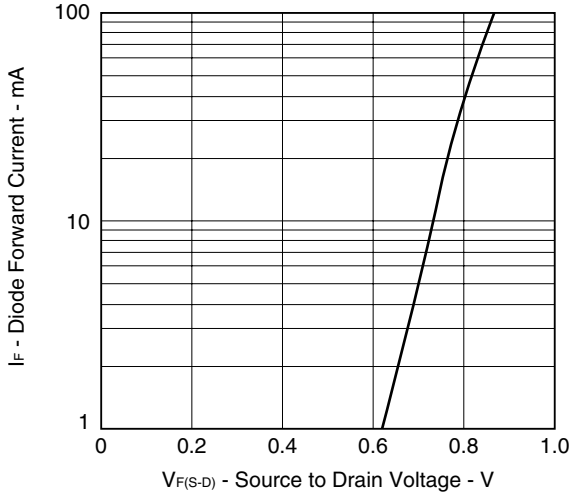
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



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