

SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

## DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

## FEATURES

- Low On-State Resistance  
 $R_{DS(on)1} = 18 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 17 \text{ A)}$   
 $R_{DS(on)2} = 27 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 17 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 2100 \text{ pF TYP.}$
- Built-in Gate Protection Diode
- TO-251/TO-252 package

## ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3225	TO-251
2SK3225-Z	TO-252

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	$\pm 20$	V
Gate to Source Voltage	$V_{GSS(DC)}$	+20, -10	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 34$	A
Drain Current (Pulse) <sup>Note</sup>	$I_{D(pulse)}$	$\pm 136$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	40	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

**Note**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

## THERMAL RESISTANCE

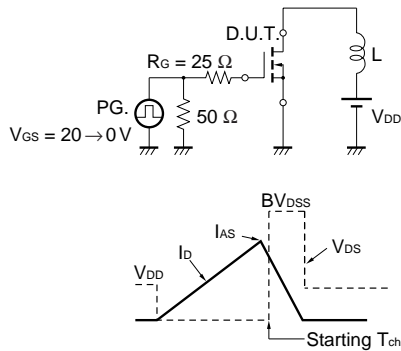
Channel to Case	$R_{th(ch-C)}$	3.13	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

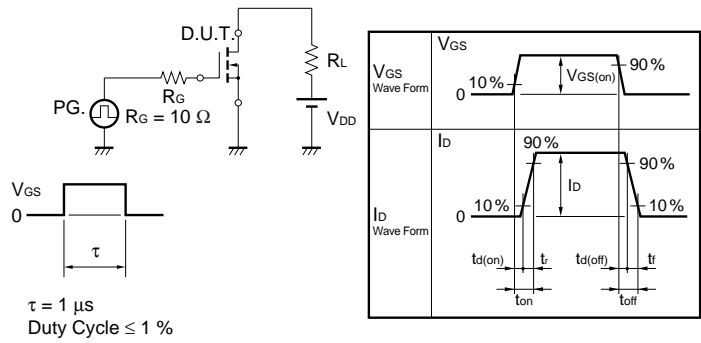
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17 A		13	18	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 17 A		18	27	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 17 A	13	27		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		2100		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		550		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		220		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 17 A		32		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		300		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		110		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		140		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 34 A		45		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 48 V		7		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS(on)</sub> = 10 V		13		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 34 A, V <sub>GS</sub> = 0 V		0.94		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 34 A, V <sub>GS</sub> = 0 V		60		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		95		nC

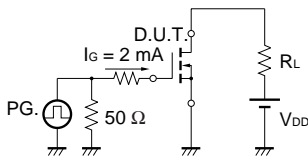
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

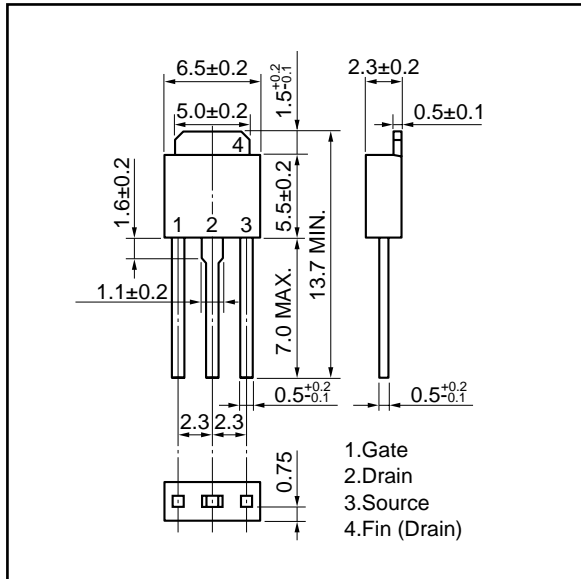


**TEST CIRCUIT 3 GATE CHARGE**

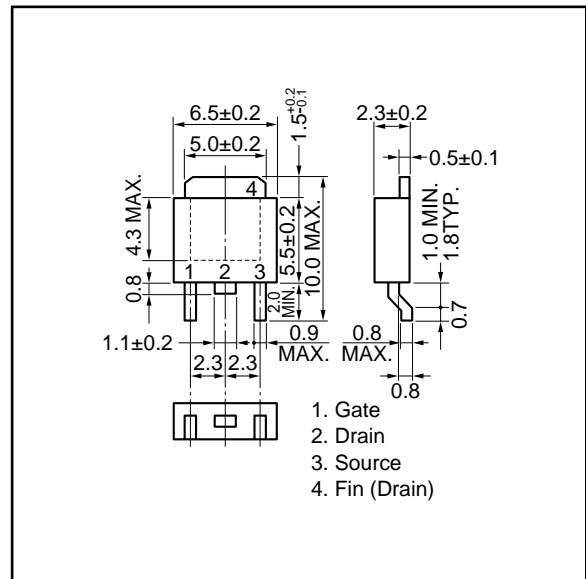


PACKAGE DRAWINGS (Unit : mm)

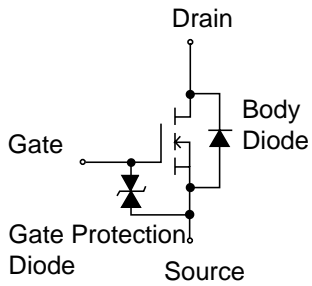
1)TO-251 (MP-3)



2)TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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