# 2SK3076(L),2SK3076(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

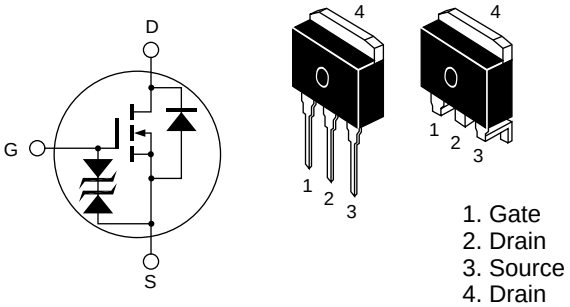
ADE-208-656 (Z)
1st. Edition
Jun 1998

## Features

- Low on-resistance
- High speed switching
- Low drive current.
- Built-in fast recovery diode (trr=120 ns)

## Outline

LDPAK




1. Gate
2. Drain
3. Source
4. Drain

Hitachi semiconductor

## Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 500 | V |
| Gate to source voltage | $V_{GSS}$ | ±30 | V |
| Drain current | $I_D$ | 7 | A |
| Drain peak current | $I_{D(pulse)}$ Note1 | 28 | A |
| Body-drain diode reverse drain current | $I_{DR}$ | 7 | A |
| Channel dissipation | Pch Note2 | 60 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C

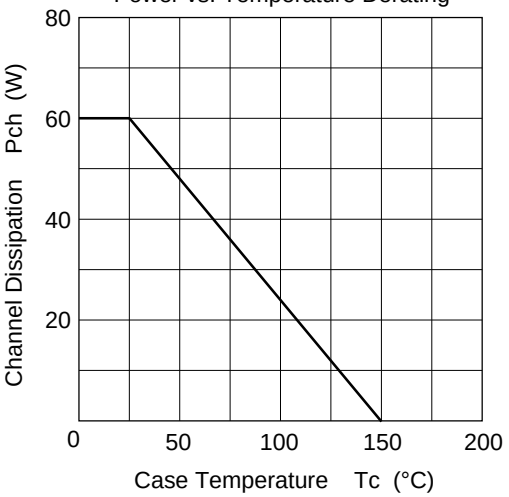
## Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 500 | — | — | V | $I_D$ = 10mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±30 | — | — | V | $I_G$ = ±100µA, $V_{DS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±25V, $V_{DS}$ = 0 |
| Zero gate voltege drain current | $I_{DSS}$ | — | — | 250 | µA | $V_{DS}$ = 400 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 2.0 | — | 3.0 | V | $I_D$ = 1mA, $V_{DS}$ = 10V |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.7 | 0.9 | Ω | $I_D$ = 4A, $V_{GS}$ = 10V Note4 |
| Forward transfer admittance | $\|y_{fs}\|$ | 3.5 | 6.0 | — | S | $I_D$ = 4A, $V_{DS}$ = 10V Note4 |
| Input capacitance | Ciss | — | 1100 | — | pF | $V_{DS}$ = 10V |
| Output capacitance | Coss | — | 310 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 50 | — | pF | f = 1MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 15 | — | ns | $I_D$ =4A, $V_{GS}$ = 10V |
| Rise time | $t_r$ | — | 55 | — | ns | $R_L$ = 7.5Ω |
| Turn-off delay time | $t_{d(off)}$ | — | 100 | — | ns | |
| Fall time | $t_f$ | — | 48 | — | ns | |
| Body–drain diode forward voltage | $V_{DF}$ | — | 0.9 | — | V | $I_F$ = 7A, $V_{GS}$ = 0 |
| Body–drain diode reverse recovery time | $t_{rr}$ | — | 120 | — | ns | $I_F$ = 7A, $V_{GS}$ = 0<br>diF/ dt =100A/µs |

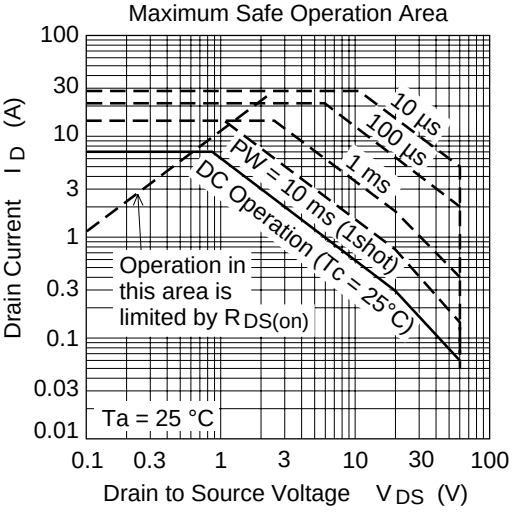
Note: 4. Pulse test

## Main Characteristics

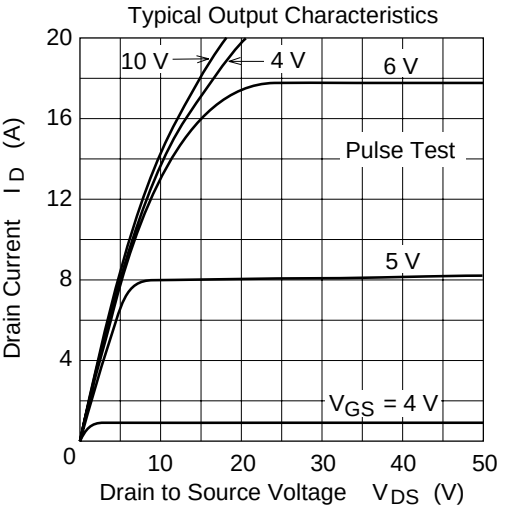
Power vs. Temperature Derating



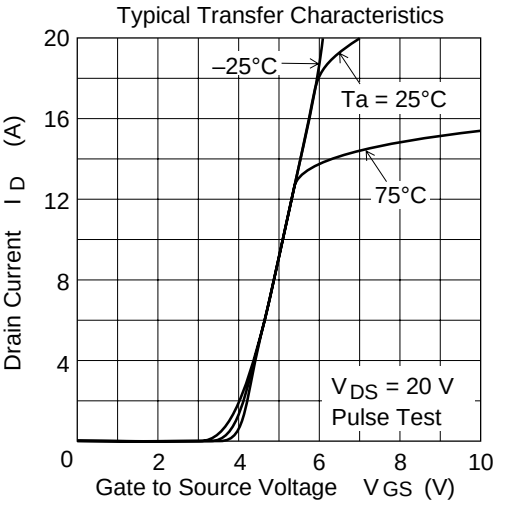

Maximum Safe Operation Area



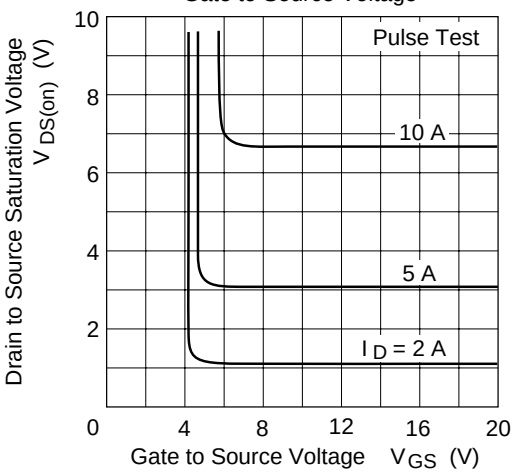

Typical Output Characteristics



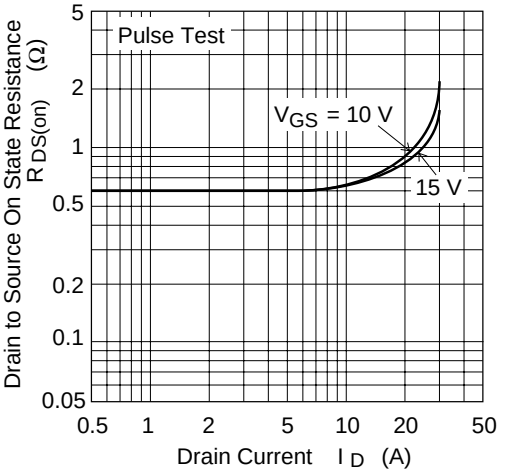

Typical Transfer Characteristics



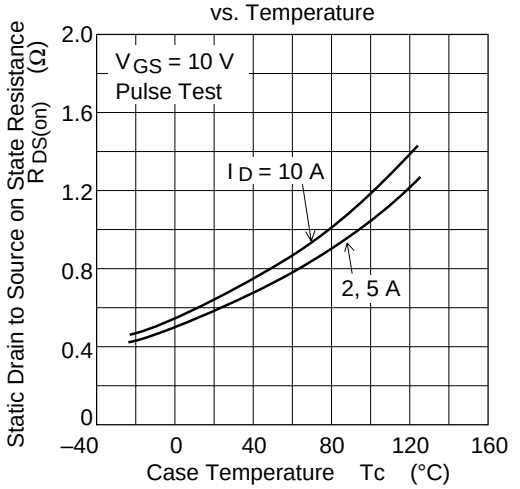
Drain to Source Saturation Voltage vs. Gate to Source Voltage



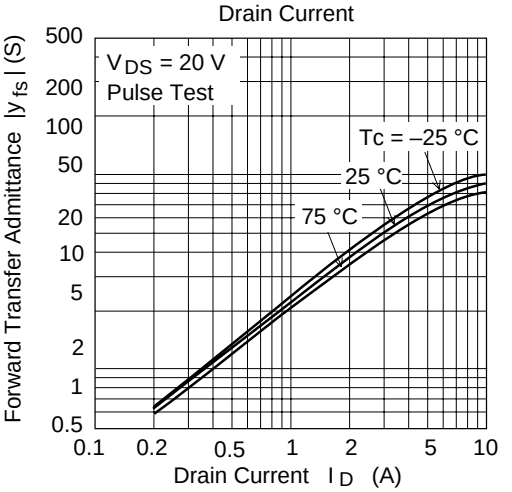

Static Drain to Source on State Resistance vs. Drain Current



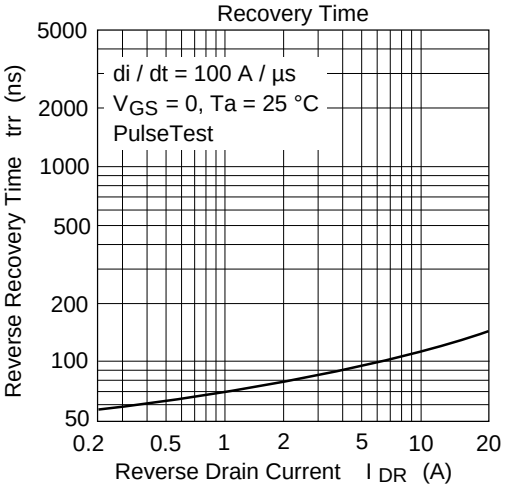

Static Drain to Source on State Resistance vs. Temperature



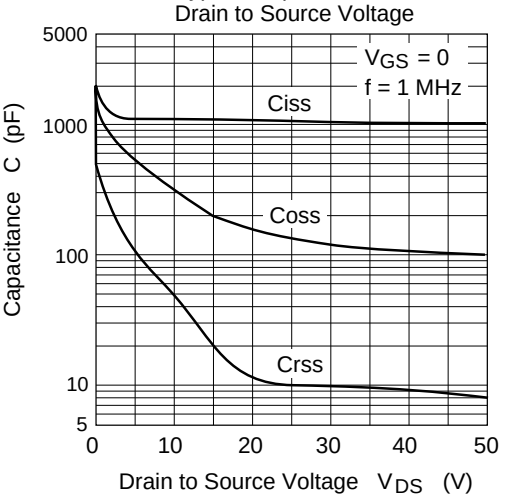

Forward Transfer Admittance vs. Drain Current



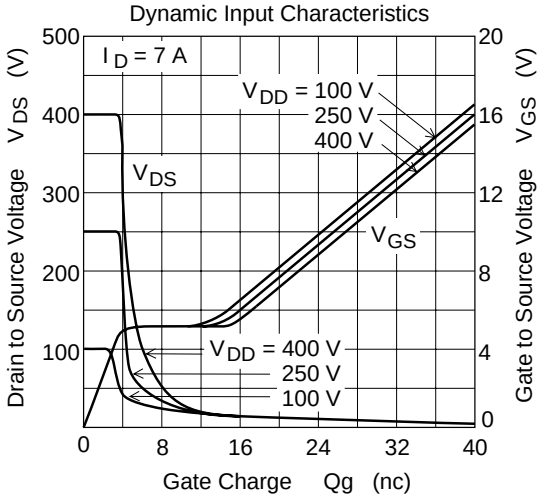
Body–Drain Diode Reverse Recovery Time



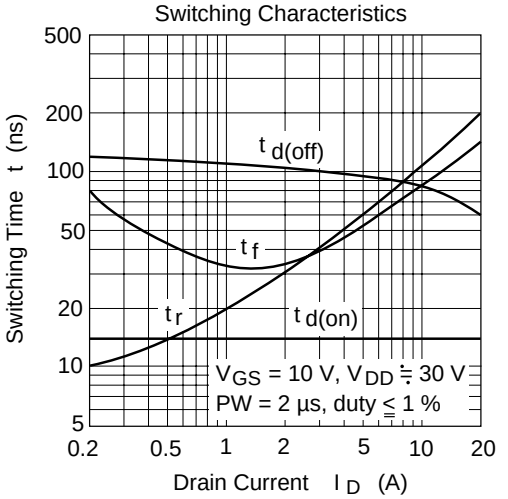

Typical Capacitance vs. Drain to Source Voltage

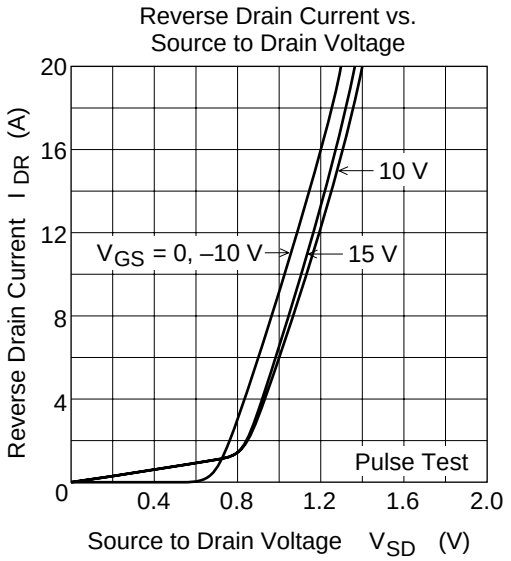


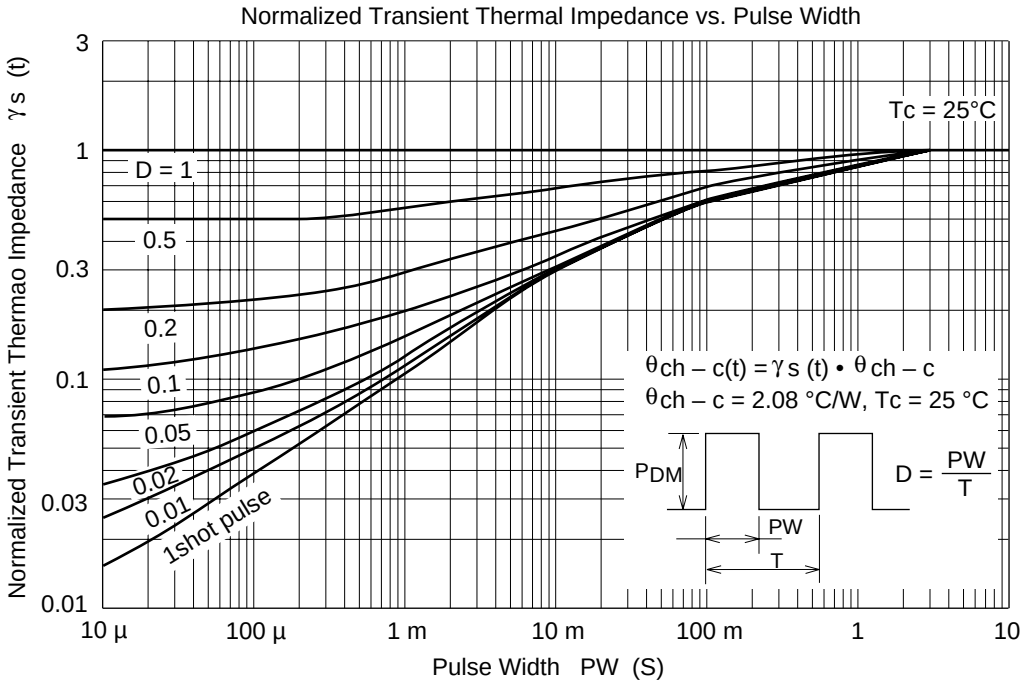

Dynamic Input Characteristics



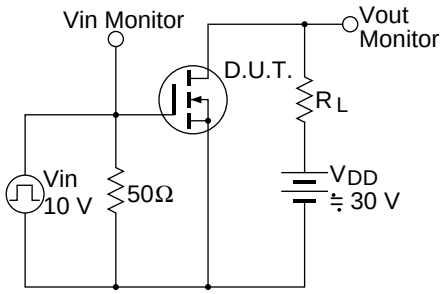

Switching Characteristics



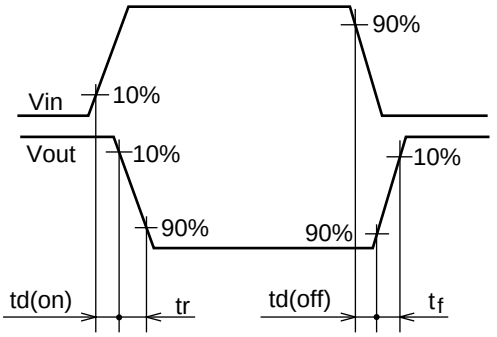

Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
20
16
12
8
4
0
10 V
VGS = 0, –10 V
15 V
Pulse Test
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage VSD (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermao Impedance γs (t)
3
1
0.3
0.1
0.03
0.01
Tc = 25°C
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch – c(t) = γs (t) • θch – c
θch – c = 2.08 °C/W, Tc = 25 °C
PDM
D = PW / T
PW
T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (S)

Switching Time Test Circuit

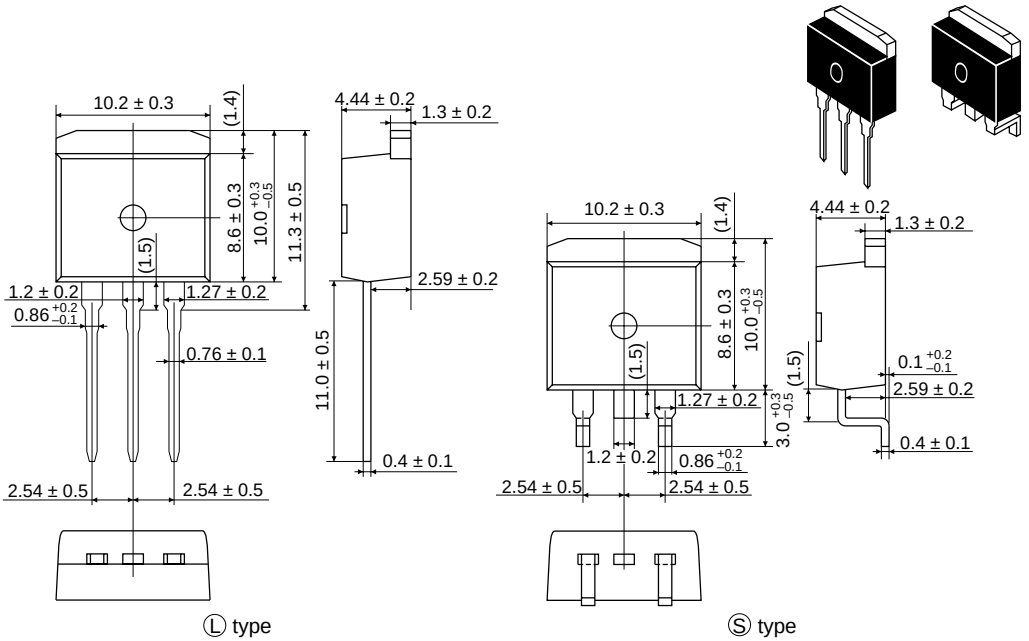



Waveform



## Package Dimensions

**Unit: mm**

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