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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2958(L),2SK2958(S)

Silicon N Channel MOS FET
High Speed Power Switching

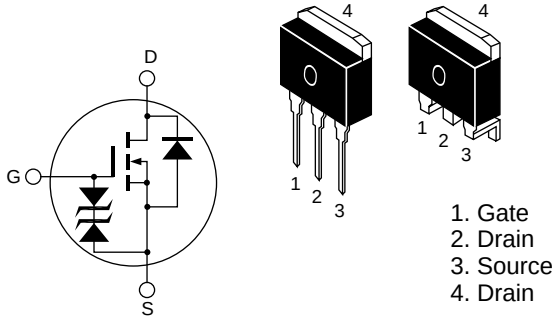
ADE-208-568B (Z)
3rd. Edition
Jul. 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 5.5mΩ typ.
- 4V gate drive devices.
- High speed switching

Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ Note1	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Channel dissipation	Pch Note2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C

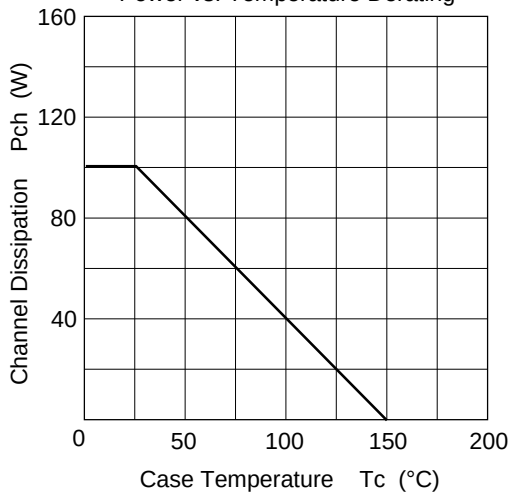
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	5.5	7.0	mΩ	I_D = 40A, V_{GS} = 10V Note3
Static drain to source on state resistance	$R_{DS(on)}$	—	9.0	14.0	mΩ	I_D = 40A, V_{GS} = 4V Note3
Forward transfer admittance	$\|y_{fs}\|$	35	60	—	S	I_D = 40A, V_{DS} = 10V Note3
Input capacitance	Ciss	—	4100	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	2700	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	800	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	V_{GS} = 10V, I_D = 40A
Rise time	t_r	—	430	—	ns	R_L = 0.25Ω
Turn-off delay time	$t_{d(off)}$	—	460	—	ns	
Fall time	t_f	—	440	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 75A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	I_F = 75A, V_{GS} = 0 diF/ dt =50A/µs

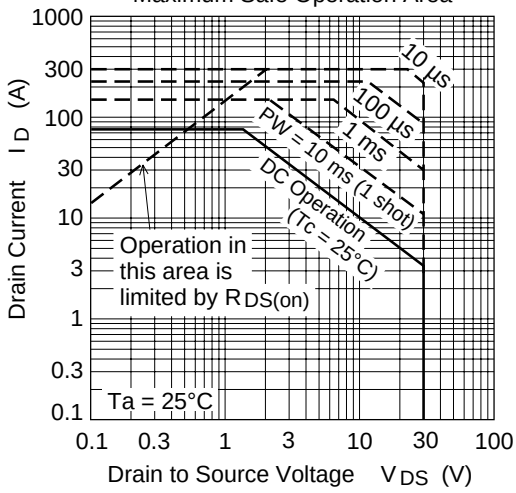
Note: 3. Pulse test

Main Characteristics

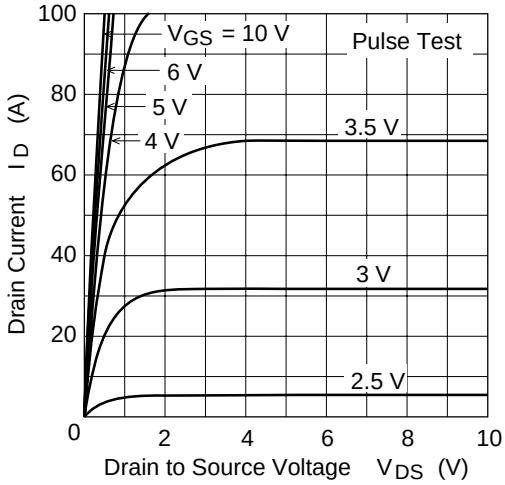
Power vs. Temperature Derating



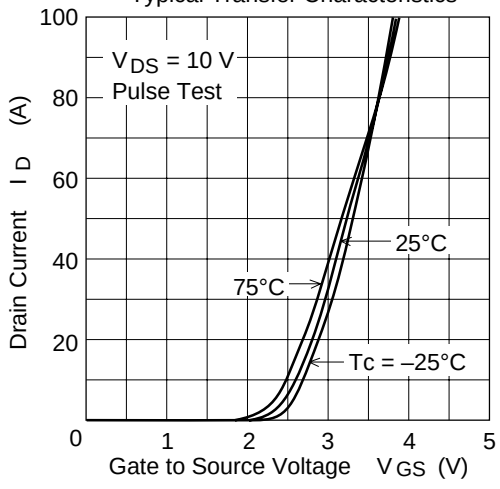
Maximum Safe Operation Area



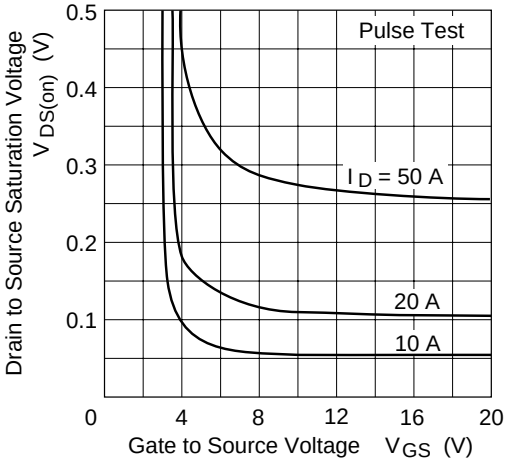
Typical Output Characteristics



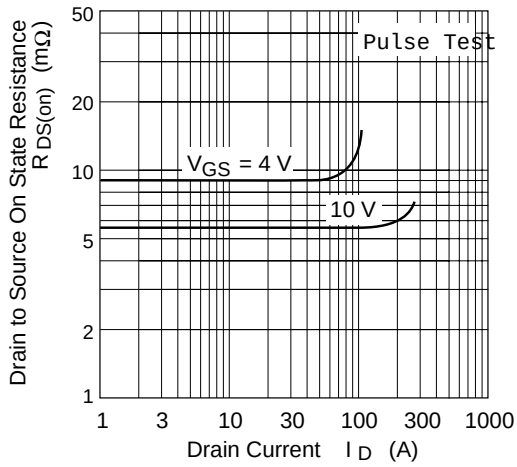
Typical Transfer Characteristics



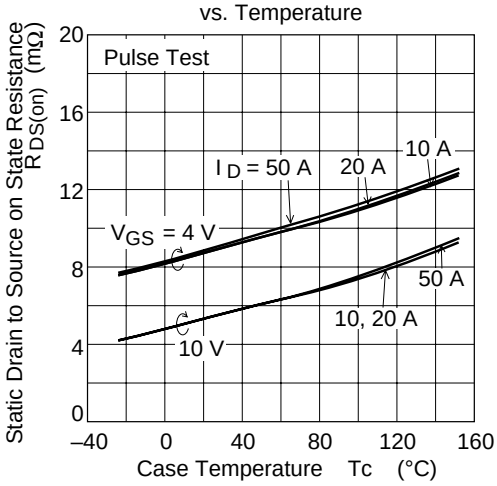
Drain to Source Saturation Voltage vs. Gate to Source Voltage



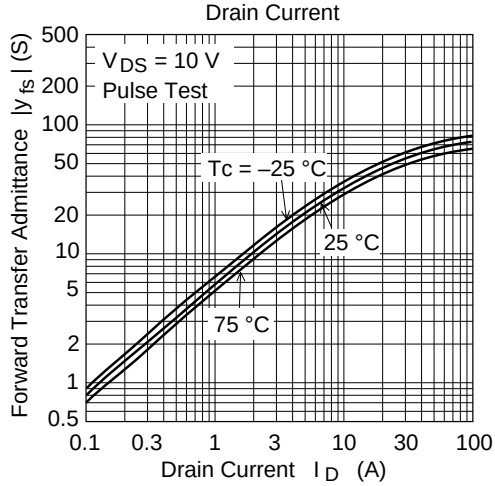
Static Drain to Source on State Resistance vs. Drain Current



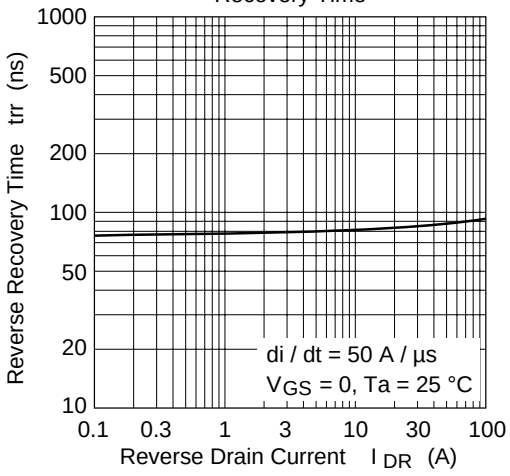
Static Drain to Source on State Resistance vs. Temperature



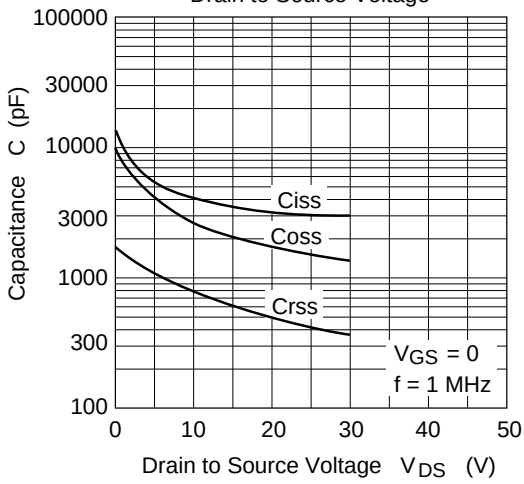
Forward Transfer Admittance vs. Drain Current



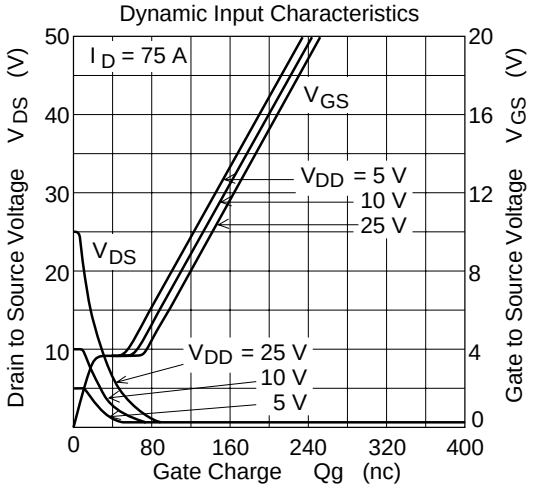
Body–Drain Diode Reverse Recovery Time



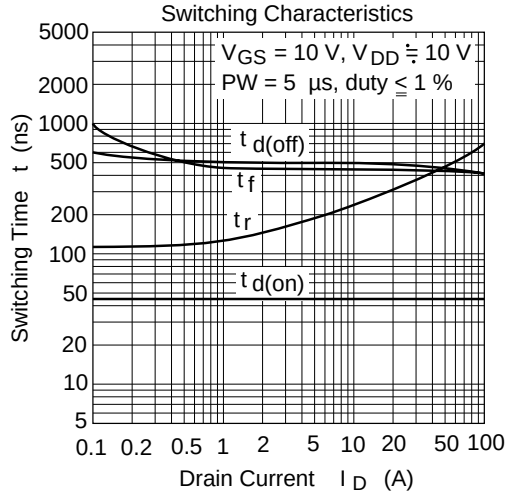
Typical Capacitance vs. Drain to Source Voltage



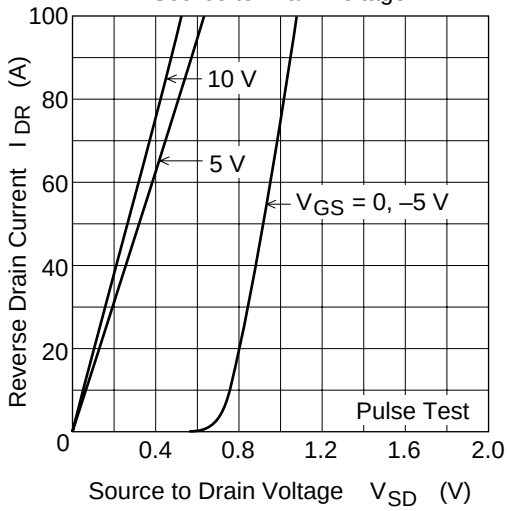
Dynamic Input Characteristics



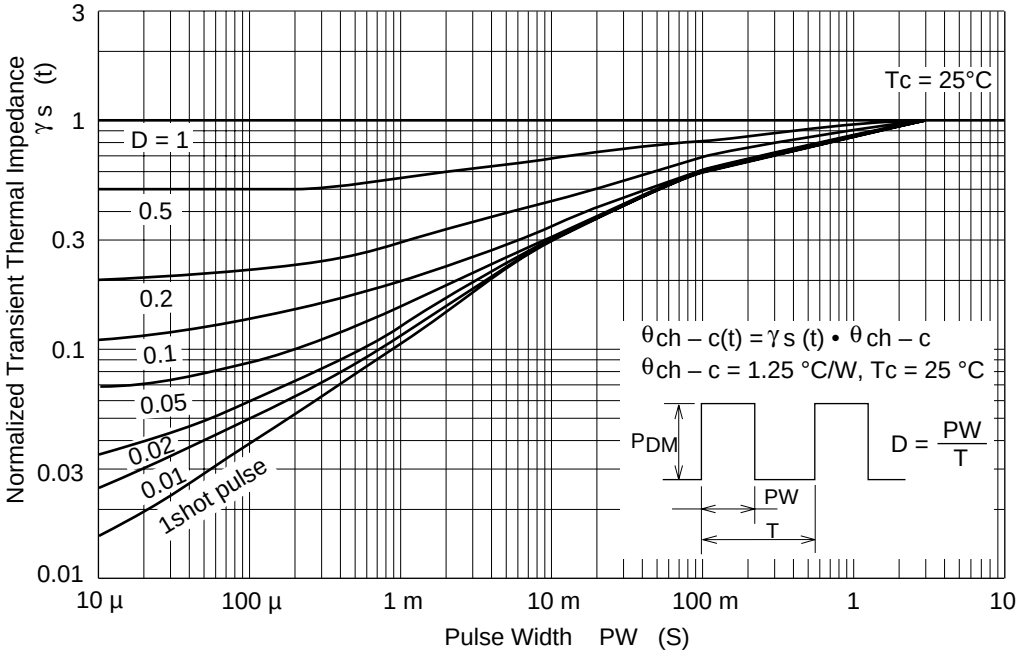
Switching Characteristics



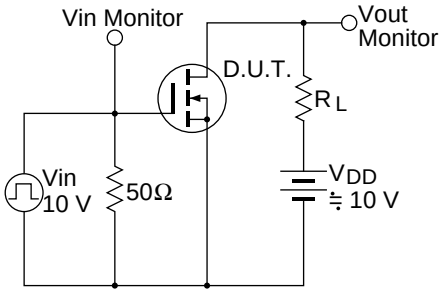
Reverse Drain Current vs.
Source to Drain Voltage



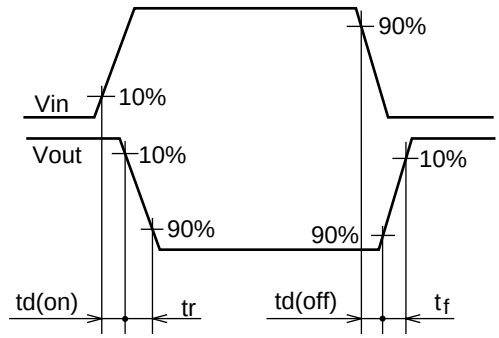
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



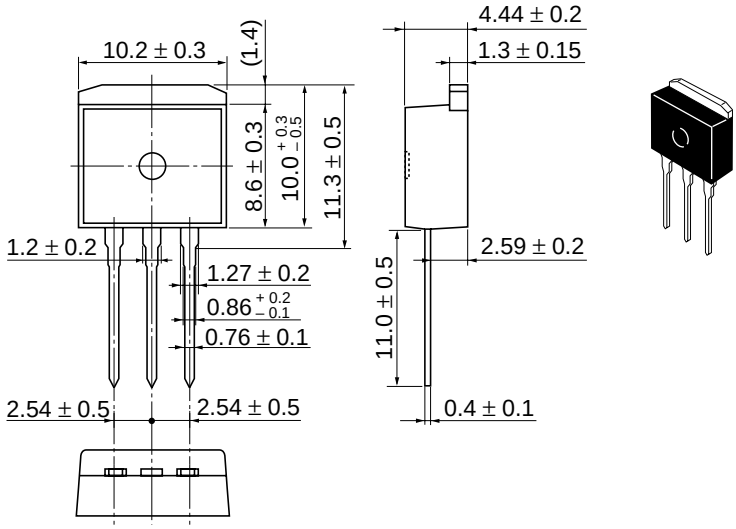
Waveform



Package Dimensions

As of January, 2001

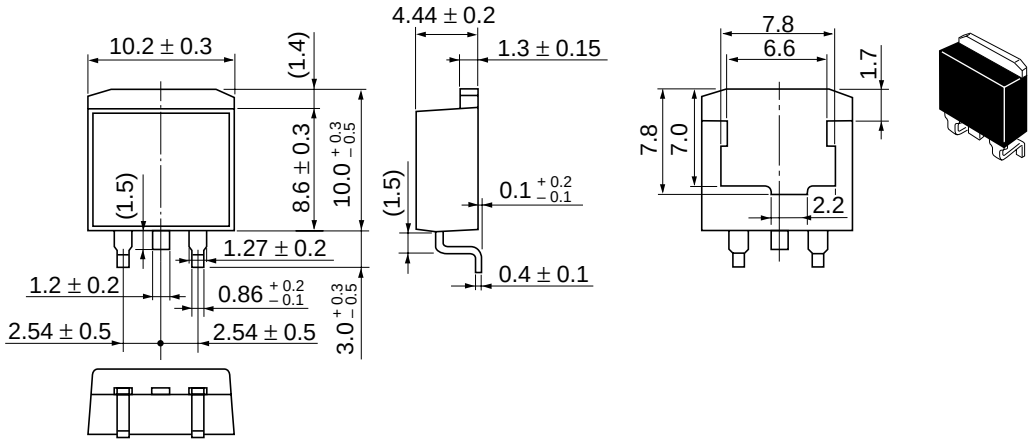
Unit: mm



Hitachi Code	LDPAK (L)
JEDEC	—
EIAJ	—
Mass (reference value)	1.4 g

As of January, 2001

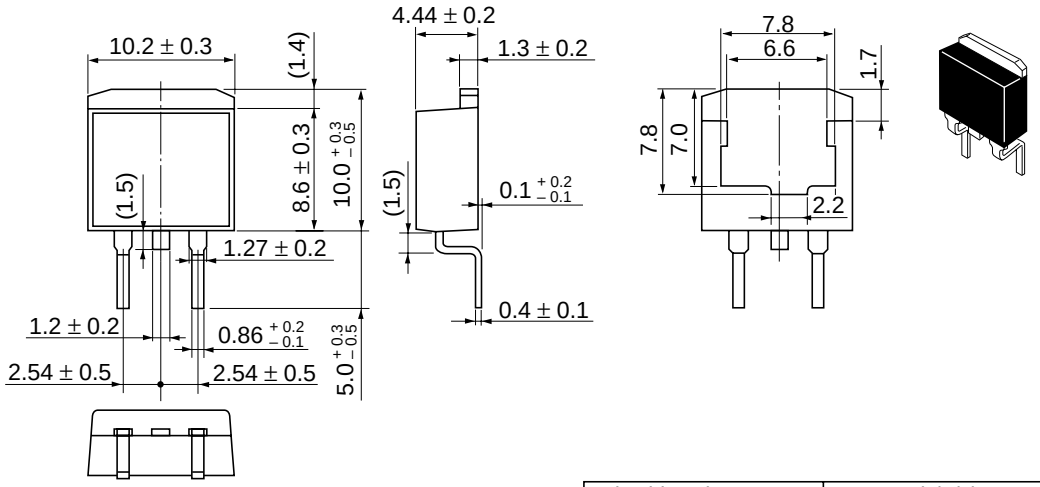
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
EIAJ	—
Mass (reference value)	1.3 g

As of January, 2001

Unit: mm



Hitachi Code	LDPAK (S)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	1.35 g

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